High-Precise Portable Time Interval and Frequency Counter

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Abstract—We describe a precise, portable time interval and frequency counter module controlled and powered via the USB port. To obtain both wide measurement range and high precision the counting of periods of a reference clock is combined with a two-stage interpolation within a single clock period. In the second stage of interpolation newly developed multiple independent coding lines are used to provide the time-to-digital conversion with a resolution of 1.8 ps and precision not worse than 10 ps. The counter module allows measurement of time intervals within the range from 0 up to 1000 s and frequency from 1 mHz up to 3.5 GHz. The main units of the counter are integrated in an FPGA device. The on-board DDR RAM memory supported by a dedicated memory controller block, integrated in FPGA, allows the decrease of the dead time of the counter and achieves the maximum measurement rate of 5×10^6 measurements per second. The comprehensive control, diagnostics, and statistical data processing are provided by the dedicated software.

I. INTRODUCTION

Picosecond-level time interval measurements take place in various precise instruments developed for timekeeping, laser range finding, testing of electronic devices, navigation, geodesy, and high energy physics. The first precise time counters were built from the beginning of the 70's of the last century with the use of the interpolating method with analogue expansion [1–3]. Among typical examples of such counters the following should be mentioned: the family of instruments for laser measurements from the Earth orbit [4, 5], the multichannel time interval counter [6], the universal time counter HP5335A [7] mass-produced by the *Hewlett-Packard Company* (HP), and the series of precise time counters T-1500, T-1600 and T-1700 [8, 9] developed at the Military University of Technology (MUT, Poland) for testing of electronic elements and precise laser range finding. In the course of time, instead of analogue time expanders, the time-amplitude-digital converters have been used for precise time digitizing. Such a solution was applied in the precise time counter T-1810B, developed at the MUT [10] and in the universal time counter SR620 manufactured by *Stanford Research Systems* (SRS) [11]. Due to its high precision, the counter SR620 became a part of the standard equipment of many research and industrial laboratories.

Rapid development of CMOS technology at that time led to precise but large, heavy and consuming a lot of power, stationary time counters that began to be displaced by instruments based on integrated circuits. The first time counters of that type were designed and developed at the beginning of the 90's. For example, in 1993, the research team of European Organization for Nuclear Research (CERN, Switzerland) developed the 16-channel time counter with the resolution of 1.56 ns and measurement range of 205 ms [12]. Three years later the research team from the University of Oulu (Finland) developed a 9-channel time counter with a higher resolution (625 ps) for a laser range finder for three-dimensional imaging [13]. Both counters were designed with the use of CMOS technology and developed as *Application Specific Integrated Circuits* (ASIC). Such integrated circuits customized for a particular use are characterized by a long and expensive process of design and fabrication. At the same time the first interpolation counter in a cheaper and more commonly available *Field Programmable Gate Arrays* (FPGA) technology were

developed and the resolution of 200 ps was achieved [14, 15]. Thanks to further improvements in construction and the use of newer series of FPGA devices this resolution has been doubled [16].

The steady increase in requirements for precise time interval measurements and development of the electronic technology caused that, in the last decade, the time counters began to be designed also in the form of PC cards. One of the first constructions of this type was the measurement card GT200 (*Geotest*) [17]. Other examples are the time and frequency counters designed at the MUT with the use of programmable devices. First of them, designed in 2002, allowed to measure of time interval, frequency, period, pulse parameters and pulse counting in time gate [18]. In 2009, the same team designed another counter based on the new method with direct time-to-digital (T/D) conversion in two independent, discrete time coding lines [19]. This solution provided the resolution of 25 ps and precision below 35 ps within a wide measurement range (> 1h) [19, 20]. Based on that counter, series of measurement cards with PCI, USB or Wi-Fi interface were developed. The module with Wi-Fi interface is the first and so far the only available device of this type.

The idea of two independent coding lines [19] was expanded for the case of multiple (up to 16) coding lines [21]. Then we used the technique of multiple coding lines to design an FPGA-based time and frequency counter, which serve us to develop a versatile portable counter module. This paper contains general information about the counter module.

II. TIME COUNTER ARCHITECTURE

The block diagram of the time counter module is presented in Figure 1. Time intervals are precisely measured with the use of two-stage interpolation method, which combines the well known counting method and a precise T/D conversion within a narrow range. The counting method is easily implemented in integrated circuits and provides wide measurement range. Its main drawback consists in the low resolution equal to the period of reference clock. The microelectronic technology limits the frequency of such clock to few hundreds of megahertzs. It means that the resolution of the counting method cannot be higher than few nanoseconds. To improve the resolution a precise T/D conversion within a single clock period has to be used. Typically for T/D conversion in integrated circuits the tapped delay lines are involved. They allow to increase the resolution by even hundred times with regards to the counting method. However, the resolution is again limited by technology to the value of propagation time of a single delay element used to create a delay line. This limitation can be overcome by the use of multiple time coding lines (TCLs) [21]. Such lines should be reasonably short to prevent the conversion nonlinearity from increasing. Therefore multistage interpolation is naturally recommended. In our time counter there is two-stage interpolation, and thus a four-phase clock (FPC) is used in the first interpolation stage (FIS) and multiple TCLs in the second interpolation stage (SIS). The number of TCLs has an effect on the resolution of T/D conversion and doubling of the number of lines results in an increase in the resolution by about two times. In the presented time counter we implemented ten TCLs. In this way, the coarse resolution of the counting method equaled to 2 ns (period of the 500 MHz reference clock) is first improved fourfold in the FIS and next, even more than 277 times in the SIS, finally reaching 1.8 ps.

The start and end of a measured time interval are represented by two consecutive pulses applied to inputs A and B of the counter. The value of the time interval is calculated from the following formula: $T = NT_C + (T_{ST1} + T_{ST2}) - (T_{SP1} + T_{SP2})$ [3, 21]. The product NT_C consists of an integer number N of such clock periods T_C, whose leading pulse edges appeared at the input of the period counter during a measurement. The time interval between the first input pulse, applied to input A, and the nearest edge of the reference clock is simultaneously measured by two stages of interpolator START. The FIS detects the nearest edge of the FPC that appeared after the input pulse (ST). Since the edge is synchronized with the reference clock and widths of the FPC time segments are known from calibration, the time T_{ST1} between this FPC edge and the nearest edge of the reference clock can be precisely calculated. In the SIS the time interval T_{ST2} between the input pulse (ST) edge and the nearest FPC edge is measured.

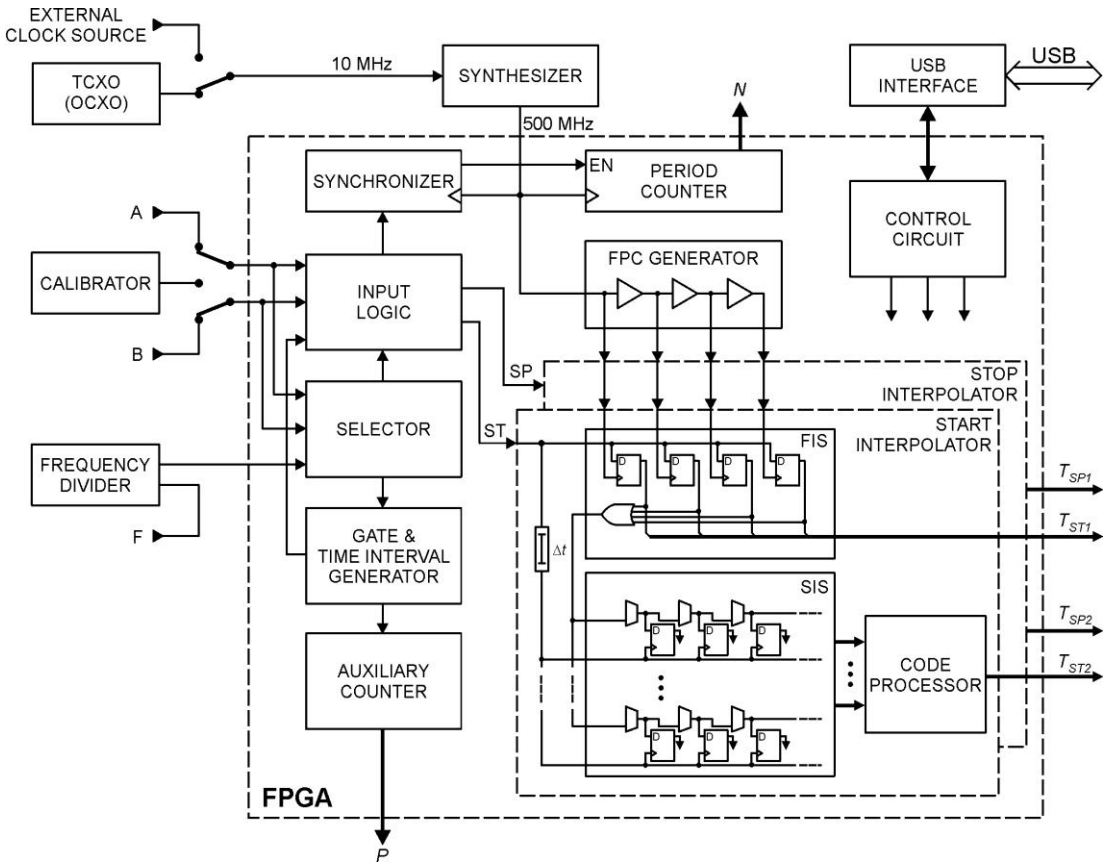

Figure 1. Simplified block diagram of the counter module.

The reference clock of 500 MHz frequency is created based on the signal from the on-board 10 MHz quartz generator. Typically the counter module is equipped with the temperature compensated quartz oscillator (TCXO), which optionally can be exchanged with a more stable oven-controlled quartz oscillator (OCXO). If higher long-term frequency stability is needed an external clock signal, for example from an atomic standard, can be used.

The precise time interval measurement is a basis for other measurement modes of this counter. The frequency of an input signal is measured with the use of the reciprocal method by measuring the time interval consisting of integer number of signal periods, counted in selected gate, calculating the duration of a single period, and evaluating its reciprocal. For this purpose the gate and time interval generator, implemented in the FPGA device, generates eight gates (from 1 μs to 10 s in decade steps) selectable with the aid of the virtual control panel. Simultaneously, the same block generates the time interval, which precisely corresponds to the duration time of an integer number *P* of signal periods that fitted into the selected gate. This time interval is then measured using the two-stage interpolation method. There are three inputs on the counter board that can be used for frequency measurements. Two of them (A and B) are intended for signals with frequency below 200 MHz, which can be measured directly by the FPGA chip. When the frequency exceeds 200 MHz the measurements are carried out with the aid of a frequency divider chip, which is connected to the F input. This extends the range of measured frequency up to 3.5 GHz.

The counter module has built-in calibration circuit, which allows to perform two consecutive calibration procedures. In the first one the transfer characteristics of both interpolators (START and STOP) are identified. It is accomplished by the code processor that first evaluates widths of quantization steps of all TCLs and then creates the transfer characteristics of a virtual equivalent coding line (ECL) for each interpolator. These characteristics are saved in the internal RAM memory and used during ordinary

measurements. The second calibration procedure calculates the time offset between the inputs A and B. Both calibration procedures are performed automatically after each power on. Since the calibration routine is short, about 5 s, it can be repeated appropriately to changes in thermal condition, power supply or due to any other disturbances. The rate of repetition can be set manually by the user or can be determined automatically by the control software according to the drift of calibration data. The calibration procedure can also be initiated in any time by the user.

III. CODING LINE IMPLEMENTATION

The main units of the counter are integrated in a single Spartan-6 FPGA device manufactured by *Xilinx* (USA) in a 45 nm CMOS technology. Main logic resources of this device are organized in configurable logic blocks (CLBs). Each of them is divided into pair of slices, which contain components of a fast carry-chain. Such a chain provides the shortest tapped delays in an FPGA device due to predefined interconnections between components of the chain. The carry-chain structure in a single slice of the Spartan-6 chip consists of four fast multiplexers (Fig. 2a). These multiplexers have short mean delays of about 19 ps. For these reason carry-chains are naturally predestined for implementing TCLs with a high resolution. We used them also in our time counter. Signal from input logic (ST or SP, Fig. 1) representing the begin of time interval measured in SIS is attached to the input Cin of the chain, while a clock signal (CLK, Fig. 2a) from FIS, distributed through a global clock network, is applied to clock inputs of all corresponding flip-flops. In this way the state of the chain after a measurement is given in the thermometric code. To take advantage of the use of multiple coding lines the mean value of results from all TCLs may be calculated. However, better resolution and precision of T/D conversion are obtained when the ECL is used [21]. The resolution of ECL is roughly as many times increased with regards to this of a single TCL as many TCLs are applied.

Since the frequency of the clock signal is relatively high (500 MHz), to ensure reliable operation of the counter most of its modules had to be placed and routed carefully. A special attention was paid to the right location of the FPC generator, FIS and synchronizer. The high uniformity of clock segments in the FPC generator was achieved by leveling off all inner-slice delays and propagation times of data paths. The FIS and synchronizer are based on double-synchronizer circuits. To obtain accurate operation of both blocks we manually routed the data paths between flip-flops involved. The optimal routing was obtained during a trial and error process. After obtaining appropriate layouts for FPC, FIS and synchronizer, they were saved as “placed and routed” hard macros that ensure exact implementation in FPGA device irrespective of subsequent compilations of the project.

The global clock network divides Spartan-6 device into several regions, within which the clock signal drives slices almost without a skew, while delay differences between clock paths in different clock regions can reach even hundreds of picoseconds. Thanks to the division of the clock period by four in the FIS, the length of a single TCL in the SIS could be shortened to 16 CLBs (64 multiplexers), and thus the whole line could be implemented in a single clock region. This significantly limits the nonlinearity of TCL. Ten TCLs were implemented in each interpolator of the counter. TCLs are located one to another (Fig. 2b) and all of them are in the same clock region. During tests we investigated an implementation of more number of lines (up to 16). However, obtained results showed that, in the context of achieving the high precision and for resource-saving, the optimal number of TCLs is between eight and ten [21].

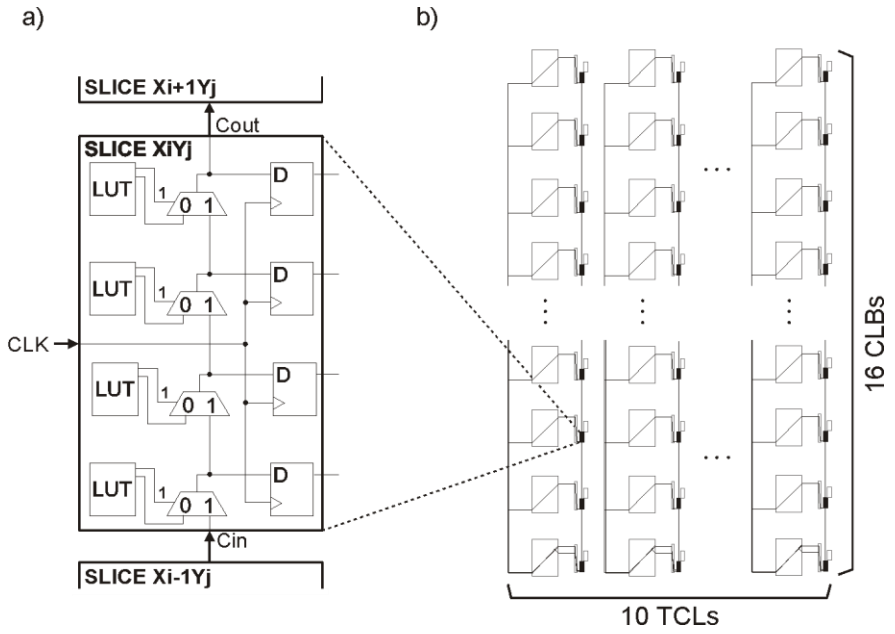

Figure 2. Implementation of TCL in a single slice of Spartan-6 (*Xilinx*) (a) and simplified layout of SIS (b).

IV. PORTABLE COUNTER MODULE AND DEDICATED SOFTWARE

The box, containing the time interval counter module, has small dimensions: 140 mm in length, 70 mm in width, and 17 mm in height (Fig. 3a). The power supply for the counter module is provided by two USB 2.0 ports. One of them is used also to control the counter. The internal view of the counter module is shown in Fig. 3b.

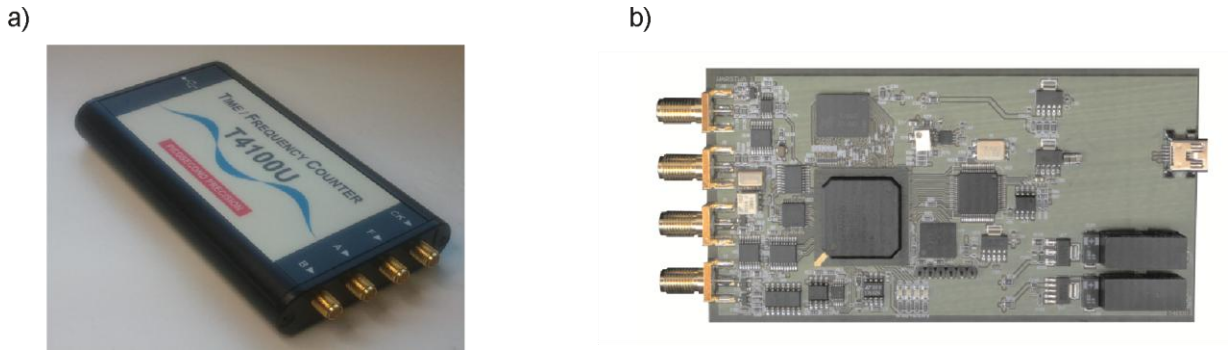

Figure 3. External view of the counter module (a) and the internal printed circuit board (b).

The dedicated software application displays on a PC monitor a user-friendly virtual front panel and provides advanced functions for control, diagnostics, and statistical processing of the measured data (Fig. 4). The software was developed using "Embarcadero RAD Studio XE" package and Delphi language. It communicates with a PC through the USB 2.0 Hi-Speed interface and ready-to-go royalty free USB drivers. Such drivers are provided by the Future Technology Devices International Limited (FTDI) for selected operation systems, for example: various versions of Windows, Linux, Mac OS, and Android. It allows users to write their own control software.

The counter supports six operation modes that include measurements of: Time Interval, Pulse Width, Frequency, Allan Deviation, Period, and the Totalize, in which the input pulses are counted within a preset time gate. Each of the mode is selected by clicking a predefined virtual key on the virtual front panel of the counter (Fig. 4). The appropriate options are then shown and a user can select, among others, an active input, the polarity and threshold of input signal, and various parameters concerning a chosen mode of operation (e.g., the gate duration in the Frequency mode). Next, a user can easily and thoroughly control the measurement process. Having finished the measurement session a user decides on the way of displaying the results (numerically or graphically) or storing the measurement data to a file. The data may also be exported to other programs for further processing. The control software automatically calculates and displays on the virtual front panel the mean value, the standard deviation, the minimum and maximum values for each measurement sample. It also provides histograms based on the measurement data.

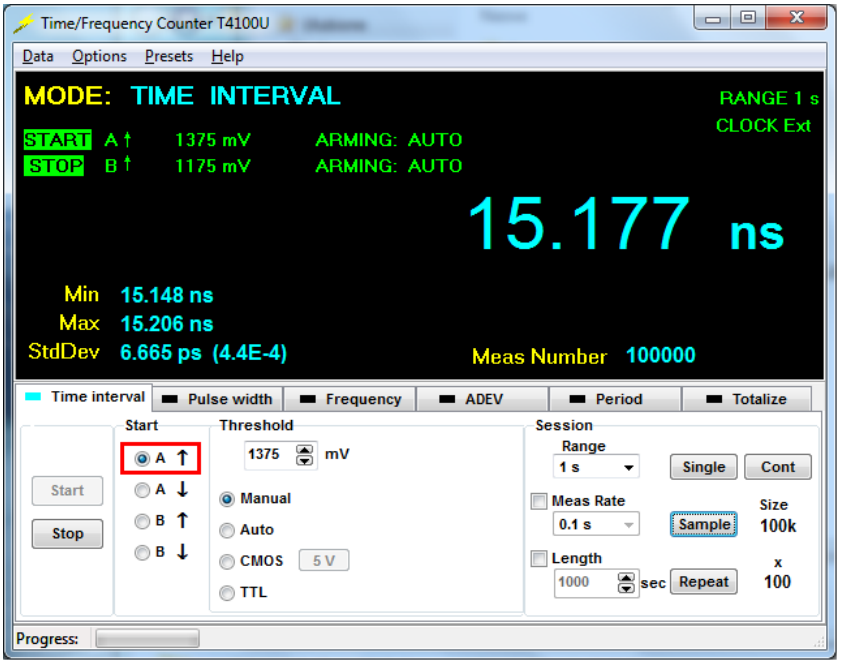

Figure 4. An example of the virtual front panel of the counter.

V. TEST RESULTS

Tests of the counter were performed with the use of the nominal supply voltages and in the ambient temperature of 20 ^{O}C. The rubidium standard FS725 (*SRS*) [22] and the GPS-disciplined quartz generator E8-Y (*Quartzlock*) [23] were used as sources of the reference clock for the counter and for the test time interval generators, respectively.

The first evaluated parameter was the time counter resolution. It was calculated as a mean value of bin widths of all TCLs involved. Ten TCLs in each interpolator allowed to reach the resolution of about 1.8 ps (1 LSB). Example characteristics of the differential (DNL) and integral (INL) nonlinearities of the START interpolator are shown in Fig. 5. The extreme values of DNL and INL are 6.23 LSB and –16.28 LSB, respectively. Corresponding values in the STOP interpolator are similar. Since the internal code processor (Fig. 2) performs on the fly correction of the measurement data, the INL is finally reduced to 0.12 LSB.

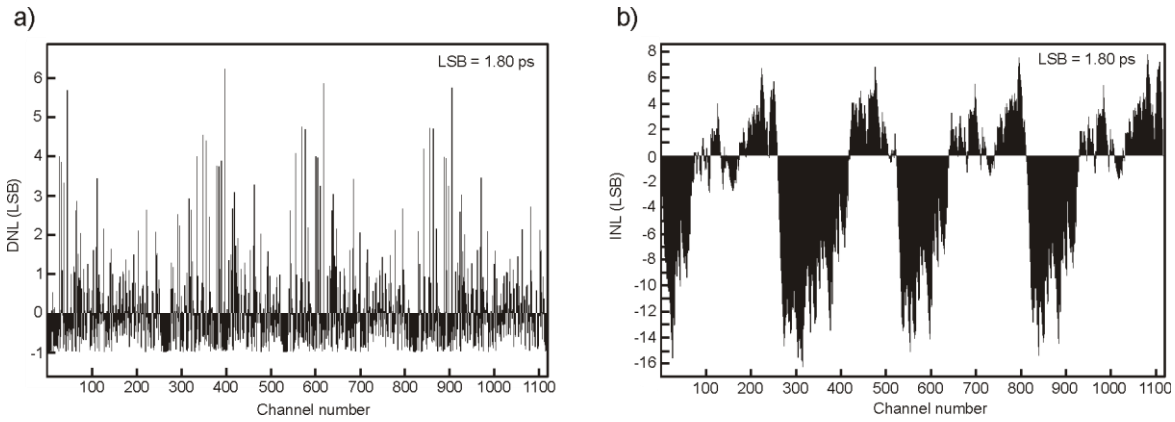

Figure 5. Differential (a) and integral (b) nonlinearities of the START interpolator.

Figure 6 shows the precision of our time counter (T4100U) that was obtained as the standard deviation calculated for a reasonably large measurement sample (1000). It is compared to precision of our previous counters (T2700U and T3200U) and two commercial and commonly used instruments (HP53132A, Agilent [24], SR620, *SRS* [11]). As test time interval generators we used three instruments: GFT1004 (*Greenfield Technology*) [25] for time intervals from 0 to 200 ns, 81130A (*Agilent*) [26] from 500 ns to 5 µs and T5300U (*Vigo Systems*) [22] for longer time intervals. They provide signals with the lowest jitter within selected ranges.

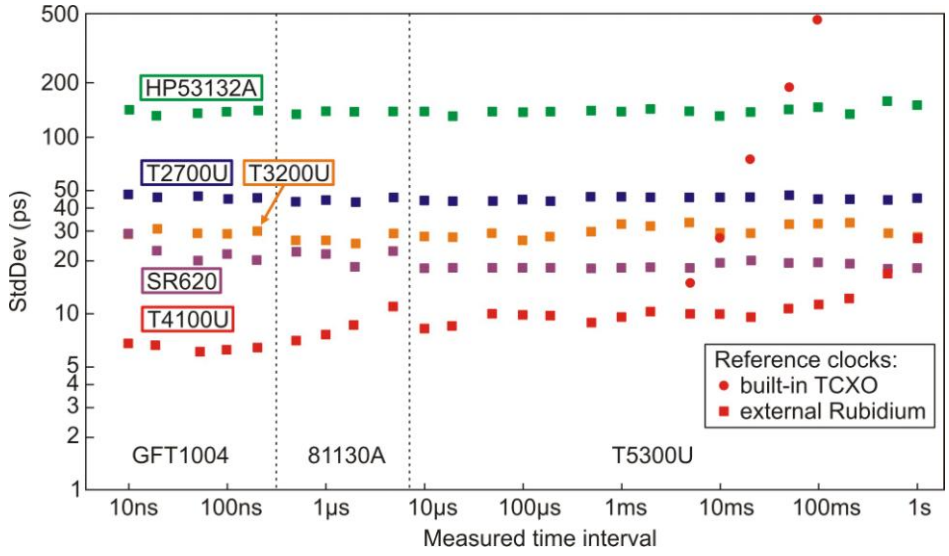

Figure 6. Comparison of the precision (standard measurement uncertainty) of succesisive versions of our time counter and selected commercial time counters.

The time counters with a single (T2700U) and double (T3200U) time coding lines in SIS have measurement precision at levels of 50 ps and 35 ps, respectively. Taken for comparison the very popular laboratory standard SR620 offers the precision not worse than 25 ps. The precision of the time counter presented in this article (T4100U) is below 10 ps within the range up to 2 ms if the on-board TCXO is used as a reference clock, and up to 100 ms if the rubidium frequency standard FS725 (*SRS*) [27] is used. For time intervals longer than about 100 ms the observed measurement uncertainty of the counter becomes more influenced by the short-term instability of the reference clock of time interval generator (T5300U).

VI. CONCLUSIONS

So far, the time interval counters with picoseconds of precision were built as ASICs or with the use of discrete elements and analog conversion methods. The use of multiple coding lines for T/D conversion allows reaching such a high precision in time counters implemented in general-purpose, cheap programmable devices. Then the FPGA-based integrated time counters can be used to develop versatile, portable measurement instruments supplied and controlled via USB ports of ordinary desktop or mobile computers. Reprogrammable FPGA technology allows easy modification of their functionality to meet user requirements.

ACKNOWLEDGEMENTS

This work was supported by the Polish National Science Centre under contract no. DEC-2011/01/B/ST7/03278.

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