PHASE NOISE MODEL FOR AN ARRAY OF COMBINED SOURCES USING DIRECT DIGITAL SYNTHESIS (DDS)

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Abstract

A direct digital synthesizer (DDS) offers the fastest frequency jumping and the finest frequency tuning resolution of any technology available today in a completely controlled digital environment. In this work, we present and experimentally verify a concise DDS phase noise model which includes the possibility of combining the outputs of an array of N parallel DDSs for improved total phase noise performance. The DDS phase noise, L_{DDS}, consists of contributions from the DDS source clock L_{Ck}, the internal DDS flicker noise $L_{1/f}$, and the DDS's digital-to-analog converter (DAC) noise floor L_{Floor}, according to the following equation:

$$L_{DDS} = \frac{1}{2} r^2 \cdot L_{Ck} + \frac{1}{N}\left(\frac{r}{r_R}\right)^2 \cdot L_{1/f} + \frac{1}{N}\kappa(r) \cdot L_{Floor}.$$

Here, r is the ratio of the DDS output frequency to its source clock frequency, and r_R is the ratio of a particular reference output frequency to the source clock frequency. Though partial versions of this model exist in the literature, the above equation provides a more concise and usable description of DDS-array phase noise than those previously offered.

We made measurements on a set of up to eight parallel DDSs to experimentally examine and validate the various relationships of the model. To verify the DDS source clock phase noise contributions, we corrupted a low-noise clock with amplified broadband noise so that the clock noise dominated L_{DDS}. We validated the contribution from the naturally dominant flicker noise by comparing it to measurements made at a reference output frequency, verifying the expected frequency scaling. We found the floor noise to be negligible at the offset frequencies measured, up to several megahertz. Combining multiple DDSs yielded phase noise improvements in flicker noise contribution, but, as predicted, it had no effect when the phase noise was dominated by the clock contribution. The experimental validation of our phase noise model suggests its utility in enabling more accurate predictions and analyses of systems incorporating DDS frequency generation.

INTRODUCTION

The general topology of a direct digital synthesizer (DDS) is shown in Figure 1 to consist of four primary elements: a phase accumulator, a phase-to-amplitude converter, a digital-to-analog converter (DAC), and

a driving clock. At each clock cycle, the phase accumulator, which is effectively a counter, is incremented by *M*, the frequency tuning word. The phase stored by this accumulator is converted to a corresponding sine-wave amplitude by the phase-to-amplitude converter, often through the use of a simple sine look-up table. The digital amplitude value from this look-up table is then passed to the DAC and transformed to an analog output. As the phase is increased by *M* on subsequent clock cycles, the amplitude output steps through the sine look-up table, generating the desired analog sinusoidal signal. Though the amplitude of this generated signal is set by the characteristics of the phase-to-amplitude converter and the DAC, the output signal frequency can be tuned by varying the frequency tuning word, *M*. A larger *M* results in the phase accumulator moving through the period of the sine look-up table more quickly, producing a higher-frequency sinusoid at the output, while a smaller *M* moves the accumulator through the sine look-up table more slowly, yielding a lower frequency output sine wave.

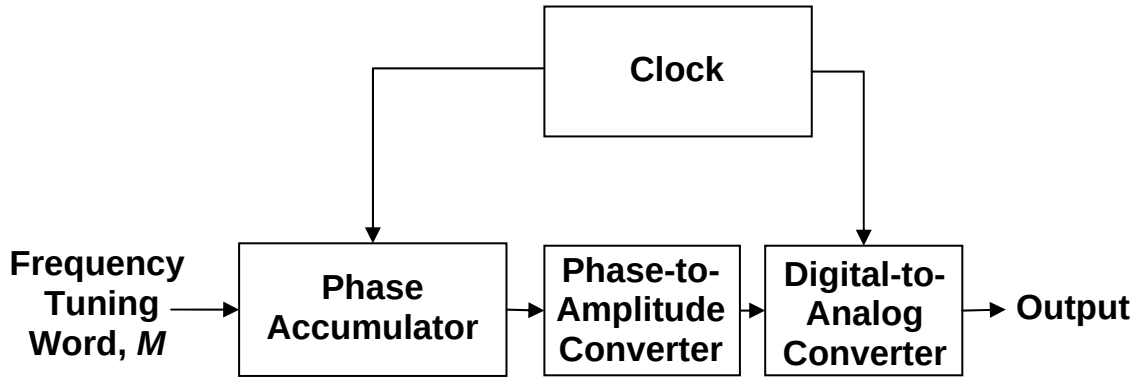


Figure 1. Basic structure of a generic direct digital synthesizer.

The ability to quickly and directly modify the frequency tuning word, *M*, enables the DDS topology to offer the fastest frequency jumping and the finest frequency tuning resolution of any technology available today in a completely controlled digital environment. As a result, DDSs have found wide application in fields including communications and test and measurement equipment. In this work, we offer and experimentally verify a concise DDS phase noise model which takes into account the possibility of combining the output of an array of *N* identical DDSs if lower phase noise than that produced by a single DDS were desired **[1]**.

DDS ARRAY PHASE NOISE MODEL

We present the following phase noise model for the combined output of an array of *N* identical DDSs, culled from various reports in the literature **[1-5]**:

$$L_{DDS}(f,r) = \frac{1}{2} r^2 \cdot L_{Ck}(f) + \frac{1}{N}\left(\frac{r}{r_R}\right)^2 \cdot L_{1/f}(f, r_R) + \frac{1}{N}\kappa(r) \cdot L_{Floor}\,. \qquad (1)$$

In this model, the DDS phase noise, L_{DDS}, consists of contributions from the DDS source clock L_{Ck}, the internal DDS flicker noise $L_{1/f}$, and the DDS's DAC noise floor L_{Floor}. r is the ratio of the DDS output frequency to its source clock frequency, and r_R is the ratio of a particular reference output frequency to the source clock frequency:

$$r = \frac{f_{out}}{f_{Ck}} \qquad \text{and} \qquad r_R = \frac{f_{out,R}}{f_{Ck,R}}$$

The source clock contributes a component equal to a scaled version of its own inherent phase noise **[5]**, while the flicker and floor components are derived from the DDS circuitry itself and are referenced to a particular frequency defined by r_R. Knowledge of the flicker noise contribution at any given output and clock frequencies allows determination of the flicker noise for any other DDS output frequency by scaling by the appropriate r and r_R terms **[2]**. The DAC contributes to the overall white noise floor with a mild frequency-dependence, $\kappa(r)$, which is a weak function of r and is specific to a particular DAC **[3]**. By combining N identical DDSs in parallel, the uncorrelated flicker noise and noise floor components are reduced by a factor of N, while the common clock phase noise component is unchanged **[1]**.

EXPERIMENTAL MODEL VERIFICATION

EXPERIMENTAL APPROACH

In order to experimentally verify the phase noise model of equation (1), we made use of a test bed consisting of eight custom-designed DDSs. Each synthesizer was based upon a 14-bit DAC (Analog Devices 9736) controlled by an FPGA (Xilinx Virtex 4). The frequency tuning word of the DDS was 32 bits and each look-up table (LUT) word was 17 bits. A single 100-MHz low-phase noise oven-controlled crystal oscillator (OCXO) was multiplied to 800 MHz to drive the DDS array, while 7th-order reconstruction filters limited the maximum output frequency of each DDS to 320 MHz. We combined two, four, or eight DDS channels using microwave power combiners after aligning the individual channel phases. The experimental arrangement is shown schematically in Figure 2.

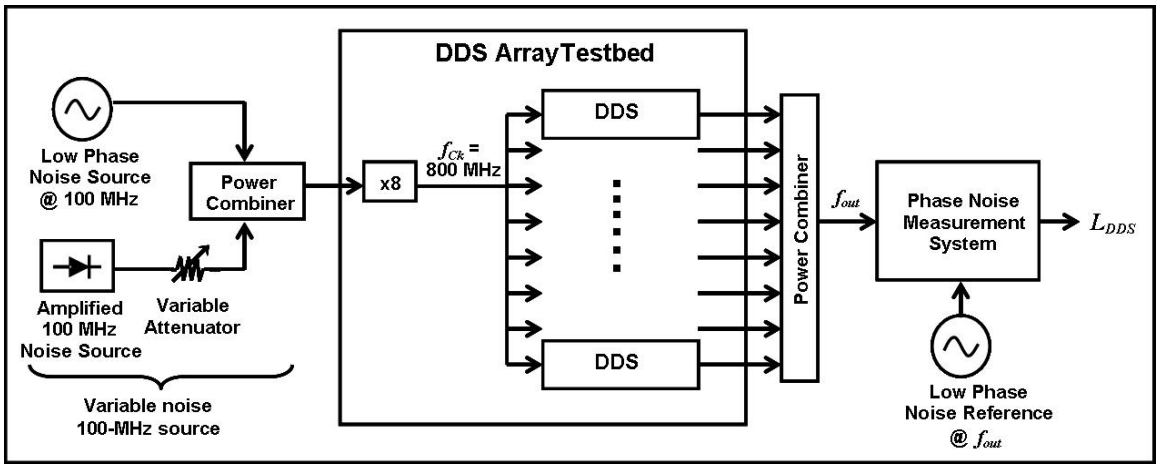


Figure 2. Experimental setup used to validate the model of equation (1).

Phase noise measurements were made using a phase detection technique in which the desired signal is mixed in quadrature with a reference oscillator of the same frequency, but possessing much lower phase

noise **[6]**. After low pass filtering and amplification, the mixer output was calibrated to provide a measure of the single-sided phase noise, L, of the desired signal. For the measurements presented in this report, we used a variety of very low phase noise OCXOs as reference sources.

SOURCE CLOCK CONTRIBUTION

In order to more easily distinguish the individual contributions of clock, flicker, and floor noise to the overall phase noise of the DDS output, we examined separate cases where a single contributor dominates the DDS phase noise. Considering first the case where the clock phase noise dominates L_{DDS}, equation (1) suggests that, when

$$L_{Ck} >> L_{1/f} \text{ and } L_{Ck} >> L_{floor}$$

then

$$L_{DDS} \approx \frac{1}{2} r^2 \cdot L_{Ck} . \tag{2}$$

Thus, when a low-stability clock is used, the DDS output phase noise should represent a scaled version of the clock phase noise, with the scaling factor related to the ratio of the output and clock frequencies. Taking advantage of the above simplification, we set out first to verify the relation

$$L_{DDS} \propto L_{Ck} \tag{3}$$

In early designs, the phase noise of most DDSs was dominated by the clock oscillator phase noise, making contributions from the other components effectively negligible. Oscillator performance has improved significantly, though, and the phase noise characteristics of current DDSs are generally dominated by internal flicker noise contributions, masking the effect of the clock noise. Our DDS array test bed is normally driven by a low-noise 100 MHz OCXO. This 100-MHz source is multiplied by a factor of n = 8 up to the 800-MHz clock signal required to drive the DDSs, as shown in Figure 2. As a result, the 800-MHz clock possesses phase noise higher than that of the 100-MHz OCXO by a factor of n^2 = 64, or 18 dB **[7]**. The 100-MHz OCXO phase noise is specified to be -174 dBc/Hz at 10 kHz offset, and even with the 18 dB increase, the DDS DAC flicker noise dominates the phase noise of our units, preventing us from observing the clock noise dependence of L_{DDS}. To overcome this limitation, we constructed a "noisy clock" by coupling our low-noise 100-MHz OCXO to an amplified broadband noise source with a 100 MHz 3 dB bandwidth. By varying the attenuation on the noise source, the magnitude of the clock phase noise after frequency multiplication, L_{Ck},, could be arbitrarily tuned and made to be much larger than the DDS flicker phase noise contribution.

We first held f_{out} and f_{Ck} (see Figure 2) constant at 80 and 800 MHz, respectively, and varied L_{Ck} by adjusting the attenuation of the broadband noise source, as described above. As no improvement in phase noise is expected from combining multiple DDS units, phase noise measurements were taken on a single DDS output. As Figure 3 shows, increasing the attenuation of L_{Ck} in increments of 10 dB decreased L_{DDS} by the same amounts, thus verifying relationship (3). The sloped portions of the spectra at low offset frequencies (f_{offset} < ~10 kHz) and high levels of clock noise attenuation (attenuation ≥ 20 dB) indicate regimes in which $L_{1/f}$ rather than L_{Ck} begins to dominate DDS noise. As a result, further decreases in the clock noise do not affect the measured L_{DDS} in these regions. The discontinuity seen at the 10 kHz offset frequency is a reproducible artifact generated by the phase noise measurement system.

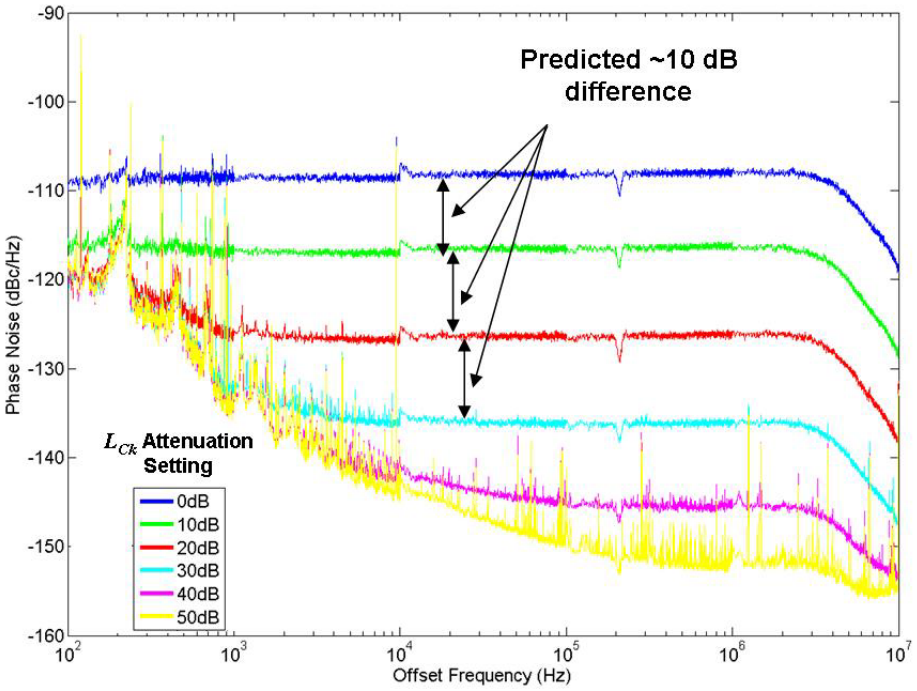
Figure 4 compares the same DDS output phase noise data for the cases when clock noise is most dominant – the 0 dB, 10 dB, and 20 dB attenuation levels – against the measured phase noise of the noisy

100-MHz source used in those instances. As mentioned above, the 100-MHz source is first multiplied to f_{Ck} = 800 MHz, resulting in an 18 dB phase noise increase:

$$L_{Ck}(f) = 8^2 \cdot L_{100\,MHz}(f)$$
$$L_{Ck,dB}(f) = L_{100\,MHz,dB}(f) + 18dB \quad (4)$$

with L_{dB} defined as L_{dB} = 10 log (L). Next, that 800-MHz signal is used to clock the DDS. For an 80 MHz DDS output, the model of equation (2) predicts a DDS phase noise 23 dB lower than that of the 800-MHz clock:

$$L_{DDS,80MHz}(f) = \frac{1}{2}\left(\frac{80}{800}\right)^2 \cdot L_{Ck}(f)$$



$$L_{DDS,80MHz,dB}(f) = L_{Ck,dB}(f) - 23dB\,. \quad (5)$$

Figure 3. Phase noise of 80 MHz DDS outputs generated using the noisy clock configuration of Figure 2 for various noise attenuation settings. The highest levels of clock phase noise are present for the "0 dB" attenuation case, while the lowest levels of clock phase noise are present in the "50 dB" attenuation case.

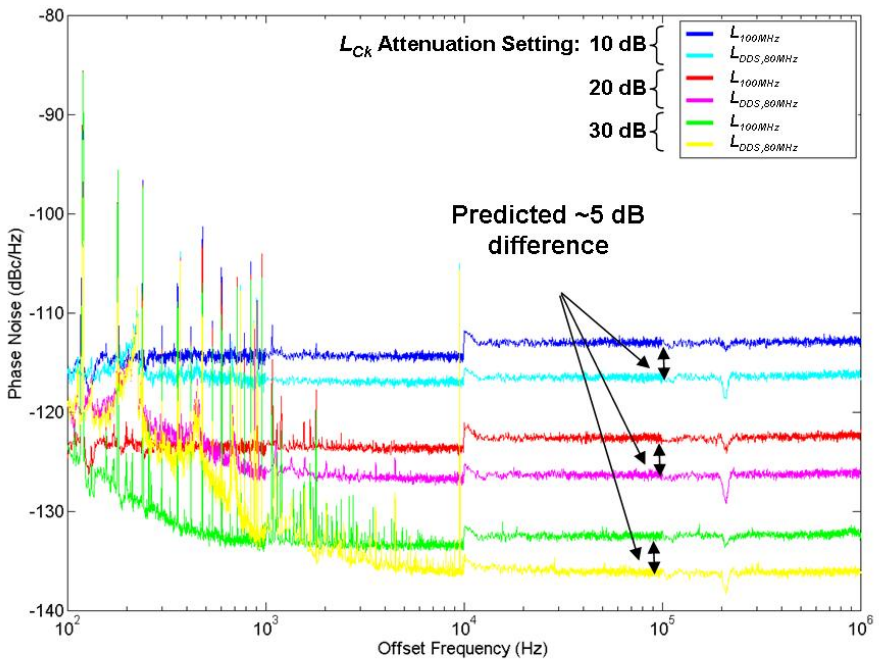


Figure 4. Phase noise of 80 MHz DDS outputs generated using the noisy clock configuration of Figure 2 plotted alongside the corresponding variable noise 100 MHz source phase noise. For all three cases, the 80 MHz DDS outputs exhibit phase noise ~5 dB less than that of the 100-MHz source.

As a result, the 80 MHz DDS output signal is expected to have phase noise 5 dB lower than that of the original 100-MHz source:

$$L_{DDS,80MHz,dB}(f) = L_{100MHz,dB} + 18dB - 23dB = L_{100MHz,dB} - 5dB\,. \tag{6}$$

This predicted 5 dB decrease in phase noise is demonstrated clearly in Figure 4 for all three source noise levels where L_{Ck} dominates DDS phase noise.

Further validation is shown in Figure 5 for the case where the output frequency of the DDS is set to 100 MHz. Using the same reasoning expressed in equations (4) through (6), but instead substituting 100 MHz for f_{out}, the expected 100 MHz DDS phase noise output is 3 dB lower than the variable noise 100-MHz source in regions where the source dominates. This decrease is clearly shown for the cases in Figure 5, where the DDS phase noise is measured to be approximately 2 to 3 dB lower than the corresponding 100 MHz source noise.

Finally, in order to further verify the frequency (f_{out}) dependence of the clock noise component in our DDS phase noise model, the DDS output frequency was increased to 200 MHz and the resultant phase noise compared to that measured for the f_{out} = 100 MHz case. According to the model, the ratio of the phase noise at f_{out}= 200 MHz to that at f_{out}= 100 MHz is:

$$\frac{L_{DDS,200MHz}}{L_{DDS,100MHz}} = \frac{f_{out,200MHz}^2}{f_{out,100MHz}^2} = \frac{200^2}{100^2} = \frac{4}{1} \approx 6dB\,.$$

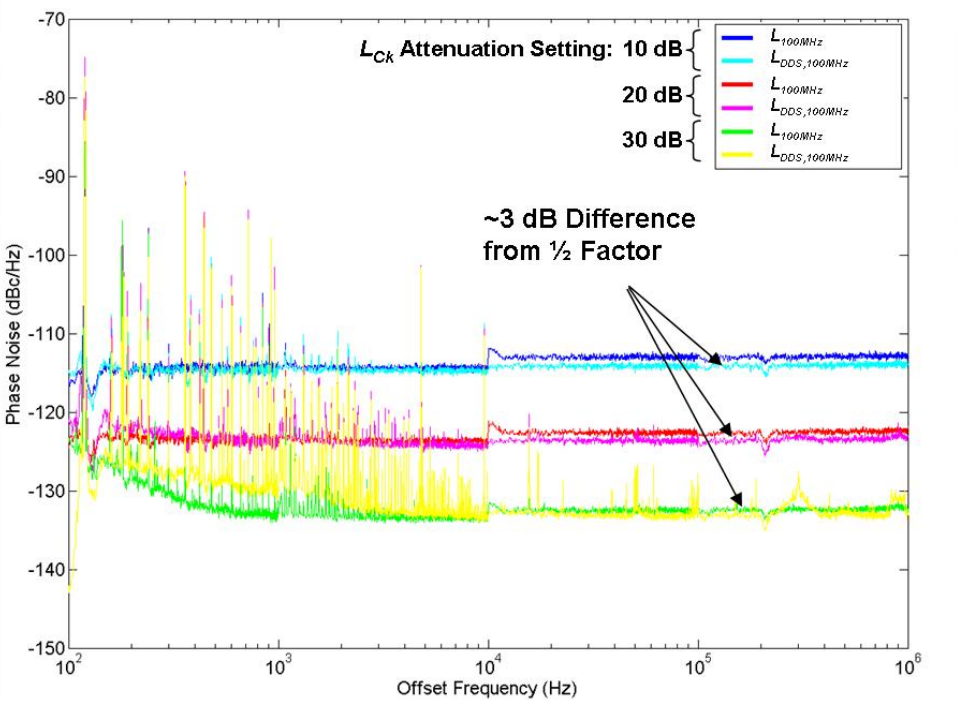


Figure 5. Phase noise of 100 MHz DDS outputs generated using the noisy clock configuration of Figure 2 plotted alongside the corresponding variable noise 100 MHz source phase noise. For all three cases, the 100 MHz DDS outputs exhibit phase noise ~3 dB less than that of the 100-MHz source.

The expected 6 dB difference is clearly seen in Figure 6 for three different levels of clock noise. Taken together, the results presented in Figures 3-6 validate the L_{Ck} dependence of DDS output phase noise *for a single DDS unit* captured by our model.

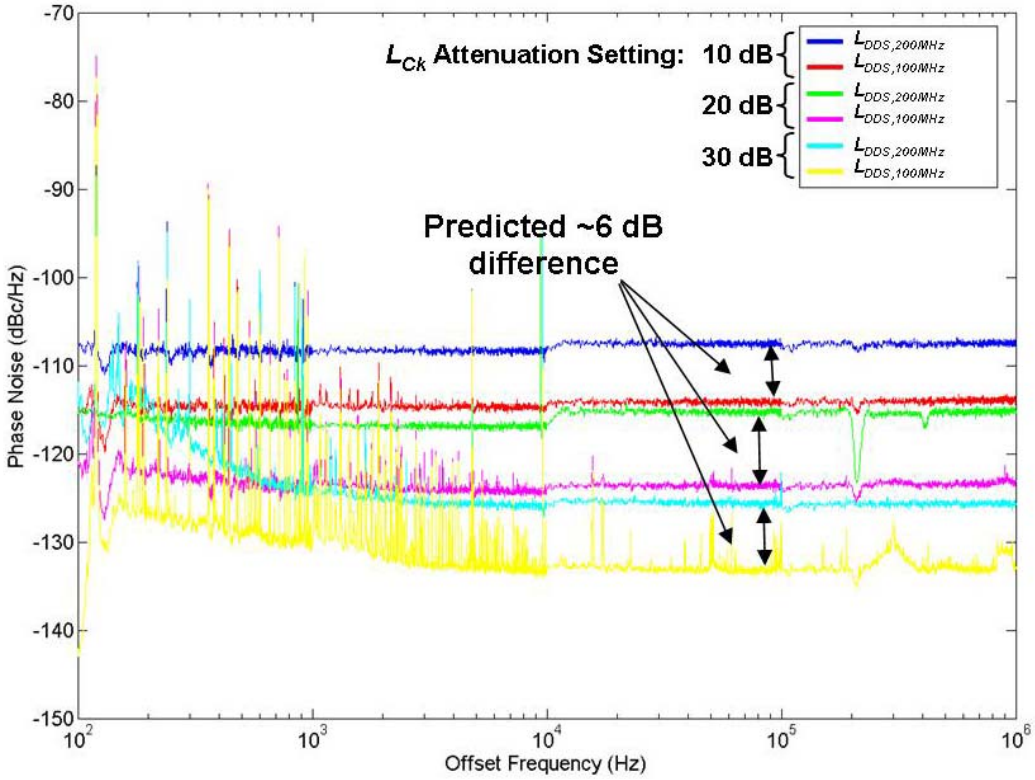


Figure 6. Comparison of the phase noise of the DDS outputs at 200 and 100 MHz. The 6 dB difference expected due to the *r* scaling factor is evident for all three levels of clock noise utilized.

In the case of multiple DDS units, if the DDS bank is driven by a common clock, the clock-noise contributions of each DDS unit are fully correlated and no improvement in overall output phase noise is achieved by increasing the number of DDSs. As a result, the clock-dominated DDS phase noise measured for multiple combined outputs should be the same as that measured for a single DDS output. In order to confirm this, we measured the phase noise of one, two, and four phase-aligned and combined channels at f_{out} = 100 MHz. Appropriate amplification and attenuation was used so as to normalize the input power to the phase noise measurement system to approximately 10 dBm in all cases for optimum phase noise measurement system performance. The results of these measurements are plotted in Figure 7 for two levels of source clock phase noise. As the figure shows, increasing the number of DDSs does not appreciably alter the DDS phase noise in regions dominated by the clock contribution.

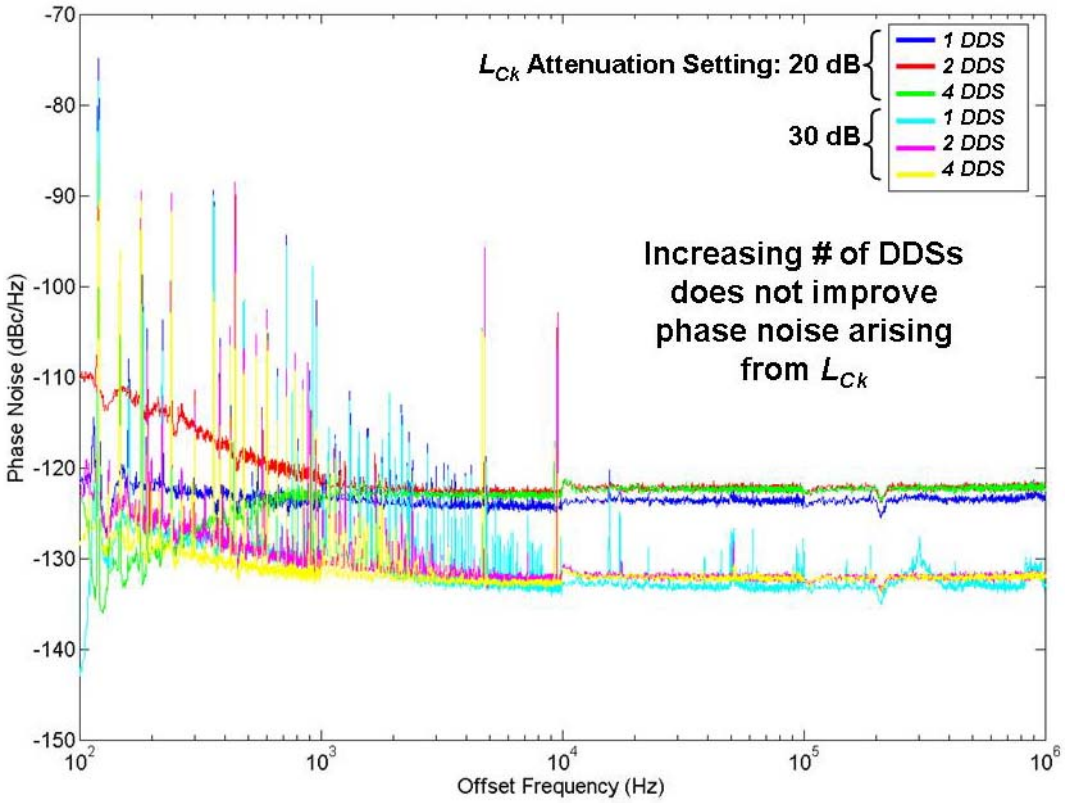


Figure 7. Comparison of the phase noise output of the DDS for various numbers of phase-aligned and combined channels generated using two different levels of attenuation of 100 MHz source phase noise. For a given clock phase noise, increasing the number of DDSs in parallel does not improve the combined output phase noise, because the common clock noise dominates L_{DDS}, as predicted by equation (2).

FLICKER NOISE CONTRIBUTION

We next consider the case where flicker noise from the DAC dominates the phase noise of the DDS array, that is

$$L_{1/f} >> L_{Ck} \text{ and } L_{1/f} >> L_{Floor}.$$

Equation (1) becomes

$$L_{DDS} \approx \frac{1}{N}\left(\frac{r}{r_R}\right)^2 \cdot L_{1/f} \tag{7}$$

where $L_{1/f}$ is the flicker noise measured at the reference frequency ratio r_R. Thus, for the case when DAC flicker noise dominates, the DDS output noise will be directly proportional to $L_{1/f}$ with a scaling factor dependent on the number of DDSs present and the output and clock frequencies. Taking advantage of this simplification, we first verified the phase noise improvement expected by implementing an array of parallel DDSs, specifically:

$$L_{DDS} \propto \frac{1}{N} L_{1/f} \ . \tag{8}$$

We replaced our variable noise source with the original low noise 100-MHz OCXO and measured the phase noise of N = 1, 2, 4, and 8 phase-aligned and combined channels at f_{out} = 100 MHz. As Figure 8 shows, each doubling of the number of channels decreased the phase noise by 3 dB, in accordance with the expected 1/N scaling.

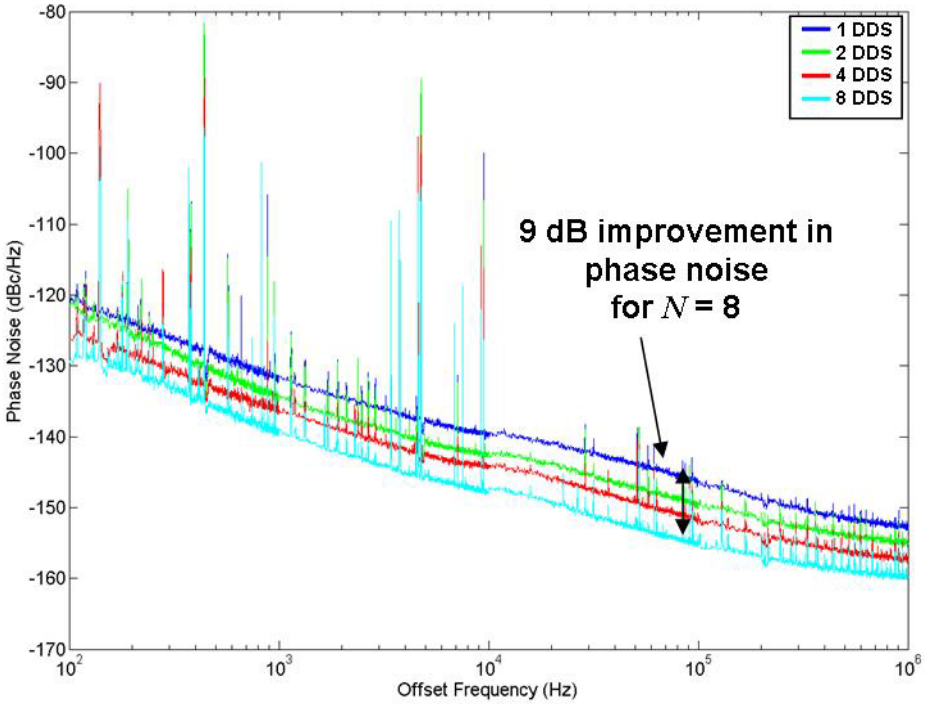


Figure 8. Comparison of phase noise output of the DDS at f_{out}= 100 MHz for N = 1, 2, 4, and 8 phase-aligned and combined channels. The expected 1/N decrease in phase noise for N-DDS arrays is clearly evidenced.

The frequency dependent scaling of the flicker noise term can be verified by comparing the DDS phase noise at different output frequencies. According to equation (7), for a given flicker-dominated DDS-array, the phase noise characteristics L_{DDS1} and L_{DDS2} recorded at output frequencies f_{out1} and f_{out2}, respectively, are related by:

$$L_{DDS1} = \left(\frac{f_{out1}}{f_{out2}} \right)^2 \cdot L_{DDS2} \tag{9}$$

which assumes a common clock frequency for both measurements. Selecting frequencies f_{out1} = 80 MHz and f_{out2} = 100 MHz yields

$$L_{DDS,80MHz} = \left(\frac{80}{100} \right)^2 \cdot L_{DDS,100MHz}$$

$$L_{DDS,80MHz,dB} = L_{DDS,100MHz,dB} - 2dB \tag{10}$$

for any N. Figure 9 shows $L_{DDS,80\ MHz,dB}$ plotted alongside ($L_{DDS,100\ MHz,dB}$ -2dB) for varying values of N. The phase noise curves measured at 80 MHz overlap nearly exactly with the shifted 100 MHz phase noise curves, validating the predicted frequency scaling of the flicker noise contribution for all combinations of DDSs measured. Deviations in the measured phase noise at low offset frequencies (f_{offset} <1 kHz) likely arise from differences in the phase-lock loops used in the phase noise measurement setup for the 80-MHz and 100-MHz oscillators.

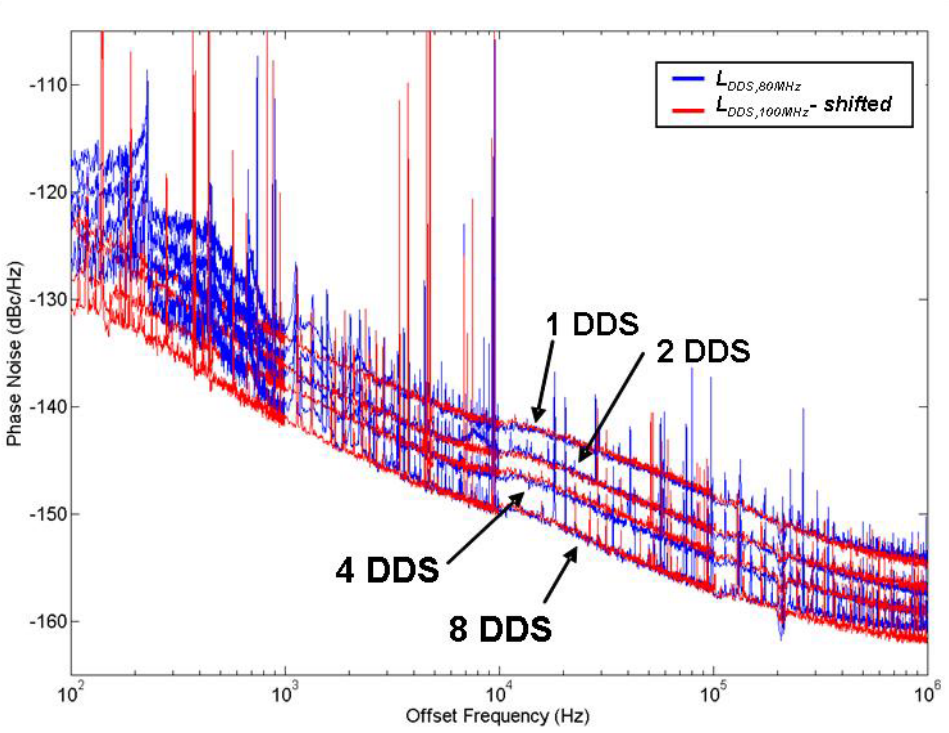


Figure 9. Plot of phase noise of DDS output at 80 MHz (blue curves) and DDS output at 100 MHz shifted downward by 2 dB (red curves). The two sets of measurements overlap very well, confirming the expected frequency scaling of the $L_{1/f}$ contribution to DDS phase noise.

We also compared phase noise measurements taken at f_{out1}=200 MHz to the reference measurements at f_{out2} = 100 MHz. According to equation (9), the phase noise relationship between these two frequencies is predicted to be

$$L_{DDS,200MHz} = \left(\frac{200}{100}\right)^2 \cdot L_{DDS,100MHz}$$
$$L_{DDS,200MHz,dB} = L_{DDS,100MHz,dB} + 6dB\,. \tag{11}$$

Similar to Figure 9, Figure 10 plots the measured DDS phase noise at f_{out1}= 200 MHz alongside ($L_{DDS,100MHz,dB}$ + 6 dB). While the overlap is not quite as good as that seen for the 100-MHz and 80-MHz outputs, the measured values still are within ~ 2-3 dB of the values predicted by frequency scaling, further confirming the validity of our proposed model. The source of the increased deviation is currently

unknown, but may be related to the stability of the 200 MHz reference oscillator or the phase-lock technique implemented in the measurement system.

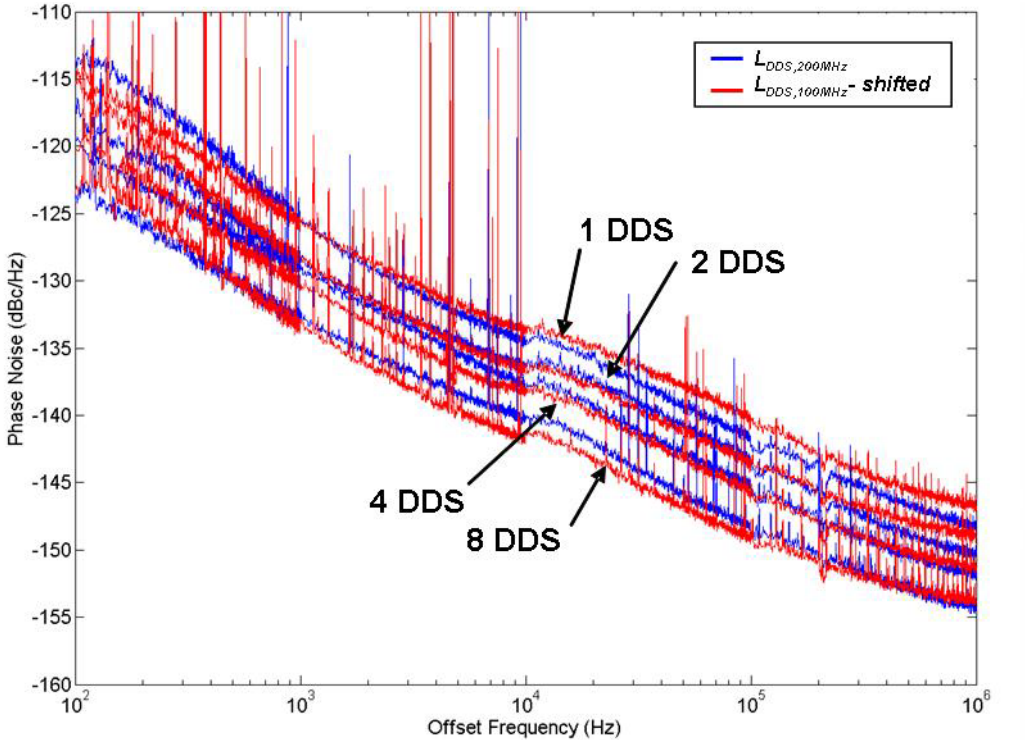


Figure 10. Plot of phase noise of DDS output at 200 MHz (blue curves) and DDS output at 100 MHz shifted upward by 6 dB (red curves).

FLOOR NOISE CONTRIBUTION

In our DDS array, the DAC floor noise contribution was negligible at the offset frequencies up to 10 MHz measured, and, unlike the clock noise, it could not easily be artificially increased to dominate the flicker noise. As a result, we were unable to verify its contribution to the overall DDS noise with our present measurement capabilities. However, L_{floor}, which is derived from the white noise of the DAC, is expected to be uncorrelated among multiple DDS units, and, like the uncorrelated flicker contribution, we expect the noise floor contribution to L_{DDS} to scale as $1/N$ in a DDS array **[1]**. Future work to increase the maximum offset frequency of the phase noise measurement system may allow direct measurement of the floor noise and verification of its inclusion in our phase noise model.

CONCLUSION

In summary, we have presented a concise, usable model for the phase noise of an N-DDS parallel array. Using a custom-designed DDS test bed, we have experimentally verified the expected dependence and frequency scaling of the output phase noise on clock and DAC flicker noise contributions. Furthermore, we have demonstrated that combining multiple DDSs yields the predicted $1/N$ phase noise improvement in flicker noise contribution, but has no effect when the noise is dominated by the common-clock contribution. The experimental validation of our phase noise model suggests its utility in the design and

analysis of systems requiring DDS waveform generation and confirms the effectiveness of parallel DDS arrays for high-performance agile frequency synthesis.

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