A Review of Time Jitter and Digital Systems

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Abstract— **Time jitter is an important parameter for determining the performance of digital systems. This paper reviews how time jitter impacts the performance of digital systems. For the purposes of later discussions, digital systems are broken down into three major categories: synchronous data transfer, asynchronous data transfer, and digital sampling systems. A statistical framework is first developed for treating time jitter. This framework explicitly deals with issues of bandwidth and noise processes with $1/f^n$ spectra. It is shown that various forms of the standard variance of time jitter are convergent in the presence of $1/f^n$ noise, if one explicitly considers the properties of the system phase response function for each of these categories. It is also shown that standard variances are preferred over 2nd difference variances in dealing with digital performance issues such as bit errors, because standard variances can be directly related to the total time error (jitter plus skew). Detailed discussions of how time jitter impacts the enumerated categories of digital systems are then presented. In synchronous data transfer systems, it is shown that time jitter causes hard bit errors, that only the white noise components of clock oscillator and gate noise make appreciable contributions to the time jitter, and that aliasing of this white noise is a major issue. In asynchronous systems, it is shown that time jitter can also cause soft errors or bit error rate degradation and that there is an additional time jitter term due to relative master clock-local clock oscillator jitter, whose value is determined by $1/f^n$ oscillator noise as well as the white noise. Finally, for digital sampling in analog-to-digital and digital-to-analog converters, it is shown that noise power or multiplicative decorrelation noise generated by sampling clock jitter is a major limitation on the bit resolution (effective number of bits) of these devices.**

I. INTRODUCTION

Time jitter is an important parameter for determining the performance of digital systems. This paper reviews how time jitter impacts the performance of digital systems. First, an overview of time jitter and digital systems is presented. In this overview, three types of digital systems useful for categorizing the various impacts of time jitter are described, and definitions of time error are discussed. Next, a statistical framework for later discussions is presented. Finally, using this framework, a detailed discussion of the impact of time jitter on system performance for each category of digital system is given.

Historically, the digital community has dealt with time jitter using standard variances as the measure of jitter [1-9]. Such treatments use the tools of stationary statistics and often do not explicitly deal with issues of bandwidth and non-stationary noise; that is, noise processes with $1/f^n$ spectra [10-18]. Now, with digital systems achieving clock speeds in the multi-gigahertz region and time jitter requirements reaching the sub-ps level, it is important to treat such bandwidth and $1/f^n$ spectra issues explicitly. The precise time community, on the other hand, has historically dealt with both these issues by using 2nd difference variances to avoid convergence problems associated with the standard variance in the presence of $1/f^n$ noise [10-18]. However, it will be shown that these 2nd difference measures of jitter are not easily connected to digital performance parameters. Thus, statistical treatment of time jitter presented here will attempt to meld both approaches. It will use the standard variance as the measure of time jitter, explicitly treating issues of bandwidth and $1/f^n$ spectra, and it will show that the standard variance converges for digital systems because of the unique properties of these systems.

II. AN OVERVIEW OF TIME JITTER AND DIGITAL SYSTEMS

Categories of Digital Systems. Figure 1 shows a (somewhat overlapping) categorization of digital systems useful for discussing the various impacts of time jitter. These categories are as follows:

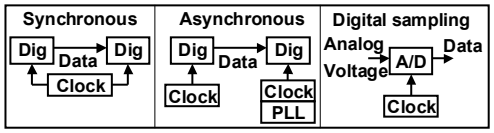

Figure 1. Categorization digital systems useful for discussing time jitter.

(1) Synchronous data transfer systems distribute a single hard-line clock between all subsystems along with the data. Clock commonality cancels most direct effects from the clock oscillator and jitter comes from the logic gates themselves. Here time jitter can generate hard bit errors or direct bit errors without any other factors being involved.

(2) Asynchronous data transfer systems distribute only data between subsystems. Each sub-system has its own local clock oscillator (LO) that is synchronized to the master unit clock oscillator (MO) using a phased locked loop (PLL). Digital communications systems are in this category [19]. In asynchronous systems, there is additional relative MO-LO time jitter along with the synchronous gate jitter. This additional jitter can create soft bit errors or bit error rate (BER) degradation, which is the term used for an increase in the BER that only occurs when thermal noise is also present [19].

(3) Digital sampling systems include analog-to-digital converters (A/D), digital-to-analog converters (D/A), and decision circuits in communications systems [19]. In this category, sampling clock jitter degrades the integrity of the sampled signal [20-23]. In A/D's and D/A's, this generates noise power, which degrades the effective number of bits

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(ENOB) of these devices [20-23]. In communications systems, sampling clock jitter in symbol (or bit) decision circuits--which are specialized A/D converters that convert an analog signal into a digital data stream--generates soft bit errors [19].

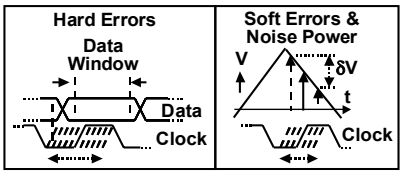


Figure 2. Time jitter and digital system degradation.

Types of Degradation Caused by Time Jitter. Figure 2 shows how time jitter can degrade the performance of digital systems. The left hand figure shows how hard bit errors are created. For data to be transferred properly from digital sub-system to sub-system at clock transition epochs, the clock epoch must fall within a data-timing window where data is settled into the correct state. A hard error thus occurs when the time jitter causes the clock transition epoch to fall outside of this window.

The right hand figure shows how both soft errors and noise power are generated in digital sampling. In symbol decision circuits, an analog signal is turned into a stream of digital symbols by comparing the sampled signal to one or more decision thresholds at the sampling clock epochs [19]. Sampling clock jitter causes variations in the sampled signal level. These variations create a greater potential for bit errors in the presence of thermal noise. This produces a higher BER for a given input SNR than there would be without the variation [19].

In A/D and D/A converters, time jitter induced random variations in the sampled signal generate multiplicative decorrelation noise from the coherent signal that is called noise power [20-23]. Sampling errors caused by this noise power add to that produced by the quantization errors of the device. The net effect of this is to reduce the effective number of bits (ENOB) of the device to something less than is given by the number of quantization bits.

Time jitter can be deterministic, such as that generated by spurs, or random, such as that generated by true noise processes. Random noise can be colored or non-stationary. In the following sections, we will mainly discuss random jitter. However, the theory presented also applies to deterministic jitter.

Definitions of Time Error. Before plunging into the statistics of time jitter, it is important clarify what is meant by time or timing error in digital applications and how time error is specified. As shown in Figure 3 in the left hand figure, for data transfer applications, the time difference between the data symbol centers and the clock edges is the time error parameter. As shown in the right hand figure, for digital sampling applications, the time difference between the clock driving the analog signal and sampling clock epochs is the time error parameter.

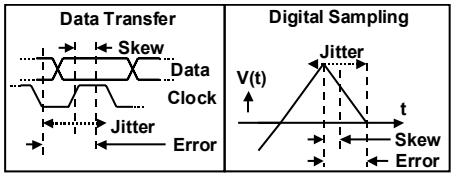


Figure 3. Timing error is separated into skew and jitter.

As also shown in Figure 3, the total time error is broken down into skew and jitter terms for both types of error. The skew or average error, is generally further partitioned into fixed, slowly varying, and environmental terms. The most often used measure of skew is the arithmetic mean of the time error over some time-period that may or may not be specified. The jitter is considered the high frequency variation and is specified by the root mean square (RMS), peak, or peak-to-peak value. The RMS value, which will be used here, is generally interpreted as an N-sample unbiased standard deviation of the time error, and often the system bandwidth properties are not explicitly defined [1-8].

It is important to note that bit errors are tied to the total error, not to either the jitter or skew alone. Thus, standard variances are preferred as the jitter measure in bit error applications because these variances directly reference the skew and allow the total error to be expressed simply as the sum of the jitter and the skew. Sometimes 2^{nd} difference variances based on Allan variances are used to define the time jitter [9, 17, 18], but these variances have the weakness of not directly referencing the skew. More will be said about this in the next section.

For digital sampling applications, reference to the skew is important for soft errors. For noise power, the skew reference is not important, but it is important for sampling accuracy considerations.

III. A STATISTICAL FRAMEWORK FOR DISCUSSING TIME JITTER

In the following section, we will develop a statistical framework for later discussions of time jitter and digital systems, and the framework developed will explicitly treat issues of bandwidth and $1/f^n$ noise. It will utilize various forms of the standard variance as the measure of time jitter, rather than 2^{nd} difference variances, because of their direct connection to the total time error. It will be shown that these standard variances converge in the presence of $1/f^n$ noise because of the properties of the system phase response function.

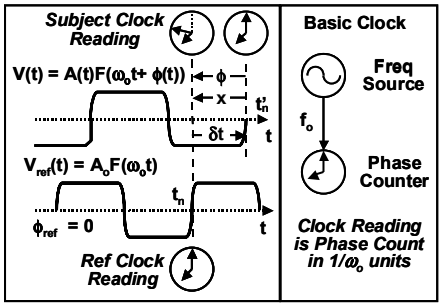


Figure 4. Time error and clock reading error.

Time Error Variables. As shown in Figure 4, there are two variables for time error that are in use in the literature [1-18]: $\delta t(t_n)$ the time or zero crossing error, and $x(t_n)$ the clock reading or normalized phase error. To understand the difference between these two variables, consider the following.

Let the voltage of a subject clock be given by

$$V(t) = A(t)F(\omega_0 t + \phi(t)) \tag{1}$$

where F(x) is a periodic function with a period of 2π, A(t) is the amplitude, ω_o is the nominal angular clock frequency ($f_o = \omega_o/(2\pi)$ is the nominal clock frequency), and $\phi(t)$ is the phase error. Thus, V(t) is a nearly periodic function whose positive going clock edges t'_n are used to define a sequence of clock epochs. These edges t'_n can be compared with equivalent edges t_n of a reference clock to define the time error

$$\delta t(t_n) = t'_n - t_n \cong -\phi(t_n)/\omega_o \tag{2}$$

where

$$t_n = 2\pi n/\omega_o = n/f_o \tag{3}$$

and where the approximate expression for $\delta t(t_n)$ given by $-\phi(t_n)/\omega_o$ can be derived from (1).

As is also shown in Figure 4, a basic clock can be defined as a frequency source with voltage V(t) and a phase counter whose reading is in units of ω_o^{-1}. This normalized phase counter reading is equivalent to the reading of a clock face driven by V(t). It can be shown using (1) that x(t) the clock reading error between the subject and references clock faces is given by

$$x(t) = \phi(t)/\omega_o \tag{4}$$

Note that x(t) is defined as a continuous variable through $\phi(t)$.

x(t) is considered the preferred variable because its derivative is just the fractional frequency error y

$$y \equiv (d\phi/dt)/\omega_o = dx/dt = -d(\delta t)/dt \tag{5}$$

whereas, the derivative of δt is the negative of y. For this reason, x(t) will be used as the time error variable for the rest of this paper.

The Variance of Regularly Spaced Samples. Regularly spaced samples of x are assumed to be given by

$$x_n = \int dt\, x(t) h_s(n\tau - t) \tag{6}$$

where $h_s(t)$ is a linear time-domain phase response function describing the filtering properties of the system of interest, and τ is the uniform sampling interval. This explicit use of $h_s(t)$ will become very important later for demonstrating the convergence properties of the standard variances of x_n.

As the basic time jitter measure, we will choose to use the N-point unbiased standard variance of the samples x_n (also known as the sample variance in stationary statistics) given by

$$\sigma_{xd}^2(\tau, N) = < (N-1)^{-1} \sum_{n=1}^{N} (x_n - M_x(\tau, N))^2 > \tag{7}$$

because of its direct reference to the skew. In the above, <…> represents an ensemble average, and $M_x(\tau,N)$ is the skew given by the N-point arithmetic mean

$$M_x(\tau, N) = N^{-1} \sum_{n=1}^{N} x_n \tag{8}$$

For comparison, the closest 2nd difference variance is given by [10]

$$\begin{aligned} \sigma_{xa}^2(\tau, N) &= < \frac{0.25\tau^2}{N-1} \sum_{n=1}^{N} (\bar{y}_n - M_y(\tau, N))^2 > \\ &= 0.25\tau^2 \sigma_y^2(N, \tau, \tau) \end{aligned} \tag{9}$$

where

$$\bar{y}_n = \tau^{-1}(x_n - x_{n-1}) \tag{10}$$

and

$$M_y(\tau, N) = N^{-1} \sum_{n=1}^{N} \bar{y}_n \tag{11}$$

One can show that $\sigma_{xa}^2(N, \tau)$ can also be written as

$$\sigma_{xa}^2(\tau,N)=\frac{1}{4(N-1)}\sum_{n=1}^{N}<\left(x_{n+1}-x_n+\frac{x_N-x_1}{N}\right)^2> \quad (12)$$

This shows explicitly that the direct reference to the skew $M_x(\tau,N)$ in $\sigma_{xa}^2(N,\tau)$ has been eliminated.

Both these variances can be related to $S_x(f)$ the double-sideband (DSB) power spectral density (PSD) of x by using the spectral integral representation of the variance [25]

$$\sigma_x^2=\int_0^\infty S_x(f)\,|H_s(f)|^2\,K_x(f)df \quad (13)$$

where: (a) f is the fourier frequency from the carrier, (b) $K_x(f)$ is a kernel describing the properties of each type of variance ($K_x(f)$ is a stand-in for either $K_{xd}(f)$ or $K_{xs}(f)$.), and (c) $H_s(f)$ is the DSB frequency-domain response function corresponding to time-domain response $h_s(t)$. The reason a kernel is used rather than the square of a frequency response function is that N-point kernels cannot be written as the square of a single response function. For $\sigma_{xd}^2(\tau,N)$ and $\sigma_{xa}^2(N,\tau)$, one must write

$$K_x(f)=N^{-1}\sum_n|H_n(f)|^2 \quad (14)$$

where $H_n(f)$ is the response function for the n^{th} residual.

The kernel for $\sigma_{xd}^2(N,\tau)$ is given by

$$K_{xd}(f)=\frac{N}{N-1}\left[1-\frac{1}{N^2}\frac{\sin^2(N\pi f\tau)}{\sin^2(\pi f\tau)}\right] \quad (15)$$

and the kernel for $\sigma_{xa}^2(\tau,N)$ is given by

$$K_{xa}(f)=\frac{N}{N-1}\sin^2(\pi f\tau)\left[1-\frac{\sin^2(N\pi f\tau)}{N^2\sin^2(\pi f\tau)}\right] \quad (16)$$

These kernels are plotted in Figure 5. For $N>>1$ and $N\pi f\tau<<1$, the kernels can be approximated by

$$K_{xd}(f)\cong(1/3)N^2(\pi f\tau)^2 \quad [N>>1 \text{ and } N\pi f\tau<<1] \quad (17)$$

$$K_{xa}(f)\cong(1/3)N^2(\pi f\tau)^4 \quad [N>>1 \text{ and } N\pi f\tau<<1] \quad (18)$$

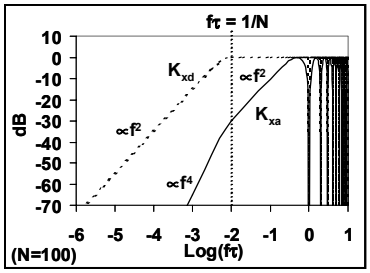


Figure 5. Kernels $K_{xd}(f)$ and $K_{xa}(f)$ vs fτ.

Thus in general, for

$$S_x(f)\propto 1/f^\alpha \quad (19)$$

$\sigma_{xd}^2(\tau,N)$ diverges when $\alpha>2$, but $\sigma_{xa}^2(N,\tau)$ doesn't diverge until $\alpha>4$. However, when $H_s(f)$ has a low-frequency cut-off, $\sigma_{xd}^2(\tau,N)$ can converge for $\alpha>2$.

For $N-\propto$ but finite $N\tau$, $K_{xd}(f)$ can be written as

$$K_{xd}(f)\cong 1-\sin c^2(\pi fN\tau) \quad [N\to\infty, \text{finite } N\tau] \quad (20)$$

From (20), one can see that $K_{xd}(f)\to 1$ when $N\tau$ also goes to infinity, so

$$\lim_{N\tau\to\infty}\sigma_{xd}^2(\tau,N)\cong\sigma_{x-std}^2=\int_0^\infty df\,|H_s(f)|^2\,S_x(f) \quad (21)$$

where σ_{x-std}^2 is a single point standard variance given by

$$\sigma_{x-std}^2=<(x_n-<x_n>)^2> \quad (22)$$

Thus, when $N\tau$ is large, one can use σ_{std}^2 for $\sigma_{xd}^2(\tau,N)$ unless mathematical difficulties force one to retain the use of $\sigma_{xd}^2(\tau,N)$ with finite but large $N\tau$.

$|H_s(f)|^2$ is often approximated by a square bandpass filter. In this case, σ_{std}^2 becomes a bandpass variance

$$\sigma_{x-std}^2\to\sigma_{x-bpass}^2=\int_{f_l}^{f_h}S_x(f)df \quad (23)$$

where f_h is a high frequency cut-off and f_l is a low frequency cut-off.

Now let us use the statistical theory established in the previous section as a framework for discussing the properties of time jitter for the various categories of digital systems shown in Figure 1.

IV. TIME JITTER AND SYNCHRONOUS DATA TRANSFER

The first category in Figure 1 is synchronous data transfer. As mentioned previously, this category has a common clock that is distributed to all digital subsystems along with the data. The net effect of this is to cancel clock oscillator contributions to the time jitter at low frequencies. There is some residual oscillator noise at the very highest Fourier frequencies due to time misalignments between the gate clocks in various parts of the system. This misalignment can be represented by a highpass response function given by

$$|H_s(f)|^2 = 4\sin^2(\pi f \tau_m) \tag{24}$$

where τ_m is the time misalignment. For simplicity, let us fold in this highpass filtered oscillator noise into the logic gate white noise. The PSD of logic gates can be represented by

$$S_x(f) = g_o(1 + f_k / f) \tag{25}$$

Here, we are assuming that the logic gate PSD has the same spectral form as the PSD of the amplifiers and transistors that logic gates are composed of [24]. g_o is the white-x noise density coefficient and f_k is a parametric 1/f knee that is given by the frequency at which the 1/f noise density equals the white noise density.

For this category, $H_s(f)$ can be approximated with a square lowpass filter. Thus, f_l is equal to zero because there is no physical reason to introduce a low frequency cut-off, and f_h is equal to f_g, where f_g is the analog noise bandwidth of the components used in the gates. Note that f_h is not f_o the clock frequency, which in general is much smaller than f_g. Since a digital system steps uniformly in time from state to state at the clock frequency f_o, it is equivalent to a uniformly sampled system. Thus the analog $S_x(f)$ noise in bandwidth f_g is aliased by this sampling into a smaller sampled bandwidth f_o [25]. As shown in Figure 6, this multiplies the effect of the white noise in $S_x(f)$ by a factor of f_g/f_o for time jitter considerations.

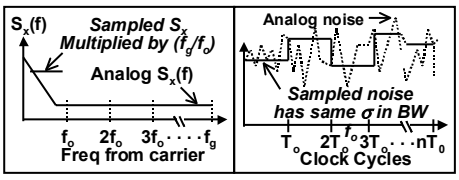


Figure 6. Aliasing of white noise in digital systems.

Since we have included a 1/f term in (25), we need to consider its impact on σ^2_{xd}. Using (17) in (13), one can show that

$$\sigma^2_{xd} \cong f_k g_o \ln(\pi f_g N\tau) + f_g g_o \tag{26}$$

Thus, the 1/f term in (26) equals the white term when

$$T_k = N\tau = \frac{e^{f_g/f_k}}{\pi f_g} \tag{27}$$

One can show, for all the types of logic families that exist, that T_k is much greater than the life of the universe. Thus, we can ignore the flicker term in (25) and (26) for all practical values of $N\tau$ and write

$$\sigma^2_{xd}(\tau, N) \cong \sigma^2_{x-std} \cong f_g g_o \tag{28}$$

In other words, for synchronous systems, we only need use white noise terms for jitter calculations.

V. TIME JITTER AND ASYNCHRONOUS DATA TRANSFER

In asynchronous systems, only data is sent from the master unit or transmitter to remote units or receivers, and local clock oscillators (LOs) in the remote units are synchronized to the master clock oscillator (MO) using phase locked loops (PLLs). Because of this, relative MO-LO clock oscillator time jitter is generated at the receivers in addition to synchronous jitter. The PLL in each receiver can be described by a baseband response function pair $h_p(t)$ and $H_p(f)$ [26]. $H_p(f)$ has a lowpass response with a bandwidth B_p. For fourier frequencies less than B_P, the LO tracks the MO and suppresses the MO-LO jitter, so the MO-LO contribution to the time jitter variance can be written as [19]

$$\sigma^2_{x-std} = \int_0^\infty S_x(f)\,|1 - H_p(f)|^2\,|H_h(f)|^2 df \cong \int_{B_p}^{f_h} S_x(f) df \tag{29}$$

where: (a) $S_x(f)$ is the sum of the PSDs of all the oscillators in the Tx-Rx link (MO and LO plus other LOs in the Tx-Rx link), and (b) $H_h(f)$ is the DSB complex envelope response of the transmit-receiver link [19]. For communications systems, $H_h(f)$ can be approximated by a square lowpass filter where f_h is equal to ½ the symbol rate R_s [19]. For other asynchronous data transfer systems such as RS-422, one has to analyze the system in detail to obtain f_h (f_g can be used as a worst case value).

VI. TIME JITTER AND DIGITAL SAMPLING

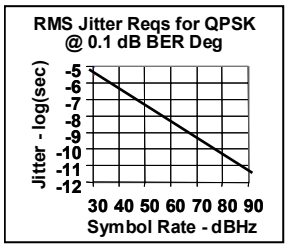


Figure 7. RMS Jitter that will produce 0.1 dB BER degradation in QPSK systems [19].

Time jitter in digital sampling causes two effects: (1) BER degradation in digital communications systems symbol (or bit) decision circuits, and (2) noise power in A/Ds and D/As. Symbol decision circuits in communications receivers turn the received analog signal into a stream of digital symbols by comparing the signal to one or more decision thresholds at sampling clock epochs [19]. Jitter in these epochs creates multiplicative voltage noise, which is generated from the coherent input signal by slope modulation as shown in Figure 2. In symbol decision circuits, this multiplicative noise interacts with thermal noise that is present along with the signal to increase the BER for a given input SNR, and is called BER degradation [19]. The appropriate time jitter variance for computing this effect is the sum of the synchronous and asynchronous MO-LO variances. Figure 7 shows the RMS Jitter that will produce 0.1 dB of BER degradation in QPSK systems as a function of symbol rate [19]. Note that, for systems in the GHz symbol rate range, the time jitter requirement approaches 1 ps.

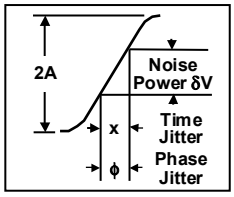


Figure 8. Noise power generation in A/D and D/A converters [22].

In A/Ds and D/As, the multiplicative noise is called noise power [20-23]. To determine the size of this noise power as a function of the sampling clock jitter, consider Figure 8. The following simple derivation of the noise power in A/Ds due to sampling clock jitter is based on that in reference [22]. The derivation can also apply to D/As with some redefinition in terminology. Let us assume the input signal is a sinewave given by

$$V(t) = A \cdot \sin(\omega_s t + \phi) \tag{30}$$

where ϕ is the phase error due to sampling clock jitter, $\omega_s = 2\pi f_s$ is the sinewave angular frequency, and A is the sinewave amplitude. If we assume that the sampling point is near the middle of the sinewave, one can see from Figure 8 that

$$\phi = \omega_s x = \delta V / A \quad [\text{near zero}] \tag{31}$$

Taking the variances of both sides of (31), we obtain near zero

$$2\sigma_V^2 / A^2 = \sigma_V^2 / P_s = 2\sigma_\phi^2 = 2\omega_s^2 \sigma_{x-std}^2 \quad [\text{near zero}] \tag{32}$$

where P_s the average power in the sinewave is

$$P_s = A^2 / 2 \tag{33}$$

Equation (32) is pessimistic for the average noise to signal ratio (NSR) because the sampling point is not always near the center of the sinewave. Using σ_ϕ^2 without the factor of 2 as a better approximation for σ_V^2 / P_s, the noise to signal ratio (NSR) and signal to noise ratio (SNR) can be written as

$$NSR_{jitter} = SNR_{jitter}^{-1} = \sigma_\phi^2 = \omega_s^2 \sigma_{x-std}^2 \tag{34}$$

Note that the SNR_{jitter} limit in (34) is independent of the number of digitized bits. Thus, time jitter requirements become more restrictive as the number of digitized bits in A/Ds and D/As increases.

For white time jitter, the sampled voltage PSD in the digitized signal is given by the voltage variance divided by the clock frequency f_o [27]

$$S_V(f) \cong f_o^{-1} P_s \omega_s{}^2 \sigma_{x-std}^2 \quad [\text{for white x-jitter}] \tag{35}$$

The effective number of bits (ENOB) can be derived from (34), if we make some further assumptions about the operating conditions. These assumptions are not unique. The ones chosen here lead to more conservative ENOB formulas than those in other references [22], but are more realistic in terms of actual operating conditions.

To generate the ENOB from (34), one first has to define the relationships between various contributions to the NSR. For our definition of ENOB, let us assume that the NSR_{jitter} equals NSR_{quant} the NSR due to quantization error and that there are no other NSR contributors (such as A/D inaccuracies above the quantization level). Thus, we will assume the total NSR is given by

$$NSR_{tot} = 2 \cdot NSR_{jitter} \tag{36}$$

Second, one has to define the input signal power relative to A/D full scale. Let us assume the input signal power is backed-off (BO) by a factor η from the value for a full-scale osculating sinewave (A = ½ of full scale). For the purpose of generating the ENOB charts to be described below, we will assume the BO η is -10 dB because this value approximately optimizes the SNR for a Gaussian signal input [20, 22]. This differs from the BO used in [22], which uses the value of η = 0 dB, an unrealistic value for complex signal inputs. For a BO of η, NSR_{quant} is given by [20, 27]

$$NSR_{qaunt} = (2/3)\ 2^{-2L} / \eta \tag{37}$$

where L is the number of A/D quantization bits.

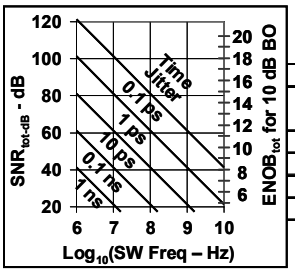
Using (34), (36), and (37), we can thus write NSR_{tot} as

$$NSR_{tot} = 2\omega_s^2 \sigma_{x-std}^2 = (2/3)\ 2^{-2 \cdot ENOB_{tot}} / \eta \tag{38}$$

where we have set NSR_{tot} equal to an NSR_{quant} value that would be obtained if it were the only contributor to the NSR. Rewriting (38), we obtain

$$ENOB_{tot} = -\log_2[(3\eta)^{1/2}\omega_s\sigma_{x-std}] \qquad (39)$$

The graph in Figure 9 shows the time jitter requirements as a function of the total SNR and ENOB verses the sinewave frequency, and the table in the figure gives typical numerical values. Note, for a 16-bit $ENOB_{tot}$, that 1 ps of jitter is required for digitizing a 4 MHz signal, and 0.1 ps of jitter is required at 44 MHz. Correspondingly, for a 10 bit $ENOB_{tot}$, the 1 ps and 0.1 ps thresholds are crossed for 300 MHz and 3 GHz signals. Thus, time jitter requirements for high speed A/Ds and D/As are extremely stringent. This is a major performance limiting issue for high-speed A/Ds and D/As.



Jitter→	1 ps	0.1 ps
ENOB tot	SW Freq MHz	SW Freq MHz
16	4	44
12	71	709
10	284	2838
8	1135	11351

Figure 9. SNR_{tot} and $ENOB_{tot}$ as a function of time jitter and sinewave frequency for η_{dB} = -10 dB .

How to calculate σ^2_{x-std} or σ^2_{xd} for digital sampling systems in the presence of $1/f^n$ noise is a matter of application. For systems in which there is a common analog signal and sampling clock, one would use the formulas for synchronous data transfer. Similarly, when the sampling clock is locked to the analog signal clock through a PLL or some equivalent, one would add the MO-LO time jitter formulas for asynchronous data transfer to the synchronous jitter. For totally unsynchronized clocks, the standard variances diverge in the presence of $1/f^3$ and higher power noise. However, the equivalent of a PLL is often buried in hidden calibration applied to nominally unsynchronized systems.

VII. SUMMARY & CONCLUSIONS

Now let us summarize some of the major conclusions from the paper. First, it has been shown that if one explicitly includes the properties of the system response function $h_s(t)$ for various types of digital systems, one can use the standard variances $\sigma^2_{xd}(\tau, N)$ and σ^2_{x-std} to define time jitter when $1/f^n$ noise is present. Second, in synchronous data transfer, time jitter causes hard bit errors, one need only consider the white noise component, and one must consider the effects of aliasing on this noise component. Third, in asynchronous systems, time jitter can also cause soft errors or bit error rate degradation, and there is additional jitter due to relative MO-LO clock oscillator jitter. Furthermore, $1/f^n$ clock oscillator noise contributes to this MO-LO jitter, and the jitter is bounded because of the highpass properties PLL's in the system. Finally, for digital sampling, noise power in A/Ds and D/As generated by sampling clock jitter is a major limitation on the effective number of bits in high-speed devices.

[1] IEEE Standard for Digitizing Waveform Recorders, IEEE Std. 1057-1994, IEEE, 1994.

[2] ANSI/IEEE Std 802.3a,b,c,e-1988, (Supplements to ANSVIEEE Std 802.3-1985), An American National Standard IEEE Standards for Local Area Networks: Supplements to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, IEEE 1988.

[3] IEEE Std 802.11, Information technology —Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements —Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, IEEE 1999.

[4] IEEE Std 181-2003, IEEE Standard on Transitions, Pulses, and Related Waveforms, IEEE 2003.

[5] Jean-Marie Janik, Daniel Bloyet, and Benoît Guyot, Measurement of Time Jitter Contributions in a Dynamic Test Setup for A/D Converters, IEEE Trans. I&M, VOL. 50, NO. 3, JUNE 2001, p786.

[6] Agilent (no author listed), Measuring Jitter in Digital Systems, Application Note 1448-1, http://cp.literature.agilent.com/litweb/pdf/5988-9109EN.pdf, June 1, 2003.

[7] Brian Fetz, Jitter Measurements in Digital Circuits, http://www.home.agilent.com/upload/cmc_upload/All/01-24-03-Jitter-Digital-Circuits-Fetz_794-NOTES.pdf, January 24th, 2003.

[8] S. Saad, The effect of accumulated time jitter on some sine-wave measurements," IEEE Trans. Instrum. Meas., 44, pp. 945–951, 1995.

[9] ITU-T Recommendation G.810 (08/96), Definitions and Terminology for Synchronization Networks. ITU, 1996.

[10] James A. Barnes, et. al., "Characterization of Frequency Stability, IEEE Trans. I&M, v IM-20, no 2, May, 1971, p105.

[11] B. E. Blair, Ed, Time and Frequency Fundamentals, NBS Monograph 140, U. S. Govt. Printing office, CODEN:NBSMA6, 1974 p166.

[12] L. S. Cutler and C. L. Searle, Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards, Proc. IEEE v 54, no 2, February, p 136.

[13] Patrick Lesage and Claude Audoin, Characterization of Frequency Stability: Uncertainty due to the Finite Number of Measurements, IEEE Trans. I&M, v IM-22, no 2, June, 1973, p 157..

[14] J. Rutman and F. L. Walls, Characterization of Frequency Stability in Precision Frequency Sources, Proc. IEEE, v 79, no 7, July, 1991, p952.

[15] D. B. Sullivan, D. W. Allan, D. W. Howe, F. L. Walls, Characterization of Clocks and Oscillators, NIST Technicla Note 1337, CODEN:NTNOEF, U. S. Government Printing Office, January, 1990.

[16] W.F. Walls and F.L. Walls, Computation of Time-domain Frequency Stability and Jitter from PM Noise Measurements," Proc. 2001 IEEE Int. Freq. Cont. Symp., 161–166.

[17] D. A. Howe and T. N. Tasset, Clock Jitter Estimation based on PM Noise Measurements, Proceedings of the 2003 IEEE International Frequency Control Symposium Jointly with the 17th European Frequency and Time Forum, August, 2003, Montreal.

[18] IEEE 1139-1999: Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology—Random Instabilities, IEEE, 1999.

[19] Victor S. Reinhardt, The Calculation of Frequency Source Requirements for Digital Communications Systems, Proceedings of the IEEE International Frequency Control Symposium 50th Anniversary Joint Conference, 24-27 August, 2004, Montréal, Canada. See also http://www.ieee-uffc.org/freqcontrol/Reinhardt_files/frame.htm.

[20] Glenn A. Grey and Gene W. Zeoli, "Quantization and saturation noise due to analog-to-digital conversion," IEEE Trans. on Aerospace and Electronic Systems, Jan. 1971, pp 222-223.

[21] T. Michael Souders, Donald R. Flach, Charles Hagwood, Grace L. Yang, The Effects of Time Jitter in Sampling Systems, IEEE Trans. I&M, VOL. 39, NO. 1, FEBRUARY, 1990, p80.

[22] Analog Devices (no author listed), Mixed-Signal and DSP Design Techniques, Section 2, Sampled Data Systems, internet published, see http://www.analog.com/Analog_Root/static/pdf/dataConverters/MixedSignal_Sect2.pdf, p35-36.

[23] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Std 1241-2000, IEEE 2000.

[24] F.L. Walls, E.S. Ferre-Pikal, and S.R. Jefferts, The Origin of 1/f PM and AM Noise in Bipolar Junction Transistor Amplifiers, IEEE Trans. Ultrasonics, Ferroelectrics, and Frequency Control, 44, pp. 326–334, March 1, 1997.

[25] John G. Proakis, Digital Communications, McGraw-Hill, 1989.

[26] William F. Egan, Frequency Synthesis by Pahse Lock, Wiley-Interscience, 1999.

[27] Lawrence R. Rabiner and Bernard Gold, Theory and Application of Digital Signal Processing, Prentice-Hall 1975.