Digital Recursive Oscillator with Reduced Frequency versus Temperature Dependency Utilizing a Dual-Mode Crystal Oscillator

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***Abstract*—The paper deals with a reduction of static frequency vs. temperature (f-T) dependency of digitally generated sinusoidal signals. The f-T dependency reduction is based on a self-temperature-sensing of a quartz crystal in dual-mode crystal oscillator, which produces the reference clock. We have proposed a digital oscillator, which automatically compensates the f-T dependency of its sampling clock over a wide range of operating temperatures. Numerical accuracy limitation of the oscillator due to finite word-length arithmetic is also analyzed in this article.**

I. INTRODUCTION

Digital sinusoidal oscillators are widely used in digital signal processing and they are essential elements in many applications. Usually, frequency stability of a digitally synthesized signal is determined by the frequency stability of the reference clock signal used. However, last year we have published an effective implementation of the clock signal static frequency vs. temperature (f-T) dependency compensation utilizing field programmable gate arrays (FPGA) and a single-chip direct digital synthesizer (DDS) [1]. In addition to DDS, digital sinusoidal signals can be flexibly synthesized using the digital recursive oscillator (second-order recursive system with zero damping).

Simple recursive oscillator can be characterized by the second-order difference equation with two initial conditions:

$$y_n = 2\cos\left(2\pi\frac{f}{f_S}\right)\cdot y_{n-1} - y_{n-2}\,,\quad n = 0,1,2,3,... \qquad (1)$$

$$y_{-1} = 1,\quad y_{-2} = \cos\left(2\pi\frac{f}{f_S}\right)$$

In (1) f_S represents the sampling clock frequency and f the frequency of the generated sinusoidal signal.

We have designed a digital recursive oscillator, which automatically compensates the static f-T dependency of its sampling clock. The cosine coefficient of the recursive oscillator is automatically evaluated regarding to an actual sampling clock frequency. In this way, the stability of the recursive oscillator is improved.

The utilized crystal self-thermometry eliminates temperature offset and lag effects since no external temperature sensor is used [2], [3]. A dual-mode crystal oscillator (DMXO), which excites simultaneously fundamental and 3rd overtone c-modes (i.e. slow-shear acoustic modes) of the stress compensated (SC) crystal, was originally published in [3]. Processing of the both c-modes actual frequencies enables prediction of their frequency shifts due to ambient temperature variations in a wide range.

II. FUNCTIONAL DESCRIPTION

Block diagram of compensated recursive oscillator, we have designed, is shown in Fig. 1. We utilized a dual gain loop DMXO, which has been described in [3] and [4]. The sampling clock signal of a digital-to-analog converter (DAC) is directly driven from the 3rd overtone part of the DMXO.

Interpretation of all registers and variables in FPGA is integer. Basic numerical precision was considered b=30 bits. It means that the real value 1.0 was in FPGA internally represented by the integer 2^{30}. One more bit was utilized if negative integers (in twos complement representation) were necessary.

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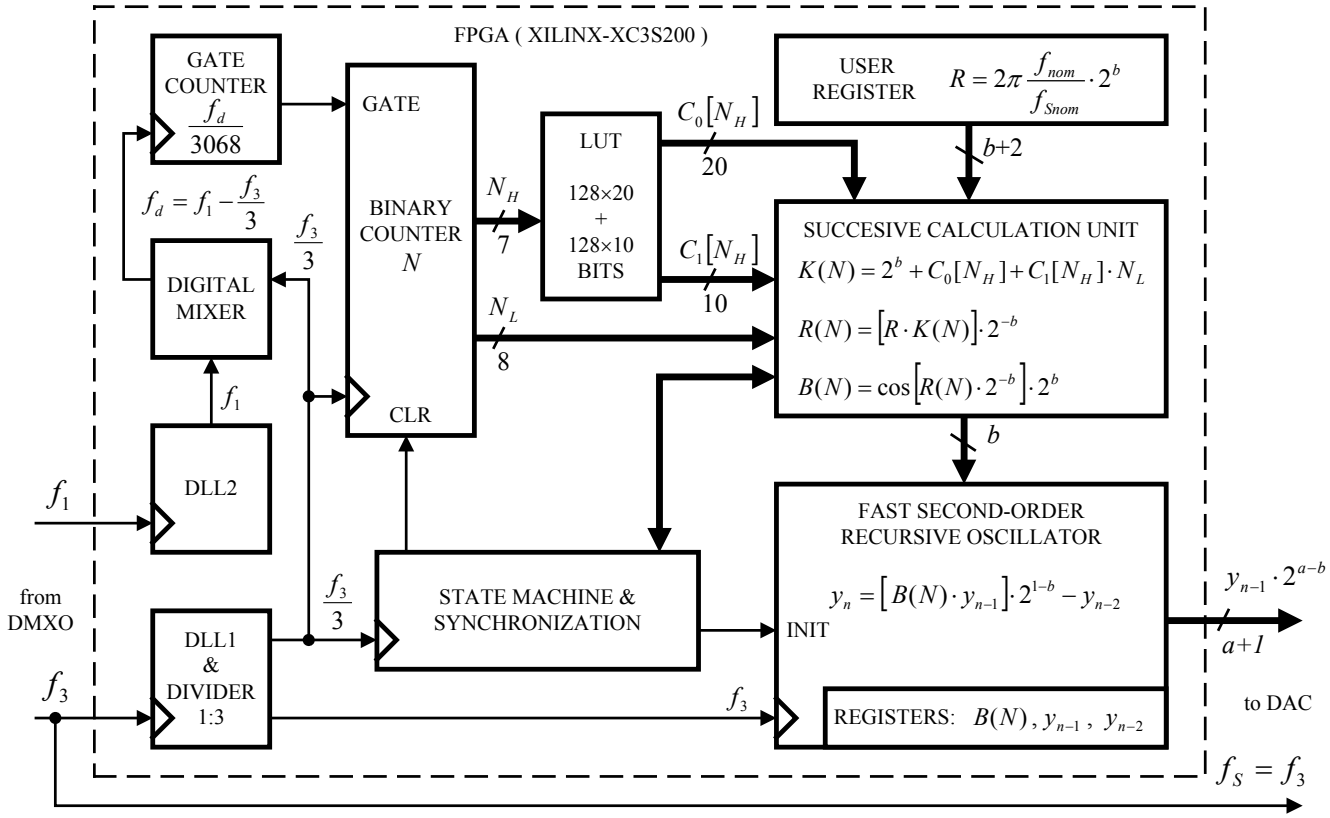

Figure 1. Block diagram of the recursive oscillator, which incorporates the sampling clock f-T dependency compensation.

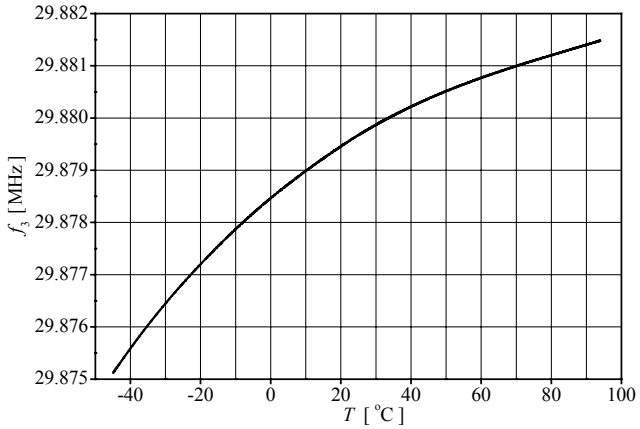

Figure 2. The SC crystal 3rd overtone c-mode series resonant frequency vs. temperature.

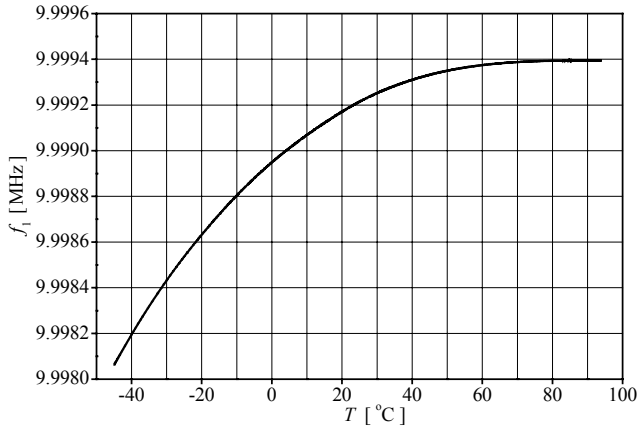

Figure 3. The SC crystal fundamental c-mode series resonant frequency vs. temperature.

The slow successive calculation unit evaluates the cosine coefficient $B(N)$ for the fast second-order recursive oscillator approximately twelve times per second regarding to the actual sampling clock frequency f_S. The sampling clock frequency depends on the 3rd overtone c-mode series resonant frequency f_3 of the used crystal unit. Figure 2 captures the actual f_3 vs. temperature dependency. The actual fundamental c-mode series resonant frequency f_1 vs. temperature dependency is shown in Fig. 3.

An effective internal clock forming circuits, digital mixer and gate counter implementations have been published in [1]. Subtracting one third of the sampling clock frequency (i.e. $f_3/3$) from the fundamental frequency f_1 using a digital mixer yields the difference frequency f_d. Figure 4 shows that the difference frequency is almost linear function of the temperature with the slope approximately -135 ppm per °C. The difference frequency varies more than 18 000 ppm over the temperature range between -45°C and +85°C.

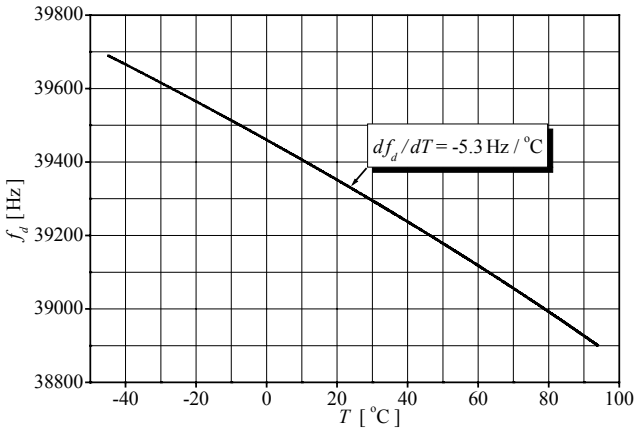

Figure 4. The difference frequency vs. temperature.

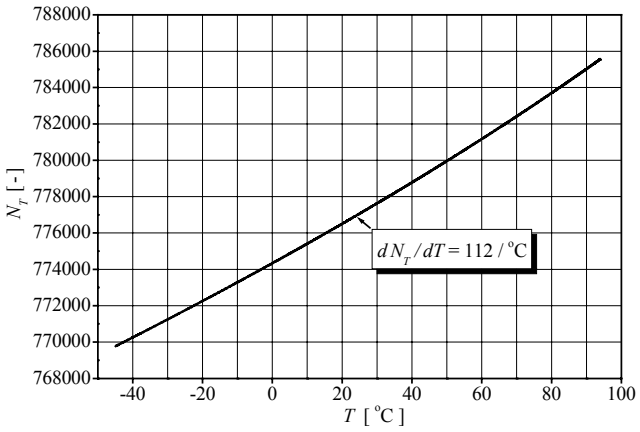

Figure 5. Total amount of the pulses accumulated during the interval $3068/f_d$ vs. temperature.

The gate counter produces the time interval $3068/f_d$ during which the 15-bit binary counter accumulates pulses with frequency $f_3/3$. During the interval the 15-bit binary counter 47 times overflows. After the accumulation the content of the 15-bit binary counter is given by:

$$N = N_H \cdot 2^8 + N_L = N_T \bmod 2^{15} = \\ = \mathrm{int}\left(\frac{f_3}{3f_1 - f_3} 3068\right) \bmod 2^{15} \qquad (2)$$

In (2) N_T represents total amount of the pulses, N_H represents seven most significant bits and N_L represents eight least significant bits of the 15-bit binary counter. Figure 5 illustrates total amount of the accumulated pulses N_T vs. temperature. N_H forms the address bus of two look-up tables, which store the set of pairs of coefficients: C_0 and C_1. An effective implementation of the two look-up tables has been illustrated in [1].

The successive calculation unit utilizes the C_0 and C_1 coefficients to calculate the correction factor $K(N)$ according to following formula:

$$K(N) = 2^b + C_0[N_H] + C_1[N_H] \cdot N_L \qquad (3)$$

The coefficients C_0 are actually implemented as signed integers in 20-bit representation and the coefficients C_1 as signed integers in 10-bit representation. The $K(N)=2^b$ in the case when the actual sampling clock frequency reaches its nominal value f_{Snom}. During the system calibration the value f_{Snom} is used to determine the set of coefficients C_0 and C_1. The coefficients computation is made using a simple PC program we have developed. The computation is based on the data set representing the actual f-T characteristics of DMXO. During a prototype verification we considered $f_{Snom} = f_3(25^oC) = 29.879\,670$ MHz.

A user has to set an initial 32-bit value R that represents the relative angular frequency of the required sinusoidal signal, which has to be generated. Considering the nominal sampling clock frequency f_{Snom}, the R should be set according to following formula:

$$R = \mathrm{int}\left(2\pi \frac{f_{nom}}{f_{Snom}} \cdot 2^b\right), \quad \frac{f_{nom}}{f_{Snom}} \le 0.25 \qquad (4)$$

The successive calculation unit evaluates the compensated relative angular frequency according to the previously calculated correction factor:

$$R(N) = \left[R \cdot K(N)\right] \cdot 2^{-b} \qquad (5)$$

The most complicated task for the successive calculation unit is the evaluation of the cosine coefficient $B(N)$ required for the fast second-order recursive oscillator. The evaluation is based on the previously calculated value $R(N)$ and on the Taylor expansion of the cosine. In the integer representation it can be expressed by following formula:

$$B(N) = 2^b + \sum_{k=1}^{6} \left\{ (-1)^k \cdot \left(\frac{R(N)^2 \cdot 2^{-b}}{2}\right)^k \cdot \mathrm{int}\left(\frac{2^{b+k}}{(2k)!}\right) \cdot 2^{-b} \right\} \qquad (6)$$

The successive calculation unit can be effectively implemented in Spartan-3 devices with "SRL16E" elements we have described in [1]. The modules realize the computation of (5) and (6) should be designed regarding to the maximum required alternating rate of generated sinusoidal signal frequency (i.e. alternating rate of the R). In general, a successive multiplication requires much longer computational time when compared with a parallel multiplication. On the other hand the successive multiplication can considerably save an FPGA resources. An example of the effective successive multiplication has been published in [1].

When the successive calculation unit has finished the new cosine coefficient $B(N)$ calculation it is written to the dedicated register. Simultaneously the two storage registers within the fast second-order recursive oscillator are initialized as follows:

$$y_{n-1} = 2^b \; ; \quad y_{n-2} = B(N) \tag{7}$$

Fast second-order recursive oscillator calculates one new value y_n per one sampling clock period as follows:

$$y_n = \left[B(N) \cdot y_{n-1}\right] \cdot 2^{1-b} - y_{n-2} \tag{8}$$

To calculate (8) a fast (b+1)×(b+1)-bit multiplier and a fast (b+1)-bit subtracter has been utilized. The multiplier has been implemented with assistance of the four dedicated 18×18-bit hardware multipliers. It should be noted that the repetitive initialization of the storage registers removes the errors eventually accumulated during the continuous operation of the recursive oscillator. On the other hand the initialization produces a phase discontinuity of the generated sinusoidal signal.

The data for a DAC can be derived directly from the most significant part of the y_{n-1} storage register:

$$y_{n-1} \cdot 2^{a-b} \approx \mathrm{int}\left\{ \cos\left[R(N) \cdot 2^{-b} \cdot n\right] \cdot 2^a \right\} \tag{9}$$

In this case, the generated sinusoidal signal is in the form of sequence of a-bit truncated signed integers.

The recursive oscillator we have designed occupies approximately one third of XC3S200 resources. The utilized FPGA-XC3S200 is the low-density (200 000 equivalent system gates) member from the Spartan-3 FPGA family.

III. Effect of The Cosine Coefficient Quantization

Limited numerical precision induces a quantization error of the cosine coefficient. An impact of the cosine coefficient least significant bit to the relative shift of sinusoidal signal frequency can be evaluated as follows:

$$\delta f = \frac{\arccos\left[\cos\left(2\pi \frac{f}{f_S}\right) \cdot \frac{2^b - 1}{2^b}\right] - \left(2\pi \frac{f}{f_S}\right)}{\left(2\pi \frac{f}{f_S}\right)} \tag{10}$$

Figure 6 captures the mentioned impact in the cases of numerical precision: b=24, 26, 28 and 30. It is evident that the error dramatically rises in the case of very low frequencies. In the case of basic numerical resolution b=30 bits, the usable range of the relative frequencies is approximately between 0.02 and 0.25.

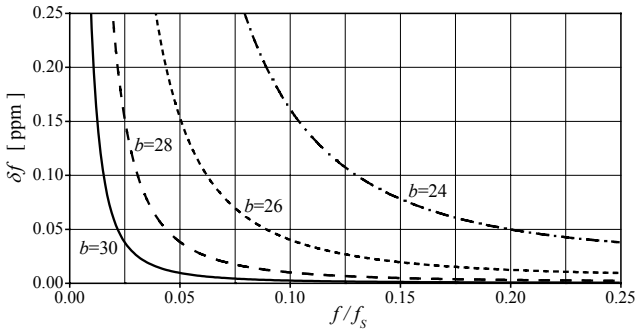

Figure 6. Relative shift of generated sinusoidal signal frequency due to quantzation of the cosine coefficient; error=-1LSB.

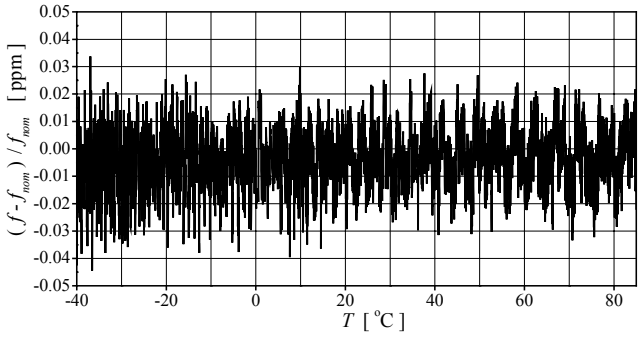

Figure 7. Residuals vs. temperature; f_{nom}=1.000 000 MHz, b=30 bits.

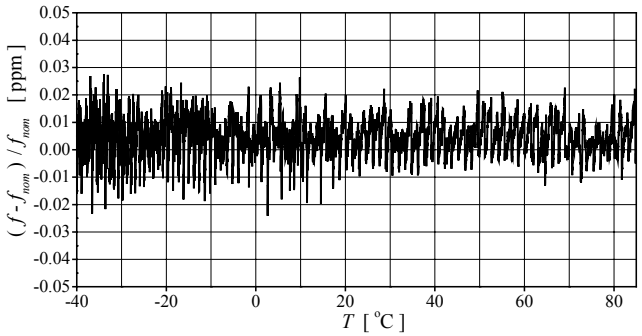

Figure 8. Residuals vs. temperature; f_{nom}=7.000 000 MHz, b=30 bits.

IV. Results

Figure 7 and 8 illustrates the shift between frequency of generated sinusoidal signal and the nominal frequency in the case of f_{nom}=1.000 000 MHz and f_{nom}=7.000 000 MHz respectively.

Output power spectrum mostly depends on the characteristics of the utilized DAC. The power spectrum calculated with assistance of 2084-point fast Fourier transform in the case of 14-bit DAC (e.g. AD9744) is illustrated in Fig. 9. However, the noise close to the generated carrier particularly depends on the DMXO and SC crystal properties [5], [6].

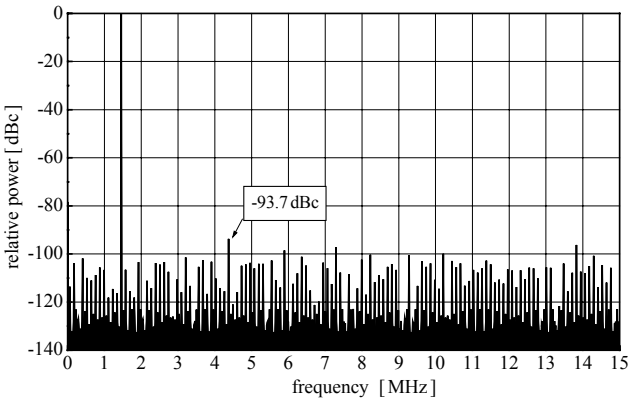

Figure 9. Calculated spectrum of the recursive oscillator output signal with assistance of 2048-point FFT; f_{nom}=1.458 870 MHz, 14-bit DAC (AD9744).

V. CONCLUSIONS

The presented compensation method can significantly reduce static f-T dependency of the digital recursive oscillator over a wide range of operating temperatures without a need of stabilization of reference crystal oscillator temperature. There is also no need of tuning the crystal oscillator frequency.

Since the crystal self-thermometry is utilized and no external temperature sensor is used, the temperature offset and lag effects are eliminated.

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