LOW PHASE NOISE UHF TCXO

D. V. Bogomolov, R. Boroditsky
Valpey-Fisher Inc., 75 South Street, Hopkinton, MA 01748, USA

Abstract – **Low phase noise, good frequency stability over wide temperature range, tight initial frequency calibration and low power consumption of the signals sources are essential for many modern communication applications operating in UHF frequency band. The best sample of TCXO can provide good combination of these parameters only in 10÷50 MHz frequency band. A frequency translation technique should be applied to transform those signals in UHF band without phase noise degradation. UHF VCXO looked by PLL on a signal of 10Mhz TCXO allows to keep a good temperature stability and to achieve a phase noise level $L_\varphi(1\ kHz)$=-108 dBc/Hz at 1 GHz carrier frequency. The circuit optimization allows decreasing an influence of PLL noise and obtaining a spectral purity of output signal, the level of a comparison frequency signal doesn't exceed –85dBc.**

Keywords **- low phase noise, TCXO, UHF band, PLL circuit**

I. INTRODUCTION

Modern communications protocols, radar equipment, high frequency DAC, DSP, est. require low phase noise, good frequency stability and low power consumption of UHF frequency sources. A small size and low cost of the oscillators are essential as well. For example, in digital links employing quadrature-amplitude modulation (QAM), different phase states represent digital bits. Excessive phase noise in the system can obscure these bits, resulting in an excessively high bit-error rate and possible loss of data. So the phase noise requirements are determined by the allowable bit error rate in the channels data stream. Good frequency stability over temperature range and initial frequency calibration are essential in applications, which use UHF signals synchronization. The frequency discrepancy of these signals should be in a certain narrow band for fast phase look. That requirement defines a demanding frequency stability of UHF signal sources. The low power consumption is important for equipment operating under autonomous power supply conditions.

The combination of these parameters for UHF band signals can be achieved in TCXO. Modern small size TCXO can provide a good temperature compensation of a frequency drift Δf= ± 0.5 ppm in -40÷85°C range and low phase noise $S_\varphi(1\ kHz)$=-130 dBc/Hz at l0 –50 MHz frequency band. An extension of the traditional design technique of a temperature compensation oscillator into UHF band is complicated by larger frequency dependency upon the circuit components, long-term stability (aging) of the crystal, etc. Proposed approach employs a PLL technique using standard, low cost, good aging, small, well compensated low frequency TCXO as a reference; standard low cost PLL IC with low pass filter (LPF); and UHF band low phase noise voltage control crystal oscillator (VCXO).

The application of PLL technique has well known shortcomings [1]:

1) PLL contributes "technical noise" and a spur on comparison frequency;
2) necessary to provide larger pull-ability of UFH VCXO for aging and temperature drift compensation;
3) the value of output frequency should belong to a frequency grid.

This paper is concerned with UHF band TCXO design and discuses how to keep low phase noise in PLL based devices.

II. AN EVALUATION OF TCXO PARAMETERS

The phase noise of the output signal in PLL circuit is determined by the phase noise of output oscillator in offset frequencies realm above a cutoff frequency (f_{cut}) of low-pass filter (LPF). To rich a low level of phase noise TCXO in UHF band it is necessary to use low noise VCXO as output oscillator. Proposed VCXO is based on Pierce circuit with low cost 3rd overtone AT-cut crystal resonator. VCXO may be fabricated in 50÷250 MHz the frequency range of the carrier signal. If higher output frequencies are required - the selection of the 3rd or the 5th harmonic of the main oscillation allows to extend the range of the output signal to up to 1GHz. Further filtration and amplification provides the suppression of undesirable harmonics typically down to -50 dBc.

The main means to decrease an influence of PLL comparison frequency (f_{comp} – frequency of the signals at the phase detector inputs) on a spectrum of the output signal is an increase of f_{comp}/f_{cut} ratio. The value of the comparison frequency is determined as maximum of common multiple of required output frequency f_{out} and reference frequency of a phase detector. To determine a minimum possible value of f_{cut} , it is necessary to evaluate UHF VCXO phase drift at time interval $\tau = 1/f_{cut}$. It is possible to do by using the common formula [2] by means of a calculation of the phase deviation at a time interval τ:

$$\sigma^2_{\Delta\varphi}(\tau) = 8\int_0^\infty S_\varphi(f)[\sin(\pi f \tau)]^4 df \quad (1)$$

to simplify equation we can change low integral limit by $f_\tau = 1/\tau$ and upper by $2f_{out}$ [3], it is important to take in to account that the value of the integral mostly depends upon contribution at low frequencies. So we assume that the phase noise behavior describes following function $S_\varphi(f) = \beta_3/f^3$ and we may use referent point $S_\varphi(1kHz)$ = -125 dBc/Hz at 200 MHz crystal frequency for a calculation. To resolve equation (1) with regard to τ it is possible to modify it into the following form:

$$\sigma^2_{\Delta\varphi}(\tau) = 4\beta_3\left[1/f_\tau^{\,2} - 1/f^2_{\max}\right] \quad (2),$$

where $f_{\max}$ is maximum frequency in the realm where a phase noise graph has the slope $1/f^3$. The second term of the equation (2) gives an infinite small contribution if

$f_\tau << f_{\max}$. So if we can assume phase drift $\sigma_{\Delta\varphi}$= 0.01 radian, because that value is compatible with intrinsic noise of phase detector in PLL circuit , we obtain simple expression for τ:

$$\tau = \sigma_{\Delta\varphi} / 2\sqrt{\beta_3} = 0.5$$

That result similar to the equation from [4], that source gives us in those conditions:

$$\sigma^2_{\Delta\varphi}(\tau) = \tau^2 \beta_3 \ln 2$$

Both equations are showing that UHF VCXO phase is stable at the time interval about 1 second. The value of LPF cut-off frequency f_{cut} may be decreased down to 2 Hz, so the ratio f_{comp}/f_{cut} usually may be chosen large than 20 thousand. It gives good opportunity to suppress the comparison frequency signal and to reduce an influence of PLL noise on VCXO. The level of spurious, generated by comparison frequency signal in the output spectrum is below -85 dBc, while the level of other spurious components is below -120 dBc/Hz.

The developers of IC pay a lot of attention to the layout techniques for the low jitter PLL's. Dedicated analog V_{CC} /GND pins for the core analog blocks helps isolate them from supply variations. Guard rings which surround the analog blocks are tied to analog supplies to quiet the substrate. The external filter pin is placed between the analog power to avoid stray coupling outside the chip and magnetic coupling via bond wires.. The "white space" between the analog blocks and the noisy areas like digital cores, output buffers provides additional isolation from the "technical noise". The same design rules should be valid for the whole pc-board layout of the oscillator.

The admitted level of sub-harmonics and spurious suppression for UHF band signal can be evaluated by the equations which describes a phase harmonic modulation. This evaluation has been considered in paper [5]. The obtained result shows that in order to attain phase deviation less than 0.01 radian, spectral amplitude of the disturbing component should not exceed -45 dB of the output signal level

III. Circuit description

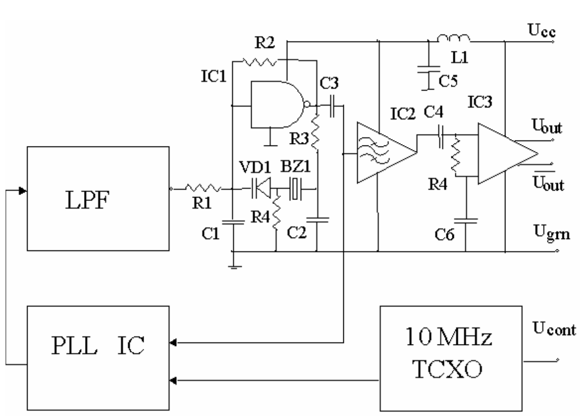

Fig.1. The simplified TCXO schematic, where: IC1-CMOS nAND Gate, VC2-resonance amplifier, IC3-output buffer.

The simplified TCXO schematic for 1 GHz output frequency signal is shown in Figure 1. The oscillator stage is a Gate type circuit and it generates at frequency f_0 = 200 MHz. The stage contains a third overtone A-cut "inverted mesa" quartz crystal. Advanced Silicon CMOS fabrication of Gate IC provides high speed operation (propagation delay < 2.5 ns) and can produce long series of the signal harmonics. The harmonics set decreases in power from 10 dBm at f_0 frequency to –21 dBm at 1 GHz. So it's possible to select a required harmonic from this spectrum. The decupling filters between stages allow to reduce the suppression requirements for filtering stages. This structure of VCXO allows to use the harmonic selection technique which was developed for UHF VCXO [6].

The second stage of the oscillator is a narrow band amplifier, which is also tuned on the required output frequency . To obtain a good spectral purity of VCXO output signal, it is necessary to pay attention to isolating of the frequency multiplication stage from the filtering and the output buffer stages to avoid an excessive amplification in device circuit. The power-supply decoupling of all the stages is essential as well.

The buffer stage is a PECL differential receiver /driver with Enable/Disable feature. This IC provide Q and invert Q PECL output signals. The oscillator has a frequency pull-ability of ±15 ppm in the voltage control range of 1.5V ± 1.0V. The device is packaged in FR-5 based SMD 20 x 18.5 x 3.6 mm^3 case

IV. Measurement results

The plots of the phase noise spectral density L_φ *(f)* (single side band) versus frequency offset *f* are presented on Figure 2. The bottom curve belongs to 200 MHz TCXO signal, which doesn't use the frequency multiplication technique. The upper curve describes the phase noise of 1GHz TCXO signal. The total frequency multiplication factor *N* in this cases is 5 and a degradation ΔS_φ due to the frequency multiplication equals:

$$\Delta S_\varphi = 20 \log N = 20 \log 5 = 17 \text{ dB}. \quad (4)$$

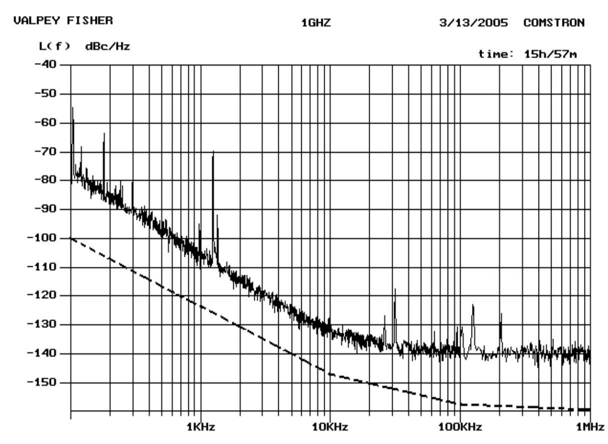

Fig. 2. The power spectral density of the phase noise.

The phase noise plots show good argument with the expression (4). Presented dash line curve shows high value of the loaded Q-factors of a third overtone quartz resonator at 200MHz carrier frequency (about 20 thousand). This value approaches to unloaded Q-factor for AT-cut inverted mesa crystal resonators at that frequency band. The enlarge of the noise on the floor for 1.0 GHz signal at the offset larger than 100 kHz is due to the additional phase noise of the output PECL buffer.

The plot of TCXO frequency stability over temperature is presented on Figure 3.

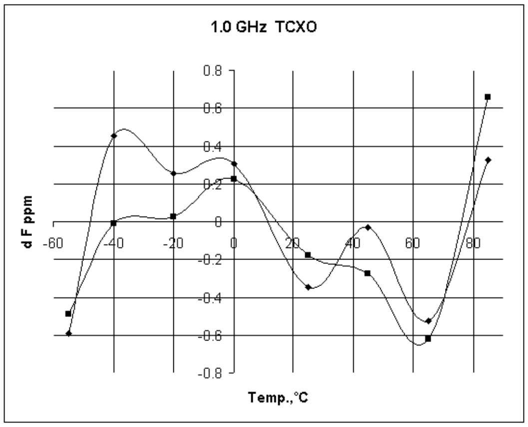

Fig. 3. The dependence of frequency stability Δf over temperature *t*.

The dependence of the frequency stability Δf over temperature *t* is "compensated" cubic function of *t*. This dependence shows that the frequency stability does not exceed ±1 ppm in operating temperature range of –40 to + 85 °C.

The spectrum of output signal is shown on Figure 4.

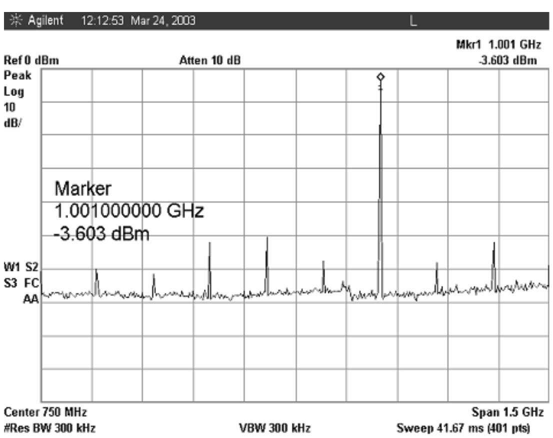

Fig. 4. The spectrum of TCXO output signal.

The suppression of sub-harmonics and their multiples is better than 49 dB with respect to the 1Ghz signal level.

The spectral purity of TCXO signal is shown on Figure 5

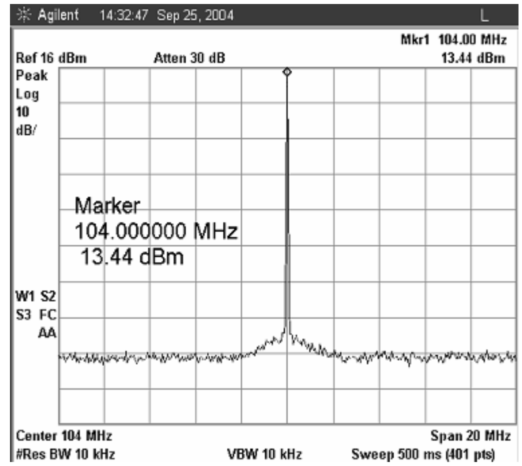

Fig. 5 . The spectrum of TCXO signal in a realm near to the carrier.

The TCXO output spectrum in a vicinity of the carrier shows a good suppuration. comparison frequency signal

V. CONCLUSIONS

The frequency translation technique has allowed expanding the operation realm of low phase noise TCXO to UHF band. This TCXO architecture has permitted to combine the good temperature stability and low phase noise in a small SMD package device. The disadvantages of the PLL application was overwhelmed by maintaining high loaded Q-factor of VCXO crystal and by minimizing the "technical" noise injection. The TCXO output signal has an excellent spectral purity –85 dBc. The overall frequency stability does not exceed ± 1 ppm over temperature with good aging and tight initial calibration, provided by the low frequency reference.

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