A NEW DIGITAL PHASE MEASUREMENT SYSTEM

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Abstract

The Naval Research Laboratory (NRL) is developing a digital phase measurement system. The measurement system uses high speed Analog to Digital Converters (ADC) to make tens of millions of measurements per second, Digital Signal Processing (DSP) hardware for intermediate calculations, and a PC for the final phase calculations. Performance of the present configuration is limited by a 12-bit analog-to-digital converter. Averaging times can be as small as 0.0001 seconds. Multiple input frequencies to over 10 MHz can be measured simultaneously. Modular construction will allow for expansion to many channels. Absolute phase measurements are possible. Inputs to channels can be switched between frequencies and then returned to an original frequency without losing phase coherency of the measurements. This system to be used in the laboratory and may be used on the GPS satellites to monitor a hot backup clock. The basic system measures the coefficient of a Discrete Fourier Transform (DFT) at the assumed frequency of the input signal. This paper will describe the special purpose DSP hardware and software used to measure the signal and transform the measurements into conventional clock parameters.

SYSTEM DESCRIPTION

Figure 1 is a block diagram of the basic hardware module used in this system. It consist of an ADC, a Numerically Controlled Oscillator (NCO), two digital multipliers, and two digital accumulators or Complex Multiplier Accumulator (CMAC). An analog sine wave at a frequency, Fs, is sampled and quantized with an ADC at a rate determined by the sampling clock, Fc. Typically for best performance Fs < .4 Fc. The NCO, sometimes referred to as Direct Digital Synthesis (DDS), generates two digital reference sine wave signals in quadrature at a frequency Fr very near Fs at a rate of Fc. The two sine waves represent a complex wave with the cosine part representing the real part and the sine representing the imaginary part. The real part is referred to as the I for Inphase and the imaginary as Q for Quadrature. The output of the ADC is multiplied by both the I and Q outputs of the NCO in two multipliers. This multiplication acts as a mixer translating the Fs by Fr to close to zero. The CMAC

accumulates the product, typically for 512 cycles. The number of CMAC accumulation cycles is called N_CMAC. If Fc is 25 MHz, the rate of CMAC accumulator outputs will be approximately 48.8 kHz and can easily be handled by programmable software operations. After accumulation, the results are transferred to the computer, and the CMAC accumulators are reset to zero without missing a cycle. The NCO and CMAC are contained in a HSP45116 chip from Intersil and the ADC is an Analog Devices AD9042.

Additional accumulations occur in software for N_SOFT cycles. The total number of effective accumulation cycles is N = N_CMAC * N_SOFT. The total accumulation results in a processing bandwidth of Fc / N.

The output of the multiplication and accumulation process is:

$$S = 32767 \quad A/2 \{ e^{j(-\beta+\alpha)} \text{SIN}(N \pi (Fs-Fr)/Fc) / \text{SIN}(\pi (Fs-Fr)/Fc) + e^{j(-\beta-\alpha)} \text{SIN}(N \pi (Fs+Fr)/Fc) / \text{SIN}(\pi (Fs+Fr)/Fc) \}$$

$$S = A \ (32767 / 2) \{ e^{j(-\beta+\alpha)} G\_D + e^{j(-\beta-\alpha)} G\_S \}$$

(see Appendix #1) where N = total number of accumulations; i = Sample index, $-(N - 1) / 2 \geq i \geq (N - 1) / 2$; t = Time; t = i / Fc; and Fc = Sampling frequency.

Signal to ADC = $A \cos(2 \pi (Fs\ t + \alpha)) = A \cos(2 \pi (i\ Fs/Fc + \alpha))$; A = Signal Amplitude; Fs = Signal Frequency; α = Signal Phase at or i = 0.

Reference = $36767\ e^{-\{ j [2 \pi (Fr\ t + \beta)] \}}$; Fr = Reference Frequency (NCO);β = Reference Phase at i = 0.

Two frequency dependent gains are defined as:

$$G\_D = \text{SIN}(N \pi (Fs-Fr)/Fc) / \text{SIN}(\pi (Fs-Fr)/Fc)$$
$$G\_S = \text{SIN}(N \pi (Fs+Fr)/Fc) / \text{SIN}(\pi (Fs+Fr)/Fc)$$

G_D and G_S are the gains at the sum and difference frequencies and are both real numbers. As Fr approaches Fs, G_D approaches N. The gain terms can be used to evaluate the attenuation of other additional input signals such as harmonics, bias and noise. G_D also shows the effect of tuning errors, Fs-Fr.

Two phase shifts terms are $e^{j(-\beta+\alpha)}$ and $e^{j(-\beta-\alpha)}$.

The difference in phases at the center of the integration period is $-\beta+\alpha$. This is the primary piece of information that the hardware measures. The selection of the range of i, i = 0 in the center of the accumulation, was to simplify the phase part of the equation for S. The time needed to collect the data is N/Fc. If $|G\_D| >> |G\_S|$, the phase shift in cycles of S between accumulations is N (Fs – Fr) / Fc. This phase shift between outputs can be used to estimate Fs, G_D and G_S. This phase shift is also a term in G_D.

QUANTIZATION AND PERFORMANCE

Quantization due to the digital implementation occurs in several areas, such as the ADC, tuning the NCO, the number of bits used to address the Sine/Cosine table, the precision of the Sine/Cosine table output, and the effects of the multiplier accumulator (Figure 1).

The Sine/Cosine table uses 20 bits for an address and generates a 16-bit output. Because of two's complement representations in the hardware, the value of the sine table a function of the address is

$$\text{Table output} = \text{Nearest Integer}\ [\ 32767\ \ e^{(J\ \pi\ \text{Address}\ /\ 1048576)}]$$

The address goes from 0 to $2^{20} - 1$ in order to represent one full cycle of a sine wave. The largest positive number that can be expressed with a 16 bit signed integer is 32767. The maximum slope of the Sine/Cosine table is approximately $2\ \pi\ 2^{15} / 2^{20} = .196$. The table's input quantization effects are about 5 times smaller than the table's output quantization effects and will be negated.

The ADC has 12 bits of precision and may be increased to fourteen bits in the future. The output of the ADC is multiplied by the output of the Sine/Cosine table and accumulated. There is no quantization in the multiplier and accumulator, because there is no rounding or truncation. The precision of the product and accumulation is principally determined by the precision of the 12- or 14-bit ADC, and not by the 16 bits of the output of the Sine/Cosine table; therefore, the effects of the quantization of the output of the Sine/Cosine table will be negated. Only the quantization effects of the ADC and the NCO tuning will be analyzed.

Effects of NCO tuning are shown in the equation for S in the difference between Fs and Fr. If D equals the number of bits in the phase accumulator of the NCO, the tuning step of an NCO is $Fc/\ 2^{32}$. The maximum tuning error is half a step or .00291 Hz if Fc = 25 MHz and D=32.

The Signal-to-Noise Ratio (SNR) of the ADC is calculated by assuming the ADC quantization effects produce a white noise spread over the frequency range ± Fc / 2, and that the signal is processed with a noise bandwidth of Fc / N . If N (Fr – Fs) / Fc is small, or G_D ≈ N, the SNR of the ADC and accumulation process is

$$\text{SNR} = 3/4\ \ N\ \ (R\ \ 2^{B})^{2}$$

where B = number of Bits in a perfect ADC; R = A / (maximum input to ADC) (see Appendix #2).

SUM FREQUENCY DISTORTION

The effects of G_S on S can be greater than the effects of quantization in the ADC. The ratio of $(G\_D / G\_S)^2$ can be looked upon as an SNR to compare it with the ADC's SNR. If (.1 Fc) < Fs < (.4 Fc) , G_S will never be greater 1 / Sin (.2 π) = 1.701. This puts a worse case limit on G_D / G_S of .5877 N if G_D = N. If N is large enough, the effect of G_S will be less than the quantization of the ADC, but the value of N forces the processing bandwidth to be greater than a .01 Hz.

One method to reduce the effects of G_S is to offset Fr from Fs such that N (Fs + Fr) / Fc is close to an integer. This places G_S near a null, but may also reduce the value of G_D from N by up to ½. This method will reduce the effects of G_S to less than the ADC quantization. The minimum value of G_D / G_S is determined by how close N (Fs + Fr) / Fc is to an integer. $|G\_D / G\_S| > 2^{(D-1)}$ (See Appendix #3).

A second method is to pass the analog sine wave through a quadrature network and use two ADC's. This method generates a complex sine wave to the CMAC, with only a positive frequency component. This also requires the multiplier to perform a complete complex multiplication. If this is done perfectly, then

$$S = 32767\ A\ e^{j(-\beta+\alpha)}\ G\_D$$

It is felt that balance required in the quadrature and in the pair of ADC's circuit required to reduce the negative frequency component is not practical. The CMAC hardware supports dual ADC's inputs and a complete complex multiplication (Figure 2).

A third method is based on the known relationship between G_D and G_S, and $e^{j(-\beta+\alpha)}$ and $e^{j(-\beta-\alpha)}$. Fs can be estimated from two hardware measurements, and β can be calculated from hardware instrumentation. Then G_D and G_S can be estimated from Fs. The effects of G_S can be reduced leading to better estimates of phase. The hardware supports knowledge of β (see Appendix #4).

With proper processing, the effects of G_S can be removed, and the limiting factor in performance will be the ADC, assuming that the number of bits is 14 bits or less. Figure 3 shows the limit of the ADC's, the worse case effects of the G_S if uncorrected, and the level G_S if it is nulled by tuning. Figure 4 is the output of a simulation with all quantization effects.

ADDITIONAL PROCESSING

The first step in processing, if the sum frequency is stronger than the ADC quantization, and not nulled, is to remove the sum frequency as described above.

The modified I and Q can be used to calculate magnitude and phase. The Magnitude is $\sqrt{(I^2 + Q^2)}$ and the phase is ATAN2 (Q , I) / (2π) cycles, where ATAN2 is a double argument arctangent subroutine that produces an angle between $\pm\pi$. Phase rollovers must be removed. An assumed value of Fs called Fa will be used to calculate the expected phase shift between accumulations or N (Fa – Fr) / Fc. This is usually less than .5 cycle. The new phase must be modified by an integer number of wavelengths to match the old phase plus the expected phase change.

An additional correction is needed to correct tuning errors, or the difference in Fr and the assumed frequency Fa. Fr may be set to Fs, or it may be set to null G_S.

The phase in cycles must be expressed in time by dividing the phase in cycles by Fa to compare signals at two different frequencies.

HARDWARE CONFIGURATIONS

The simplest system compares the signal to the ADC USING the clocking signal. Multiple signals can be compared by using a common clocking signal to multiple basic units. Analog signals of different frequency can be easily compared by looking at the differences in their phases. With this configuration, the effect of the clocking frequency is common and will be reduced. The clocking frequency could come from a free-running oscillator. When two or more signals of the same frequency are compared, the NCO's and accumulators can be synchronized. However, this will cause some quantization errors to be common to both measurements (Figure 5).

The NCO's currently in use have 32-bit phase accumulators. If the tuning command to the NCO is constant, the phase of the NCO will repeat every 2^{32} clocks, independent of the tuning command. The system has a 32-bit master sync counter that counts cycles of the sampling signal. If Fc is 25 MHz, this

counter will rollover about every 171 seconds. All NCO phase accumulators can be zeroed by this rollover. NCO tuning changes can be synchronous with this rollover. The start of the accumulation cycles in the CMAC can be synchronous with rollover. The number of accumulation cycles in the CMAC should be a power of two, if the accumulation is synchronous with the rollover. The value of the master sync counter is saved at the end of each accumulation. This value can be used to calculate the NCO phase β. The absolute phase difference of two analog signals can be measured with the synchronization hardware.

With the use of an analog or digital multiplex, it would be possible to switch between multiple signals and make phase coherent measurements. Then short-term measurement capability would be lost with this method.

Square wave inputs can be used, but they must be connected to the clocking signal and must be compared with a sine wave connected to the analog input. Multiple basic units can have only one square wave input, and it is common to all basic units.

ANALOG BANDWIDTH

The analog signal need not be filtered, if it is a sine wave. The digital processing bandwidth will in most cases be significantly narrow, typically 1 kHz or less, which is smaller than the analog bandwidth. Low pass filters can keep high frequency noise from aliasing into the lower frequency spectrum.

Wideband analog noise can be an advantage. If the signals are noise free and Fc and Fs are coherent, data from the ADC will repeat. The additional of a small random noise to Fs or Fc will give digital samples a small random variation. This will improve the performance as long as this noise is small compared to the ADC quantization noise.

SYSTEM RESTRICTIONS

The analog signals are assumed to be sine waves. Information is obtained by sampling during the rise and fall of the signal. A perfect square wave at the analog input would not supply any information during the rise or fall.

The sampling signal and the analog signal should be non-coherent. If the signals were noise free, and the frequency ratio could be expressed as the ratio of two small integers, the numbers out of the ADC would repeat, and the processing gain would be determined by the unique set of samples.

Under normal operations $Fs < \frac{1}{2}\ Fc$. If this is not true, the equations for G_D and G_S are still correct. The NCO will be tuned to the correct frequency, because the hardware will only accept the 32 least significant bits of the tuning word.

STATUS

At this time, a bench top prototype system has been assembled. It consists of a DSP board plugged into a PC, a board that contains the CMACs, and two analog-to-digital converter boards. The prototype has

some noise problems that contribute to worse than expected results. No shielding was provided for the ADCs. The prototype was useful in designing the functionality of the system.

APPENDIX # 1 CALCULATION OF S

$S = \sum$ Signal(i) Reference (i)
i = Sample index, $-(N-1)/2 \geq i \geq (N-1)/2$
where
i = t Fc
t = Time
Fc = Sampling Frequency
N = total number of accumulations

Signal to ADC = $A \cos(2\pi(Fs\,t + \alpha)) = A \cos(2\pi(i\,Fs/Fc + \alpha))$
A = Signal Amplitude
Fs = Signal Frequency
α = Signal Phase at i = 0

Reference = $36767\, e^{\{-j[2\pi(Fr\,t+\beta)]\}} = 36767\, e^{\{-j[2\pi(i\,Fr/Fc+\beta)]\}}$
$32767 = 2^{15} - 1$, the largest positive that can be expressed by signed 16-bit integer.
Fr = Reference Frequency (NCO)
β = Reference Phase at i = 0

$$S = 32767 \sum_{i=-(N-1)/2}^{i=(N-1)/2} A \cos(2\pi(i\,Fs/Fc + \alpha))\, e^{\{-j(2\pi(i\,Fr/Fc+\beta))\}}$$

$\cos x = \frac{1}{2}(e^{jx} + e^{-jx})$

$$S = 32767/2\, e^{(-j\beta+\alpha)} \sum_{i=-(N-1)/2}^{i=(N-1)/2} A\, e^{\{j(2\pi i(Fs-Fr)/Fc)\}} + 32767/2\, e^{(-j\beta-\alpha)} \sum_{i=-(N-1)/2}^{i=(N-1)/2} A\, e^{\{-j(2\pi i(Fs+Fr/Fc)\}}$$

Sum of N terms of a geometrical progression, "middle term" = 1,
X = common ratio , first term = $X^{(-(N-1)/2)}$

$$\sum_{i=-(N-1)/2}^{i=(N-1)/2} X^i = X^{(-(N-1)/2)}(X^N - 1)/(X - 1)$$

$$= [X^{(N/2)} - X^{-(N/2)}] / [(X^{1/2} - X^{-1/2})]$$

If $X = e^{j\phi}$

$$\sum_{i=-(N-1)/2}^{i=(N-1)/2} e^{j\phi i} = SIN(N\phi/2) / SIN(\phi/2)$$

If $\phi = 2\pi (Fs - Fr / Fc)$

$i = (N - 1) / 2$
$\sum_{i=-(N-1)/2} e^{j\phi i} = SIN (N\pi (Fs-Fr)/Fc) / SIN (\pi (Fs-Fr)/Fc)$

If $\phi = 2\pi (Fs+Fr/Fc)$

$i = (N - 1) / 2$
$\sum_{i=-(N-1)/2} e^{j\phi i} = SIN (N\pi (Fs+Fr)/Fc) / SIN (\pi (Fs+Fr)/Fc)$

$S=A/2\{e^{(-j\beta+\alpha)}SIN(N\pi(Fs-Fr)/Fc)/ SIN(\pi(Fs-Fr)/Fc)+e^{(-j\beta-\alpha)}SIN(N\pi (Fs+Fr)/Fc)/ SIN (\pi(Fs+Fr)/Fc)\}$
$G\_D = SIN (N \pi (Fs-Fr)/Fc)/ SIN (\pi (Fs-Fr)/Fc)$
$G\_S = SIN (N \pi (Fs+Fr)/Fc)/ SIN (\pi (Fs+Fr)/Fc)$
$S = A/2 \{ e^{(-j\beta+\alpha)} G\_D+e^{(-j\beta-\alpha)} G\_S\}$

APPENDIX # 2 ADC QUANTIZATION SNR

B = Number of ideal ADC bits (including sign bit)
R = Ratio Peak Sine Wave Voltage / (Maximum ADC signal), $R \leq 1$
Fs = Signal Frequency Fc = Sampling Frequency
N = Number of independent samples

Assume a 1 ohm system
Assume Maximum level of ADC = ±1

Total Signal energy = $(R^2)/2$
Signal energy at + Fs = $(R^2)/4$
Signal energy at - Fs = $(R^2)/4$

Quantization voltage of ADC is $2^{-(B-1)}$
RMS Quantization voltage of ADC = $2^{-(B-1)} / \sqrt{12}$
Quantization Energy = $2^{-2(B-1)}/12 = 1 / (3\ 2^{2B})$
Assume quantization energy spread equally between ± Fc/ 2
Quantization energy density = $1 / (3\ Fc\ 2^{2B})$

Integration Time = N / Fc
Processing Bandwidth = Fc / N
Quantization energy in processing bandwidth = $1 / (3\ N\ 2^{2B})$
Signal to Noise Ratio = $3/4\ N\ (R\ 2^B)^2$

APPENDIX #3 NULLING OF G_S, OR G_D / G_S

$G\_D = SIN (N\pi (Fs-Fr)/Fc) / SIN (\pi (Fs-Fr)/Fc)$
$|G\_D| > .5\ N$

$G\_S = SIN(N\pi (Fs+Fr)/Fc) / SIN(\pi (Fs+Fr)/Fc)$
D = Number of bits in NCO phase accumulator
Maximum error in (Fs+Fr) / Fc from a null is $1 / 2^{D+1}$
$|SIN(N\pi (Fs+Fr)/Fc)| < N\pi / 2^{D+1}$
if (.1 Fc) < Fs < (.4 Fc) THEN $|SIN(\pi (Fs+Fr)/Fc)| > .5$
$|G\_D/G\_S| > 2^{31}/\pi$

APPENDIX #4 REMOVAL OF G_S FROM S

From two hardware measurements an estimate of Fs can be made and approximate values of G_D and G_S can be calculated.

$S = A/2\ G\_D\ e^{j(+\theta-\beta)} + A/2\ G\_S\ e^{j(-\theta-\beta)}$

$S = A/2\ e^{j(-\beta)} [G\_D\ e^{j(\theta)} + G\_S\ e^{j(-\theta)}]$
β is known from the hardware
$S\ e^{j(\beta)} = A/2 [G\_D\ e^{j(\theta)} + G\_S\ e^{j(-\theta)}]$
$REAL(S\ e^{j(\beta)}) = A/2 [\{G\_D+G\_S\}\cos(\theta)]$
$IMAGINARY(S\ e^{j(\beta)}) = A/2 [\{G\_D-G\_S\}\sin(\theta)]$
$A/2 \cos(\theta) = REAL\ (S\ e^{j(\beta)})/\{G\_D+G\_S\}$
$A/2 \sin(\theta) = IMAGINARY(S\ e^{j(\beta)})/\{G\_D-G\_S\}$
$\tan(\theta) = [A/2 \sin(\theta)] / [A/2 \cos(\theta)]$
$\theta = \arctan2\ [IMAGINARY(S\ e^{j(\beta)}/\{G\_D-G\_S\}), REAL(S\ e^{j(\beta)}/[\{G\_D+G\_S\})]$

$A = 2\ |S/[G\_De^{j(\theta)} + G\_Sej^{(-\theta)}]|$
$A \approx 2\ |S|/[G\_D]$
$A \approx 2\ |S|/N$
An iteration can be done to improve using the value of θ.

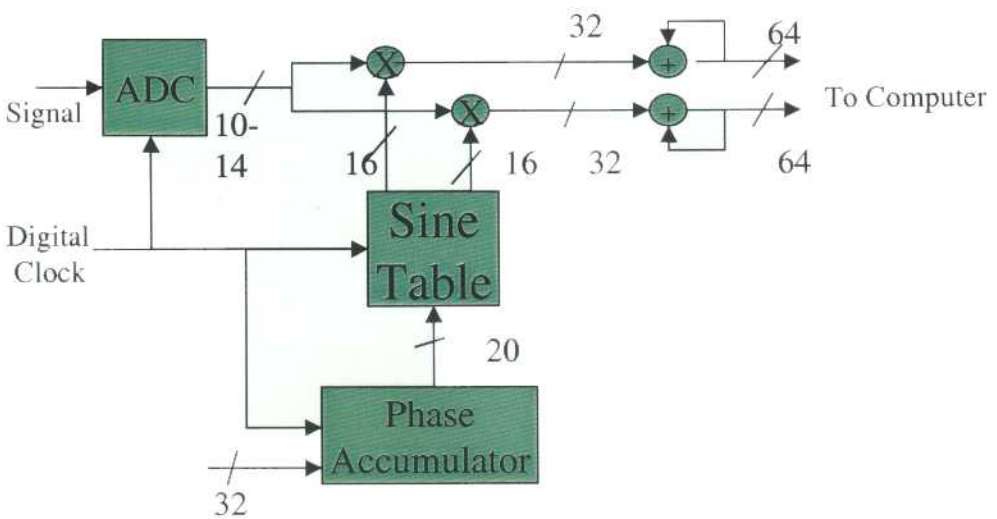

Figure 1
Basic unit Block Diagram Showing Digital Bus Width

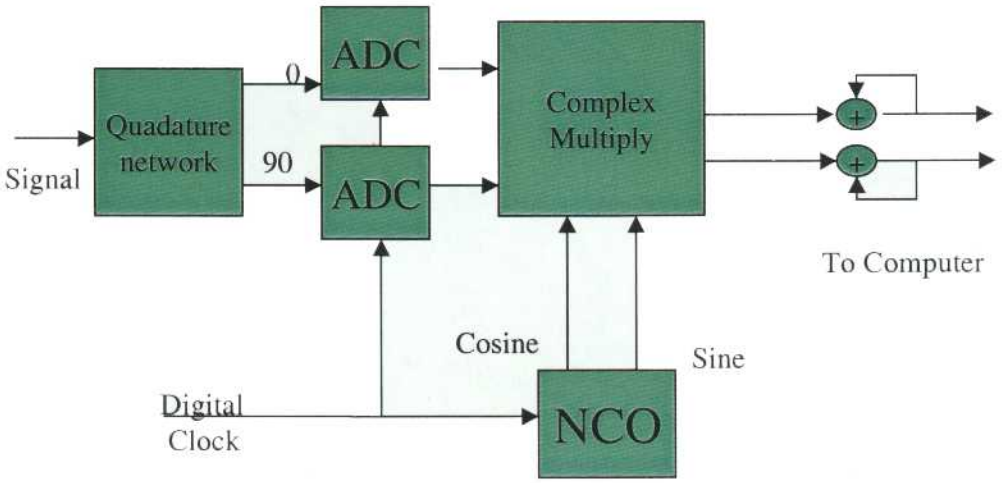

Figure 2
Basic Unit With Quadature ADC's

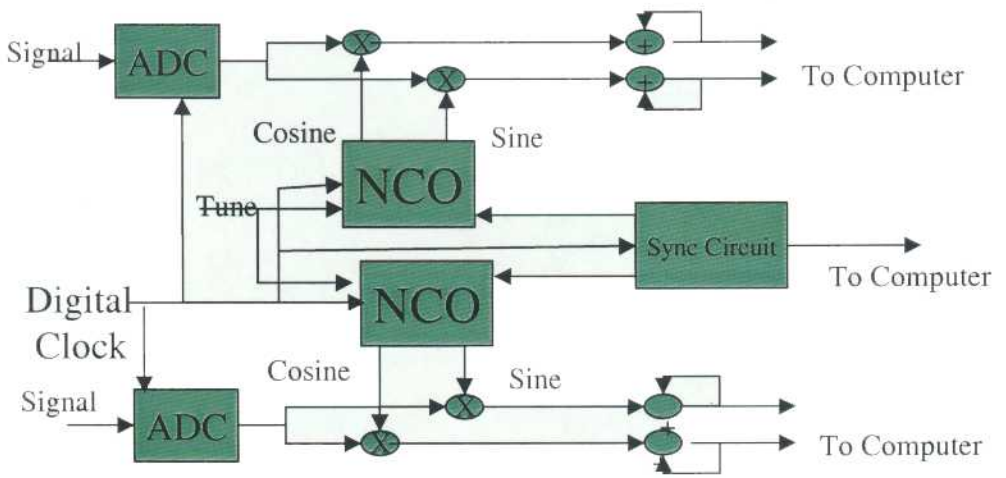

Figure 3
Dual Mixer Configuration

Fig. 4 RESOLUTION vs DATA COLLECTION TIME, Fc ~25mhz, Fs ~ 5mhz

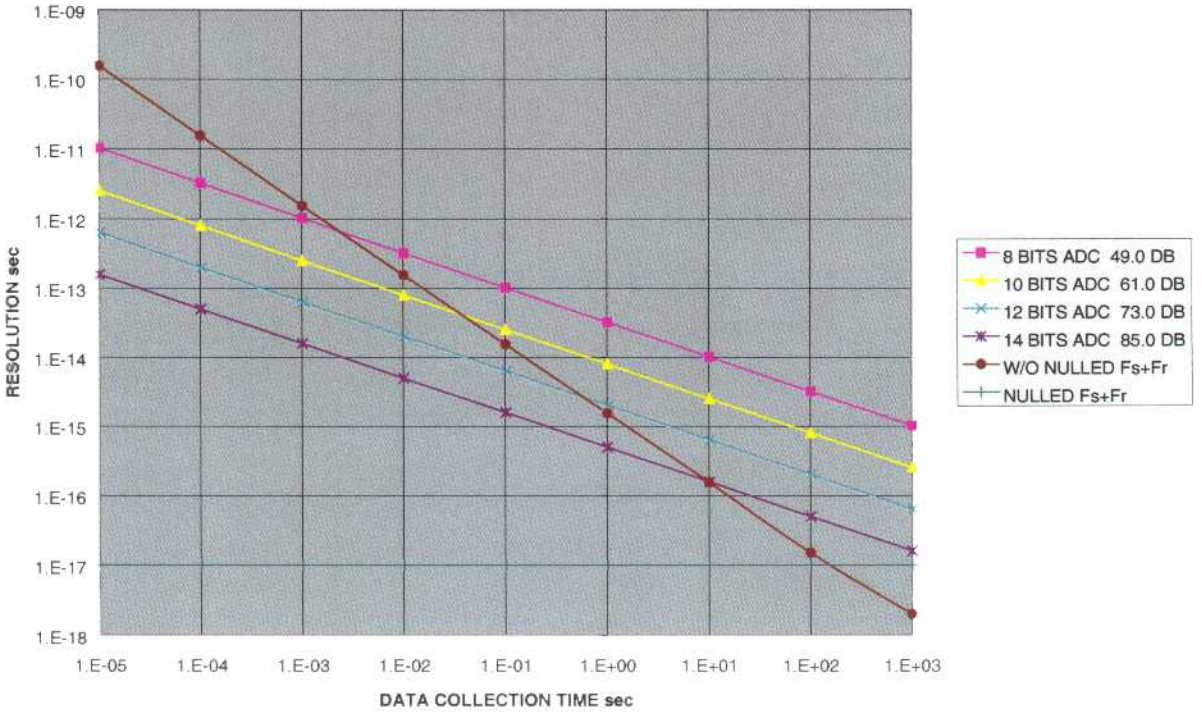

Fig. 5 Simulated TDIF Fc ~ 25mhz, Fs ~ 5 mhz,
Data collection time = .001 sec,
12 Bit ADC