ROBUST GPS-BASED SYNCHRONIZATION OF CDMA MOBILE NETWORKS

Dominik Schneuwly
Oscilloquartz SA
Brévards 16, CH-2002 Neuchâtel, Switzerland
Tel: +41 32 722 55 67; Fax: +41 32 722 55 56
E-mail: *schneuwly@oscilloquartz.com*

Abstract

Mobile communication networks based on the cdmaOne and cdma2000 standards require that the base-stations of their radio access networks be synchronized. All the base-stations of the network need a 1PPS phase reference with an accuracy of 3 μs. The Global Positioning System (GPS) is currently the only practical way of implementing this type of synchronization. This paper proposes a two-fold protection concept for the base-station's phase clock. In case of a GPS-reception problem, the phase reference signal is maintained using the auxiliary frequency reference signal taken from the SONET (Synchronous Optical Network) transport network. When the latter fails (double failure), the clock eventually enters holdover mode. The paper analyzes the performance of the two protection modes, and compares it to the requirements of CDMA-based mobile networks.

INTRODUCTION

Third Generation (3G) mobile communication networks are currently being deployed in several countries. These new networks will eventually replace today's D-AMPS and GSM mobile telephony networks. 3G networks will bring new services such as Internet access and multimedia applications. These new services are made possible by the higher data rates provided by 3G technologies. The term 3G actually includes a family of different mobile communication technologies. cdma2000 is one of these 3G technologies. cdma2000 is an evolution of the already existing cdmaOne. Networks based on the cdmaOne and cdma2000 standards require that the base-stations of their radio access networks be synchronized. All the base-stations need a 1PPS (1 Pulse Per Second) phase reference with an accuracy of 3 μs. This phase-synchronization is required in order to support handover of a connection when the user moves from one radio access network cell to another. During this move, the connection must be handed over from the base-station of the first cell to the base-station of the second cell.

The Global Positioning System (GPS) is currently the only practical way of implementing this type of synchronization. This means that all base-stations of a cdma network must be equipped with a GPS-receiver capable of delivering a 1PPS signal with a 3 μs accuracy. This is easily achieved with GPS – most GPS-receivers optimized for timing provide accuracies in the range of 20 to 100 ns. Mobile communication networks also require a high degree of availability, since safety-critical user applications rely more and more on public mobile networks. Although the GPS has an excellent system availability track record, there is a real possibility of radio interference at some base-station sites. In order to protect a base-station against failures caused by radio interference problems, the base-station's clock must be able to provide the 1PPS phase reference for some time under failure conditions affecting the satellite to receiver chain. The usual way of achieving this is by using the base-station clock's holdover mode. An alternative is to use a clock that can be slaved not only to the GPS as a primary reference, but also to an auxiliary

external signal. This additional signal is extracted from the transport network. SONET (Synchronous Optical Network) transport networks work with frequency-synchronous optical carrier signals. The idea is to derive a frequency reference signal from that optical carrier, and to use this reference to drive the base-station clock in case of failing GPS-reception. The base-stations clock has three operation modes:

1) Phase-locked Mode (PM): the clock is phase-locked to the GPS-receiver;
2) Frequency-locked Mode (FM): the clock is locked to an external frequency reference signal;
3) Holdover Mode (HM): the clock runs on its internal oscillator.

These operation modes provide a double protection for the base-station's phase reference signal, i.e. for the 1PPS signal. In case of a GPS-reception problem, the phase reference signal is maintained using the auxiliary frequency reference signal (Frequency-locked Mode). When the latter fails (double failure), the clock eventually enters Holdover Mode. An interesting question is: "For how long can the required 1PPS accuracy be maintained under failure conditions?" This depends mainly on the stability of the frequency reference signal derived from the transport network, and the holdover performance of the internal oscillator.

CLOCK STRUCTURE

Figure 1 shows the logical block diagram of a GPS clock providing the three operation modes mentioned earlier. The blocks shown in the diagram have the following functions:

G. R.	GPS receiver; delivers a 1PPS signal.
INT	Interface for the frequency reference signal coming from the transport network; derives a 1PPS signal from the input signal, which typically comes with a rate of 1544 kbit/s.
P. S.	Phase Shifter; the phase shifter adds a delay to the 1PPS signal derived from the frequency reference signal; this delay is adjusted by the Phase Shift Controller PSC, so that the delayed 1PPS signal is always in phase with the PPS signal coming from the GPS-receiver.
PSC	Phase Shift Controller; see above.
MEM1	This digital memory continuously stores the control information used to steer the Phase Shifter; this control information is used in case of failure of the 1PPS coming from the GPS receiver.
Switch 1	This switch is normally in the left position (Phase-locked Mode); in case of failure of the 1PPS coming from the GPS receiver, the switch selects the output of the memory as the new control signal for the Phase Shifter; this switchover puts the system into Frequency-locked Mode.

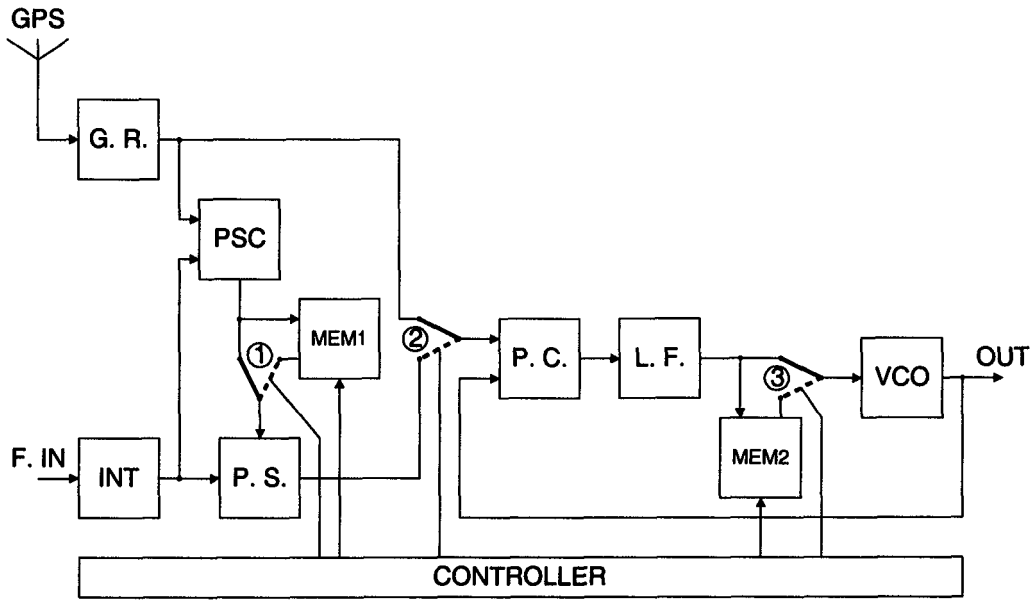

Figure 1: GPS receiver with Phase-locked, Frequency-locked, and Holdover Modes.

Switch 2	This switch is in the upper position in Phase-locked Mode, and in lower position in Frequency-locked Mode.
P. C.	Phase comparator; it measures the phase difference of the 1PPS signal coming from the front end, and the 1PPS signal fed back from the clock's output; the phase comparator is part of a conventional Phase Locked Loop (PLL).
L. F.	This is the PLL's loop filter.
VCO	This is the internal oscillator; normally, i.e. in all operation modes except in Holdover Mode, the VCO is part of the loop forming the PLL.
MEM2	The second digital memory stores the control signal that normally steers the VCO; in case the system enters Holdover Mode, the last stored control signal value is applied to the VCO.
Switch 3	This switch is in upper position when the system is in Phase-locked or Frequency-locked Mode; moving the switch to the lower position causes the system to enter Holdover Mode.

The important point in the block diagram is the presence of the two digital memories. There is one used for holding information about the last measured phase (MEM1), and another one for holding information about the last measured frequency (MEM2). The value stored in MEM1 is used when the system switches from Phase-locked Mode to Frequency-locked Mode. The stored value is applied to the phase shifter, in order to make sure that the 1PPS signal at its output is in phase with the GPS. The value stored in MEM2 is used when the system enters Holdover Mode. The stored value is applied to the VCO, in order to make sure it generates the same frequency as it was locked to just before the switchover event.

SYNCHRONIZATION AUTONOMY

The interesting question is: "For how long can the required 1PPS accuracy be maintained under failure conditions?" The question must be answered separately for the Frequency-locked and the Holdover Mode.

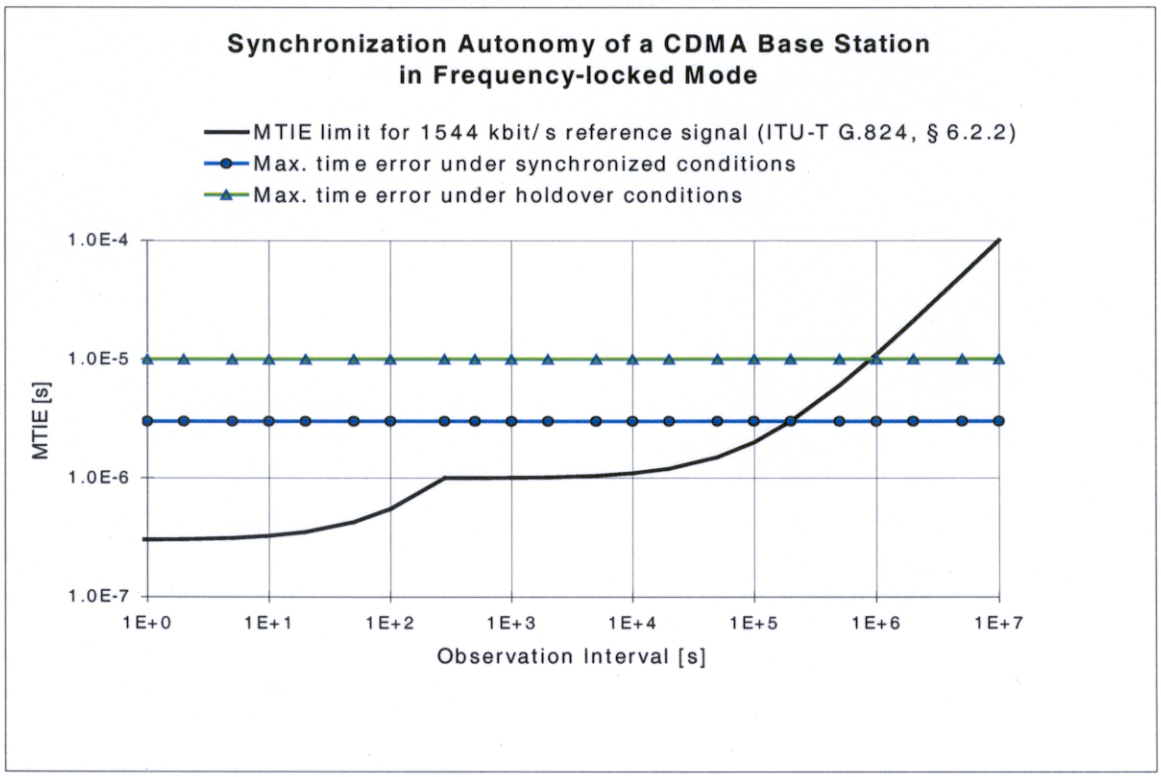

Figure 2: Synchronization Autonomy in Frequency-locked Mode.

In the Frequency-locked mode, the signal is initially in phase with the GPS. With time, however, some time error accumulates. If the frequency reference signal is taken from the SONET transport network, the accumulating time error can be expected to be below the standard limits specified for SONET. Figure 2 shows the so-called Network Limit according to ITU-T Recommendation G.824. The Network Limit is expressed as an MTIE (Maximum Time Interval Error) curve. The asymptotic behavior of the curve for long Observation Intervals is linear and corresponds to a maximum frequency error of 1×10^{-11}. As mentioned before, cdma base-stations normally require a 3 μs accuracy on the 1PPS signal. As can be seen in the figure, the Network Limit crosses the 3 μs level after 200,000 seconds, which corresponds to 56 hours. The figure also shows the cdma specification for degraded operation under holdover conditions. One can see that in Frequency locked mode this limit would be reached only after 900,000 seconds, i.e. after 10 days.

In Holdover Mode, the autonomy period is much shorter. It depends mainly on the quality of the internal oscillator and on the temperature conditions.

The two most important oscillator specifications relevant for the holdover performance are the frequency drift due to ageing and the frequency deviation due to temperature variations. According to cdma standards, the time error on the 1PPS signal is allowed to reach 10 μs in Holdover Mode. Figure 3 shows the relationship between oscillator quality and the autonomy period determined by the 10 μs limit. Each curve in the figure stands for a given autonomy period. The curve actually shows the possible combinations of the oscillator's ageing and temperature specifications leading to the given autonomy period. The curves were obtained starting from the well-known formula for the accumulation of phase-time in Holdover Mode:

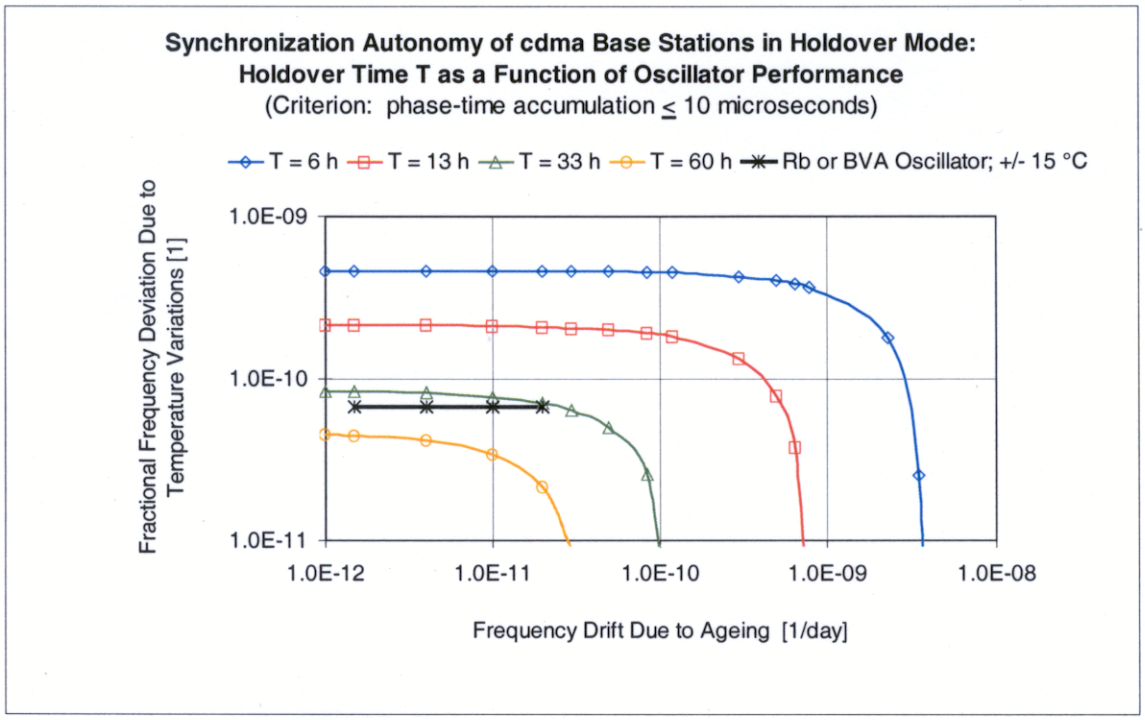

Figure 3: Synchronization autonomy in Holdover Mode.

$$x = y_Q \times T_{HO} + \frac{b \times T_{HO}}{2}$$

where:

x = accumulated phase-time

y_Q = fractional frequency deviation due to temperature

T_{HO} = holdover time period

b = frequency drift due to ageing

It follows that:

$$y_Q = \frac{x}{T_{HO}} - \frac{b \times T_{HO}}{2}$$

In order to find out what autonomy can be achieved realistically, the specifications of typical oscillators are added to the diagram. The horizontal line just underneath the 33 h curve covers state-of-art rubidium and BVA quartz oscillators. The typical frequency deviation over a temperature range of ± 15°C is 7×10^{-11} for both the rubidium and BVA quartz oscillators. The frequency drift due to ageing ranges from 1.5×10^{-12} for the best rubidiums to 2×10^{-11} for BVA quartz oscillators. With these state-of-art oscillators, an autonomy period of 33 hours can be achieved. Using a maximum time error of 10 µs, as is done in Figure 2, is appropriate in the case where the clock system switches from Phase-locked Mode directly to Holdover Mode, since the time error in Phase-locked Mode is in the range of only 20 to 100 ns. In the case where

the system switches from Frequency-locked Mode to Holdover Mode, there is an initial time error that has accumulated during the time period the system spent in Frequency-locked Mode. If the assumption is made that this initial time error is not higher that 3 µs, then there are only 7 µs left for the Holdover Mode, since the cdma specification allows for 10 µs in total. Figure 4 shows the situation where only 7 µs are allowed for the Holdover Mode. It is easy to see that with state-of art rubidium and BVA quartz oscillators, the holdover autonomy is still 24 hours. These 24 hours can be added to the autonomy period in Frequency-locked Mode, which is already 56 hours.

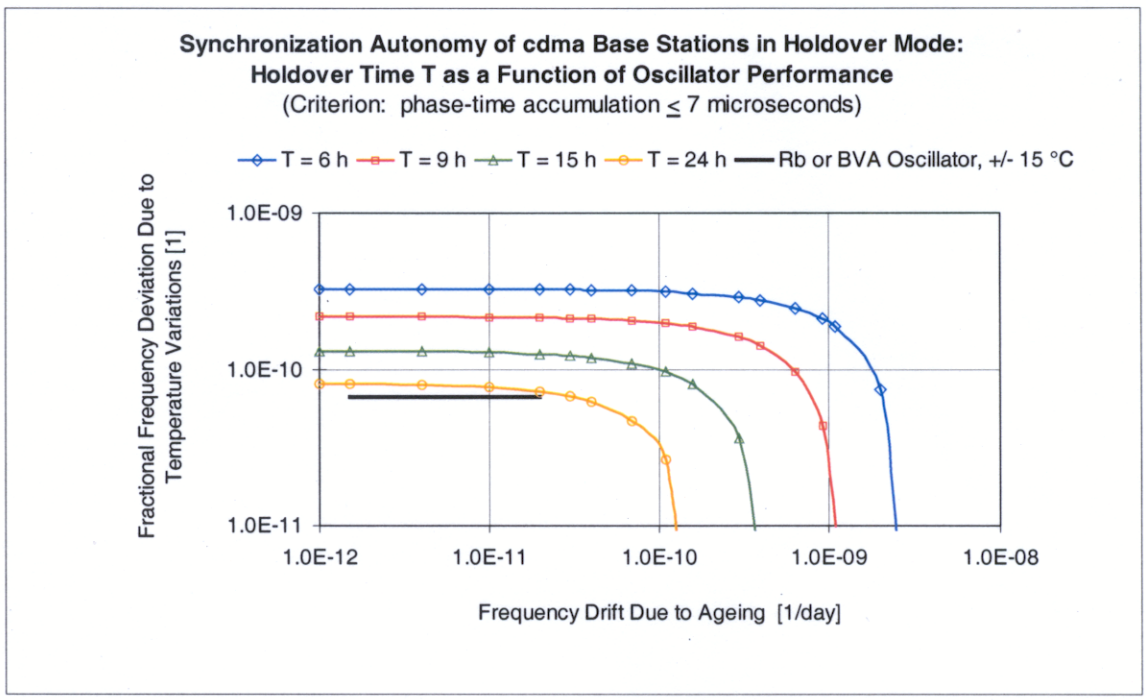

Figure 4: Synchronization Autonomy in Holdover Mode occurring after Frequency-locked Mode.

CONCLUSIONS

Base-stations in cdmaOne and cdma2000 mobile networks must be phase-synchronized with an accuracy of 3 µs in normal operation. Up to 10 µs are allowed in holdover situations, i.e. when phase-synchronism is lost due to equipment failures. Phase-synchronization is basically obtained via GPS. Figure 1 shows the block diagram of a clock capable of three operating Modes: 1) Phase-locked Mode when the GPS receiver is operating, 2) Frequency-locked Mode when the GPS-receiver has failed and the clock is locked to a frequency reference signal taken from the SONET transport network, and 3) Holdover Mode when both the GPS receiver and the frequency reference have failed. This concept provides a double protection against failures affection GPS reception. In Frequency-locked Mode, the 3 µs accuracy specification can be maintained for an autonomy period of 56 hours. In Holdover Mode and for +/- 15 °C temperature variations, the autonomy period is 33 hours, if the system was previously in Phase-locked Mode, and 24 hours, if it was in Frequency-locked Mode. Visibly the addition of an external frequency reference signal taken from the SONET transport network greatly improves the overall availability of the base-station synchronizaton.

REFERENCES

[1] International Telecommunications Union (ITU), *"ITU-T Recommendation G.824: The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy,"* Geneva, March 2000.

[2] S. Bregni, 1998, *"A Historical Perspective on Telecommunications Network Synchronization,"* **IEEE Communications Magazine, 36** (June), 158-166.

[3] D. Schneuwly, 2000, *"Cellular Synchronization Networks for Telecom Applications Based on the GPS and on SDH/SONET Networks,"* in Proceedings of the European Frequency and Time Forum (EFTF), 14-16 March 2000, Torino, Italy, pp. 82-87.