REDUNDANT ATOMIC FREQUENCY STANDARD TIME KEEPING SYSTEM WITH SEAMLESS AFS SWITCHOVER

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Abstract

This paper describes a redundant time keeping system (TKS) that provides an adjustable 10.23 MHz frequency output phase-locked to one of four 13.4 or 10 MHz atomic frequency standards (AFS) (5 MHz AFS with x2). Phase and frequency adjustment (1 ps, 0.02 uHz resolution) are accomplished without disturbing the input AFS. The TKS has a virtually perfect frequency step characteristic when a frequency change is executed. Data are presented showing that the deviation from a perfect frequency step is a transient of peak value less than 150 ps which decays in a fraction of a second. The TKS also has the ability to monitor and output the phase of a hot spare AFS relative to the primary AFS with a 1.3 ps resolution. By utilizing this phase information, the TKS can perform the seamless switchover of a digitally phase-locked VCXO from the primary AFS to the hot spare in case of primary AFS failure or problems. Seamless switchover is defined as the maintenance of both output phase and frequency continuity while and after the TKS switches the VCXO phase tracking from the primary AFS to the hot spare. Experimental data show that seamless switchover is accomplished with only a 50 ps phase transient decaying in a fraction of a second and with no observable change in frequency. Seamless switchover has applications both in space and ground time distribution systems where continuous availability and predictability after an AFS failure is desirable. For a GPS satellite, seamless switchover can eliminate a 1-2 week down time that occurs when an AFS failure is diagnosed and the satellite is prepared with a new AFS. The paper also describes a Kalman filter simulation that models the behavior of a GPS satellite phase prediction parameter during seamless and non-seamless switchover. For the non-seamless case, the simulation shows that the Kalman filter takes at least 6 hours for the filter to settle (with the orbital parameters fixed). For the seamless switchover, no detectable performance change is observed during or after switchover.

INTRODUCTION

This paper will describe a redundant time keeping system (TKS) that provides an adjustable 10.23 MHz frequency output which is phase-locked to one of four 10 or 13.4 MHz (5 MHz with x2) atomic frequency standards (AFS). Phase and frequency adjustment with 1 ps and 0.02 uHz resolution are accomplished without disturbing the input AFS. Other AFS and output frequencies can be accommodated with minor modifications to the design. The TKS has a virtually perfect frequency step characteristic when a frequency change is executed. The deviation from a perfect frequency step is a transient of peak value less than 150 ps which decays in a fraction of a second.

The TKS also has the ability to monitor the phase of a hot spare AFS with a 1.3 ps resolution (Allan deviate at 1 s). By utilizing this phase information, the TKS can perform a seamless switchover of the phase-locked VCXO from the primary AFS to the hot spare in case of primary AFS failure. As shown in Figure 1, seamless switchover is defined as the maintenance of both output VCXO phase and frequency continuity while and after the unit switches the VCXO phase lock from the primary AFS to the hot spare. This feature has applications both in space and ground time distribution systems where continuous predictability after an AFS failure is desirable. Finally, the paper will discuss the advantages of seamless switchover for improving the availability and predictability of GPS satellites in cases of AFS failure.

A block diagram of the TKS is shown in Figure 2. The TKS consists of 4 AFS's and a redundant Frequency Synthesizer Unit (FSU). In each FSU, a high isolation switch (92 dB measured isolation) selects a primary and hot back-up AFS from the 4 AFS units. The selected AFS's are routed to 2 programmable downconverters, which heterodyne the AFS frequencies to approximately 100 Hz IF's utilizing the 10.23 MHz output of a precision voltage-controlled crystal oscillator (VCXO). An event clock and phase-lock loop (PLL) processor use the zero crossings of the 100 Hz IF's to determine the phases of the two AFS's relative to the VCXO to a resolution of 1 ps (1.3 ps measured Allan deviate at 1 second). The processor then utilizes this information to digitally phase lock the VCXO to the primary AFS. The digital PLL allows the VCXO to have a commanded offset in phase (virtually unlimited range, 1 ps resolution) and a commanded offset in frequency (±1 Hz (1E-7) range, 0.02 uHz (2E-15) resolution). The processor also utilizes the phase information to model the hot spare's phase and frequency offset relative to the primary AFS. This information is used by the processor to correct the VCXO output phase and frequency when a switchover of the phase-locked loop from the primary AFS to the hot spare is initiated. Thus, the VCXO retains phase and frequency continuity within the bounds imposed by measurement error.

Seamless switchover is initiated under two conditions. First, the processor automatically initiates switchover when it detects a degradation of the integrity of the 100 Hz beat from the primary AFS. Second, an external processor or ground operations can also initiate a switchover by commanding one. AFS telemetry is provided to allow external diagnostics to aid in the detection of a primary AFS fault or problem.

A non-redundant breadboard of the TKS was fabricated and tested. Figure 3 shows a picture of the FSU breadboard. Figure 4 shows a detail of the high isolation switch. The following section will discuss some of the theory of operation and the experimental results. The reader is referred to references at the end of the paper for more detail.[1,2,3]

THEORY OF OPERATION AND EXPERIMENTAL RESULTS

1 PS PHASE MEASUREMENT SYSTEM

The phase measurement system consists of two downconverters, an event clock, and the PLL processor. Figure 5 shows a typical configuration of the downconverters. In the figure, a 13.4 MHz AFS signal is utilized to derive local oscillators (LOs) for successive mixings of the 10.23 MHz VCXO signal to a final IF of approximately 100 Hz. As shown in the figure, programmable mixers are utilized to generate the LOs by dividing the 13.4 MHz by 4, 76, and 3800 (Cs) or 4858 (Rb). For a 10 MHz AFS, the programmable dividers are set to other values that also produce an approximately 100 Hz final IF.

Since the phase is conserved through the downconversion process, the phase error[4] of the 100 Hz LO is equal to the phase error difference between the AFS and the VCXO

$$\phi_{100Hz} = \phi_{VCXO} - \phi_{AFS} \tag{1}$$

where the sign of the phase difference depends on the sidebands selected in the various mixings. The event clock and the PLL processor then utilize the zero crossing epochs t_n of the 100 Hz IFs from the two downconverters to generate differences in clock reading error[4] x between the VCXO and each AFS. The event clock first measures the epochs of each zero crossing to a resolution of 98 ns (10.23 MHz clock). The phase error of each 100 Hz IF is given, in terms of t_n, by

$$\phi_{100Hz} = \phi_{VCXO} - \phi_{AFS} = 2\pi(n - f_b t_n) \tag{2}$$

where f_b is the frequency of each 100 Hz IF. The processor determines each f_b by averaging differences in zero crossing epochs using a moving average to reduce measurement noise.

The clock reading error of an oscillator at a frequency f_o is defined by the well known formula[4]

$$x = \phi/(2\pi f_o) \tag{3}$$

In the literature, the terms phase and clock reading error are often used interchangeably, where the term phase error in xx ns is often used. The units of phase are strictly in degrees or radians and the term clock reading error is correctly used for errors in seconds. However, because of the common usage of phase for clock reading error, phase will be used instead of clock reading in future sections, but clock reading error will be used in this section to avoid confusion.

For the TKS, f_o in (3) is always 10.23 MHz regardless of the original AFS frequency because the AFS is utilized to generate all the LOs in the compound mixing process. With this choice of LO reference, the compound downconversion is equivalent to a simple downconversion with an imaginary AFS at 10.23 MHz (plus or minus 100 Hz) regardless of the actual AFS frequency.

Thus using (2) and (3), the difference in clock reading error between the VCXO and each AFS is given by

$$x_{VCXO} - x_{AFS} = (n - f_b t_n)/f_o \quad (4)$$

where n is the zero crossing count. To determine n, the processor doesn't count zero crossings, but utilizes a previously published technique[3] that relies on the smoothness properties of the 100 Hz IF to determine n. This technique keeps the n count from permanently jumping when noise creates false events or causes a count to be skipped.[3]

From (4), one can show that the clock reading resolution δx due to the event clock time resolution $\delta t = 1/f_o$ is given by

$$\delta x = f_b/f_o^2 = 0.96 \text{ ps} \quad (5)$$

The measured performance of the phase measurement system is shown in Figure 6. The Allan deviate at 1 second is 1.3 ps, and the noise floor stays well below the stability of either a cesium or rubidium AFS over the full range of averaging times. The difference in clock reading between the two AFSs is determined by subtracting the two clock reading measurements made relative to the VCXO.

PHASE-LOCK LOOP PROCESSOR

Figure 7 shows the PLL processor and event clock. To generate the digitally implemented phase-locked loop, the processor utilizes the phase difference between the VCXO and the primary AFS. First it subtracts a phase and frequency offset from the measurement. Then a phase limiter is utilized to limit the size of the measured phase error. This technique has been used in previous digital phase-locked loops to keep large measurement errors from causing cycle slips.[3] The limited error is then input to a digital embodiment of a 2nd order phase-locked loop,[5,6] where scaled versions of the limited phase error and its digital integral are added to produce the two loop orders. The digital loop operates at a sampling rate equal to the 100 Hz primary AFS IF frequency at which phase samples are collected. The summed signal is sent to a look-up table before being output to a digital-to-analog converter (D/A) that controls the frequency of the VCXO. The look-up table stores the voltage-to-frequency characteristic of the VCXO and allows the loop parameters and performance to be independent of the VCXO tuning curve characteristics (including linearity).

An important feature for the frequency step characteristic is the use of precharge in the loop integrator. When a PLL synthesizer is commanded to change frequency, the loop integrator must change to accommodate the new VCXO control voltage. Under normal operation, the change in the integrator will take several time constants to occur, causing the PLL to deviate from an ideal frequency step characteristic. A precharge circuit anticipates the new integrator value at the time of the frequency change command and preloads the new value into the integrator. This greatly reduces the settling excursion when changing frequency. Figure 8 shows the measured PLL performance with and without the precharge being circuit utilized. Note the overshoot at the frequency change without the precharge circuit, and the sharp corner with the precharge circuit.

Figure 9 is a detail of the measured deviations from an ideal frequency step with the precharge circuit in place. Notice that the peak deviation from an ideal frequency step is less than 150 ps and decays rapidly with a 0.1 s time constant (loop time constant). Thus,the TKS has very high predictability, even transiently, when frequency changes are commanded, with a simple step model predicting transient behavior at the sub-nanosecond level.

SEAMLESS SWITCHOVER

When the processor detects faulty behavior at the primary AFS zero crossings or is externally commanded based on outside fault diagnostics, seamless switchover is initiated. The processor then (a) switches the loop tracking over to the hot spare, and (b) utilizes the measured phase and frequency difference of the hot spare relative to the primary AFS to correct the loop phase and frequency offsets to minimize changes in the output phase and frequency. Measurement error is minimized for the phase and frequency offsets by using a moving average with settable time constant to generate the AFS offset data.

Figure 10 shows the measured switchover performance with and without seamless switchover. For seamless switchover, the transient behavior is very good because of the precharge circuit. The peak transient excursion is less than 50 ps, and decays with a 0.1 s time constant. There is no measurable permanent offset in either phase or frequency to within the noise limits of the TKS phase measurement system. For non-seamless switchover, there are, of course, both phase and frequency steps corresponding to the differences between the primary AFS and hot spare.

TKS ADVANTAGES FOR GPS AND OTHER TIMEKEEPING SYSTEMS

Both seamless and non-seamless switchover have been proposed in time distribution systems for space applications and utilized in systems for ground applications[1-3] where availability and predictability after an AFS failure is desirable. A non-seamless switchover system has been operating at the NASA TDRS White Sands ground station for many years.[3]

Even non-seamless switchover systems that allow monitoring of hot spares have many advantages. They allow spare AFSs to be set up and characterized before use as the primary unit. They also allow a troubled unit to be taken off-line and monitored, with the station or satellite taken off-line only for the time it takes to switch AFSs and reacquire prediction software. For GPS, this can reduce the down time of a satellite with a troubled or non-functioning AFS from 1 to 2 weeks to on the order of a day to allow for the Kalman prediction filters to reacquire new phase (clock reading) and drift (frequency) parameters. Seamless switchover systems add an even higher degree of availability in case of AFS failure or problems, allowing AFSs to be switched with no down time or degradation in predictability of the output.

KALMAN FILTER SIMULATION

A simulation was performed to compare the effects of seamless verses non-seamless switchover on Kalman filters similar to those used in GPS. For this simulation, noise models that accurately predicted both the white frequency and flicker of frequency behavior of actual GPS clocks were used, and orbit parameters were fixed. The predicted Kalman parameter studied was the N hour phase prediction. Figure 11 shows the results for the 24–hour Kalman phase prediction for seamless and non-seamless switchover. For non-seamless switchover, the Kalman filter was reinitialized at switchover to make the solution converge more quickly. For seamless switchover, the Kalman filter was not reinitialized. During the non-seamless switchover, for 24 hrs before the switchover, the prediction, of coarse, has a large error because predictions are based on the old clock and the new clock is in place 24 hours later. The non-seamless case starts out with an error greater than 400 ns at switchover and converges within 6 hrs after switchover (with the orbit parameters fixed). It is expected that the convergence will take longer—on the order of a day or so—if orbit parameters are not fixed. Smaller prediction times show smaller excursion values, but otherwise reproduce the 24-hour results. As expected for seamless switchover, the 24-hour prediction stays at pre-switchover levels (<20 ns) during the whole simulation period.

TKS GROWTH CAPABILITIES

The TKS architecture lends itself to several addition features of use in time distribution systems. These have not been implemented in the current hardware, but are easily implementable by making minor modifications to the existing system. The first is the addition of more hot AFS monitors. This is accomplished by adding more downconverters, more event clock inputs, and processor calculation algorithms. The second is correcting the VCXO output for AFS frequency drift or drift rate in GPS terminology. This is easily accomplished by adding a third correction term to the phase error calculation so that the VCXO output can be corrected for frequency drift, in addition to the existing frequency and phase corrections. The frequency drift value is supplied externally or can be measured by the TKS internally if a mixture of Cs and Rb AFSs are being monitored.The third is phase tracking of the VCXO to the average phase of multiple AFSs, suitably corrected for phase, frequency, and frequency drift. This is accomplished by utilizing the suitably averaged phase differences from several AFSs as the error term in the digital PLL.[3]

CONCLUSIONS

Data has been presented showing that the TKS provides a viable way to provide a redundant and phase and frequency steerable output derived from atomic frequency standards that has the full stability performance of its AFS references at the sub-nanosecond level. Datahavealso been presented showing the advantages of seamless switchover for increasing predictability and availability in a time distribution system whenever there is an AFS difficulty. Specifically for GPS satellites, seamless switchover can completely eliminate a 1-2 week down time in cases where the AFS must be switched. Datahavealso been presented showing that the TKS implements seamless switchover successfully, with no detectable change in phase or frequency at the sub-nanosecond level during and after switchover.

REFERENCES

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5. F. M. Gardner, PHASELOCK TECHNIQUES, Wiley, 1979.

6. W. C. Lindsay and C. M. Chie, "A Survey of Digital Phase-Locked Loops," Proc. IEEE, V. 69 #4, April, 1981.

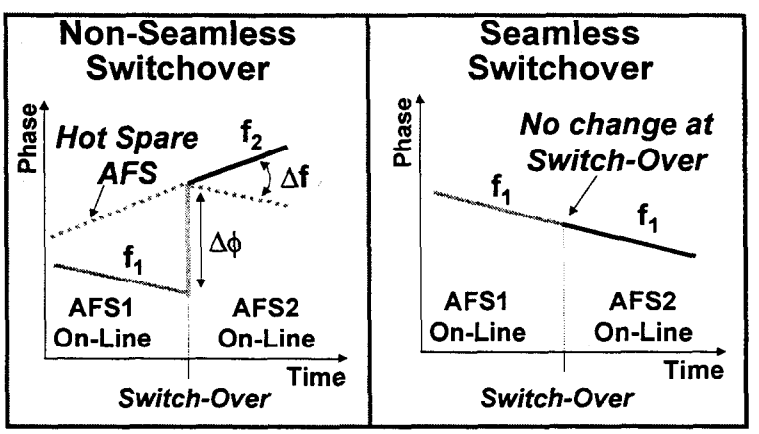

Figure 1. Seamless vs Non-Seamless Switchover.

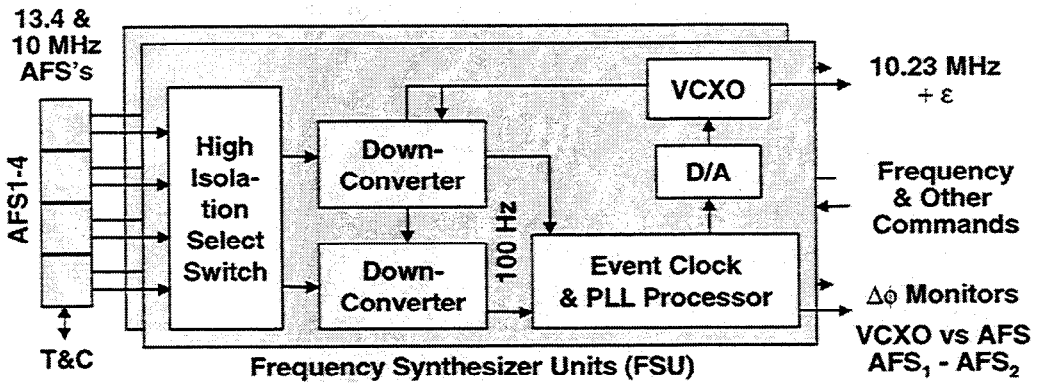

Figure 2. Redundant AFS Time Keeping System.

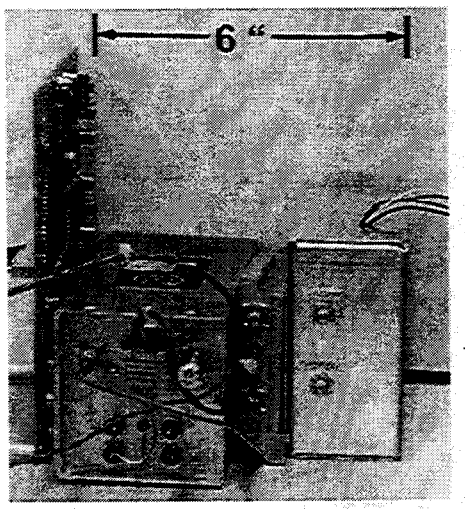

Figure 3. Frequency Synthesizer Breadboard.

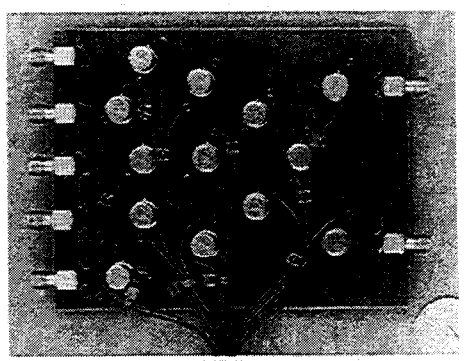

Figure 4. High Isolation Switch.

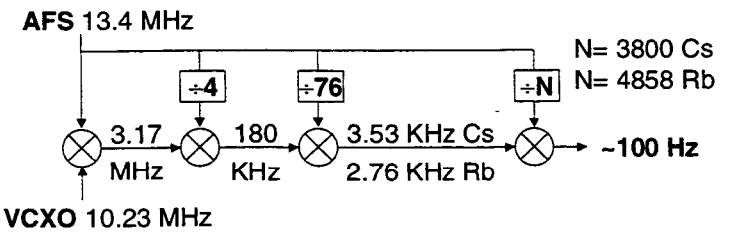

Figure 5. Typical Downconverter Configuration.

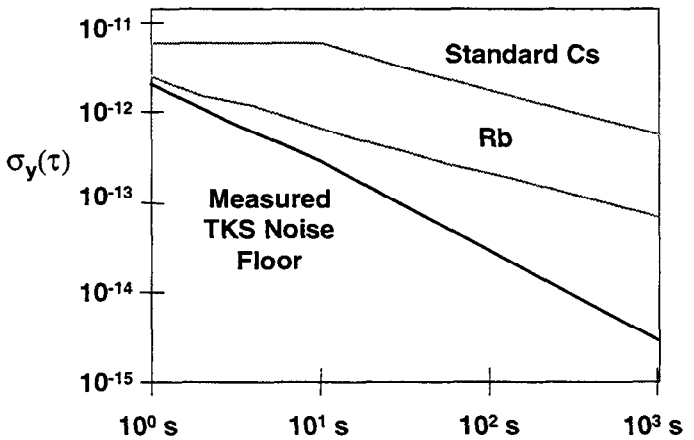

Figure 6. Measured Performance of TKS Phase Measurement System.

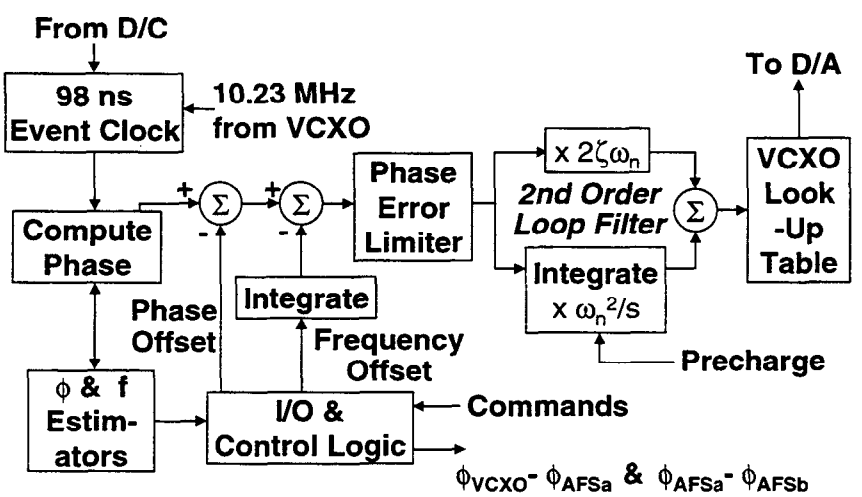

Figure 7. Phase-Lock Loop Processor and Event Clock.

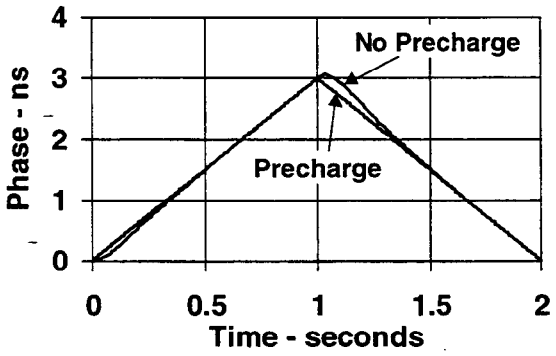

Figure 8. Measured PLL Performance with and without Precharge.

Figure 9. Measured Deviation from Ideal Frequency Step (with Precharge).

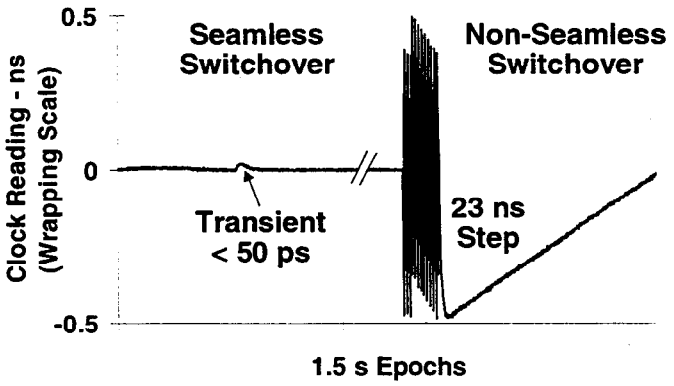

Figure 10. Measured Results for Seamless vs.Non-seamless Switchover.

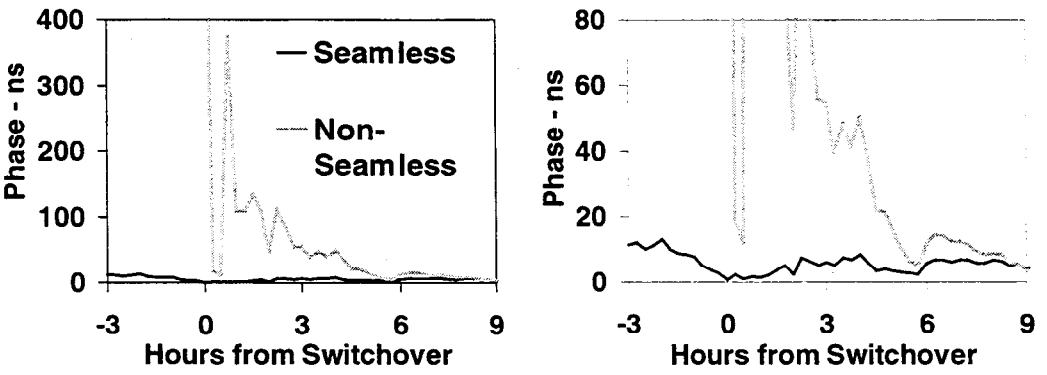

Figure 11. Simulation Results for the Kalman 24-hr Phase Prediction.