NETWORK TIMING EQUIPMENT FOR SYNCHRONOUS DIGITAL TELECOMMUNICATION

Philippe Girardet, Pascal Rochat and Erhard Graf,
Oscilloquartz S.A., Brévards 16, Neuchâtel, Switzerland

ABSTRACT

A new equipment for digital communication networks has been developed which fully meets requirements for input jitter and high redundancy. Three temperature controlled quartz oscillators using BVA crystals are locked by digital servo loops to three reference lines operating at the network frequency. Microprocessor control and majority logic extend the meantimebetween-failure to an estimated 60 years.

1. INTRODUCTION

The establishment of a digital communications network requires the generation of different base frequencies (bit rate of 2.048 Mbit/sec., 8.448 Mbit/s, ... etc.).

In general, these different signals must have the following principle characteristics :

- High frequency stability in short-term as well as long term in order to realize a sufficiently low transmission bit error rate.
- A wide availability in order to assure reliable network operation.

The first characteristic is obtained by using ultra-stable frequency sources such as :

- cesium beam frequency standards
- high stability quartz oscillators

The second characteristic is realized by creating a timing network having four levels of hierarchy and using numerous redundancies [1]. The first level of hierarchy consists of three centers, each equiped with a cesium frequency standard and two BVA quartz oscillators. Each of these centers pilots a certain number of second level centers (divided into three regions), which are equiped with three quartz BVA oscillators. Each BVA oscillator is slaved to a different line (one line coming from the second level, and two lines coming from the first level).

An important point to mention is that in a digital telecommunications network different sub-assemblies, e.g. repeators, multiplexers, etc., as well as climatic effects on the transmission lines cause large changes in phase stability of the transmitted signals (jitter, wander [1]). One of the main functions of all centers is to be able to phase-lock to an input signal of high jitter, and output a signal of sufficient phase stability to achieve the required minimum bit error rate in the transmission system.

In the following, we briefly describe development and construction of second level centers with particular emphasis on the phase-lock servoing of the BVA quartz oscillators (PLL).

2. GENERAL BLOCK DIAGRAM

The general block diagram of a second level center is shown in figure 1.

Three PLLs (phase-locked-loop) A, B, C are servoed via a time recovery circuit TEX A, B, and C to three 2.048 MHz PCM lines, N1, R3, N2.

The PLL 5 MHz output signals are summed to give two 5 MHz buses which supply, via limiters, nine pairs (maximum) of frequency converters which synthesize, from 5 MHz, all base frequencies (TDM and FDM). A more detailed discussion of the block diagram is given in reference [1].

3. PRINCIPLE SPECIFICATIONS

In the following, we enumerate and comment on the main performance requirements contained in the detailed specifications established in collaboration between the R+D division of Swiss PTT (Post, Telephone & Telegraph) and Oscilloquartz S.A.

Input signal

- Taken from a PCM line, code HDB-3, at 2.048 MHz [2]. Amplitude 224 mV p-p with 60 mV p-p additive amplitude noise.
- Jitter according to CCITT G-703 [2] as represented in figure 2, but with a minimum frequency (f1) extended to 0.01 Hz instead of 20 Hz. It should be noted that, in practice, f1 can be lower still (for example from effects of seasonal and temperature variations on transmission cables).

  1 UI = 1 period at 2.048 MHz = 488 ns, therefore jitter = 732 ns.
- Long term stability : 4×10^{-11} on input R3, 2×10^{-11} on N1 and N2.

Output signal

- TDM and FDM frequencies
- TIE according to figure 3.

  Curve 1 : TIE according to CCITT G-811 [2]

  Curve 2 : TIE specified

  The TIE (Time Interval Error) is the time difference from an ideal reference, during a time interval S [2].

  TIE = $\Delta T\ (t+S) - \Delta T\ (t) = S \cdot y$

  $\Delta T\ (t+S)$ = time difference at time t+S

  $\Delta T\ (t)$ = time difference at time t

  S = time interval

  y = average fractional frequency difference during interval S

Special aspects of PLL A, B and C

Loss of reference or a reference phase jump greater than 670 ns opens the PLL and blocks the oscillator control voltage. During loss of reference, input fractional frequency drift of the oscillator must be less than 5×10^{-10} in 18 hours.

Monitoring

A PLL is to be taken out of service by opening contacts A, B, or C (figure 1) whenever the PLL output does not conform to specifications according to the following monitoring criteria :

- to be taken out of service by means of majority decision when the TIE AB, BC, or CA exceeds the limits of curve 2 figure 3 for a time interval S from 10^{-2} s to 10^{5} s (corresponding frequency difference of 4×10^{-11}.
- to be taken out of service when the measured PLL output signal decreases > 1.5 db from nominal.

In the case of multiple malfunction, the monitoring criteria are as follows for each PLL :

- phase jump with respect to the reference greater than 670 nsec
- servo control voltage on the oscillator exceeds limits (PLL loop failure)
- presence of an alarm indication signal (AIS) in the reference
- loss of the reference
- BVA quartz oscillator oven temperature

4. PLL

The TIE specified for PLL output in the presence of high-level (1.5 periods) and low frequency (0.01 Hz) input signal jitter requires a PLL having a cut-off frequency in the order of 0.1 mHz, that is to say, time-constant of about 1500 s.

Such a requirement plays a direct role in the choice of servo system elements. It requires a digital filter for technological reasons and, in addition, an oscillator of very high stability such that the TIE requirements can be assured during at least one time constant. In other words, the oscillator long-term stability must be sufficiently high so that the oscillator can always be corrected by the servo loop.

The BVA quartz oscillator (OSA type 8600) having an aging rate $\leq 2 \times 10^{-11}$/day and a stability $\leq 5 \times 10^{-10}$ over temperature range -30° to +60°C meets the requirements of the specification by a large margin.

Performance of this oscillator when the PLL is open and control voltage blocked at the memorized value makes it possible to increase the time in which the TIE remains within specifications (figure 3). (This time interval depends upon several factors : overall-stability of the oscillator and its control voltage, value of TIE at the moment the control voltage is memorized.) The specification of 5×10^{-10} in 18 hours can be met by a large margin.

The performance requirements have a direct effect on the design of the phase comparator which must have the following characteristics :

- high gain and resolution
- sufficient dynamic response (without cycling)
- capable of initialisation on restoration of the reference

Microprecessor-based electronics will best meet the above requirements with the following advantages :

- facile realization of a digital filter
- realization of a phase comparator meeting all requirements
- reduction in space and power requirements
- flexibility attributed to a programmed system

In addition, the microprocessor enables us to obtain auxiliary functions such as, for example, measurement of TIE AB, BC and CA.

The jitter and TIE having the dimension of time enable us to make all calculations concerning the PLL in phase-time [3].

$$x(t) = \int_0^t y(t)\,dt = \frac{\phi(t)}{\omega_0} \quad [s]$$

or again :

$$\Phi(t) = \omega_0 t + \phi(t) \quad [rad] \quad \text{(phase-angle)}$$

$$\frac{\Phi(t)}{\omega_0} = t + \frac{\phi(t)}{\omega_0} \quad [s] \quad \text{(phase-time)}$$

The PLL block diagram is shown in figure 4. Different functions are represented in symbols, the shaded parts are realized by means of microprocessor. In the following, we successively describe the different PLL elements and finally its transfer function.

4.1. LOW-PASS DIGITAL FILTER

The low-pass digital filter schematic is shown in figure 5. The discrete transfer function is :

$$\frac{X'(Z)}{X(Z)} = Do \quad \frac{1+Z}{Z-Co}$$

Sampling frequency : fs $\sim$ 20 Hz

The corresponding continuous transfer function is of the form $\frac{1}{1+S\tau_2}$, τ_2 being the time-constant of the low-pass filter LPF

4.2. D/A CONVERTER

The D/A conversion is derived from a pulse-width modulator having a maximum resolution of 16 bits.

The pulse-width modulation output passes through a 3rd order low-pass analog filter with characteristics such that the output side-bands due to the pulse-width modulator are < -150 db below the carrier. The D/A resolution finally chosen is 15 bits which gives a frequency pulling factor on the oscillator of 1.6×10^{-12} per step.

4.3. PHASE COMPARATOR

Schematic of the phase comparator is shown in figure 6. The comparison of the phase-time difference Xr(t) - Xo (t) is realized as follows :

The average period of the beat between frequency $\nu r/2$ = 1.024 MHz (reference) and $\nu o/5$ = 1 MHz (5 MHz oscillator signal) is measured. It is important that this period measurement is made without dead-time in order not to introduce an error. This is accomplished by using three programmable 16 bit dividers (contained in an IC).

Counter 0 is used to divide the beat frequency by 2400. Output of this divider provides an interrupt command to the microprocessor and at the same time multiplexes the clock signals of counters 1 and 2, which signal is the input frequency ν_0.

Counters 1 and 2 are alternatively read at the rate derived from counter 0. Counter 0 provides the microprocessor interrupt signal at each leading and trailing edge of the counter output.

The values X_A contained in counters 1 and 2 correspond to the average period of the beat frequency (see also figure 4). One subtracts thus from X_A a fixed reference value X_{Ar} :

$$\Delta X = X_A - X_{Ar}$$

For signals at 1 and 1.024 MHz, the beat comparison yields a gain of 40 and the period of the clock frequency for counters 1 and 2 is 200 ns. The resolution thus obtained expressed in phase-time is 5 ns per step.

4.4. TRANSFER FUNCTION

The sampling frequency being much higher than the cut-off frequency allows us to simplify the analysis and consider that the PLL function in a quasi continuous fashion. We calculate the transfer functions with the aid of the Laplace transform. The choice of the transfer function for the digital filter is justified by the necessity to obtain the most favorable PLL servo system step response.

Expressed in phase-time, the transfer function of a PLL becomes :

$$\frac{Xo(S)}{Xr(S)} = \frac{KF(S)}{S+KF(S)}$$ see mathematical schematic figure 7

$$F(S) = \frac{1}{1+S\tau_2}$$

$K = K\phi.Ko$ with

$K\phi$ = gain of the phase comparator [steps/s]

Ko = pulling factor of the oscillator [1/step]

$$\frac{Xo(S)}{Xr(S)} = \frac{K}{S^2\tau_2+S+K} = \frac{\omega_n^2}{S^2+2\zeta\omega_n S+\omega_n^2}$$

$$\omega_n = \frac{K}{\tau_2}$$

On chosing a damping factor equal to one : $\tau_2 = \frac{1}{4k}$

with $k\phi = \frac{1}{5x10-9}$ step/s and Ko = $1.6x10^{-12}$ 1/step

one obtains :

τ_2 = 780 s and ω_n = 0.64 mrad/s

(τ_1 = 1562 s, fn = 0.1 mHz)

5. MONITORING, TIE MEASURE

Without going into details about the monitoring, it seems to us worth while to give some explanations concerning monitoring and measurement of TIE AB, BC and CA.

As it is illustrated in the block diagram figure 1, the TIE AB, BC, CA are measured in each PLL principally for reasons of reliability. The measurement of TIE, which is derived from the measure of the average frequency offset during a time interval S, is accomplished by the double-beat method [4]. For example, the TIE measure between A and B is illustrated in figure 8.

As one can see, the average periods NA and NB of the beat frequencies $\nu_A - \nu_1$ and $\nu_B - \nu_1$ are measured with two elements identical to those used for phase comparison (see figure 6).

The frequency chosen for the common beat oscillator is ν_1 = 4.9975 MHz which yields a resolution of 0.1 ns. The divider ratio K gives the rate of acquisition : K is chosen = 25 thus obtaining an acquisition every 10 ms.

The average frequency offset Y_{AB} is calculated, by the microprocessor, from NA and NB with floating decimal point according to IEEE 754. The resolution for an average time duration S of one second is $Y_{AB} = 1x10^{-10}$. The calculation of TIE = S y for longer time intervals is accomplished by taking a sliding average. The system dynamic is from +/- $1x10^{-14}$ in 10'000 seconds to +/- $1x10^{-4}$ in 10 ms.

6. RELIABILITY

One can see by studying figure 1 that the system we describe consists of three lines with a majority decision element. The decision is based on the magnitude of the TIE AB, BC, CA. In contrast to the classic system in which there is one line in use and a switch-over in the event of failure, a three line configuration has been adopted in which all lines are in use when they are functioning normally. A failure of one line causes it to be removed from service by opening the corresponding switch (A, B or C).

During the development of a redundant system, it must be borne in mind, although it would seem evident, that the reliability of a monitoring system must be much higher than the system being monitored. In the case of monitoring TIE, this is difficult to achieve in view of the relative complexity of the measurement. This has lead us to triple the measure and monitoring of TIE, then to make two successive majority decisions. One decision is made on the measurement system, the second on the measured values. As is seen in figure 1, TIE AB, BC, CA are measured in each PLL by using the microprocessor of the PLL and according to the method described in the preceeding paragraph. The majority operations as well as the commands to remove from service are realized by means of a unit presenting all the desired reliability.

This approach has enabled us to attain an estimated MTBF of 60 years for the part of the system between the inputs and the 5 MHz summing output buses (required functioning : the two 5 MHz buses are synchro-

nized to one or two references). Thus, we have gained a factor of ten, as compared to a solution of one triangular measurement of TIE only. In association with the usual techniques of repairable systems (modular concept, reliable failure alarm systems, redundant power supplies, etc.) we attained the reliability conforming to the specification.

7. CONCLUSION

The use of a BVA quartz oscillator of high stability and the application of microprocessor techniques have enabled the development of a complex system in a compact and economic form. Flexibility of the microprocessor offers great possibilities for adapting future requirements. After an 18 months development period, the prototype has been submitted to extensive tests and measurements. The results have shown that the contract specifications have been met, and in some points exceeded. This is the case, for example, for the TIE : at ambiant temperature and locked to a cesium standard, a maximum of 50 ns in 38 hours was achieved. This corresponds to a frequency offset of 3.7×10^{-13}. This is also the case for stability without reference where a maximum offset of 3.8×10^{-11} in 18 hours was recorded. Currently, second level centers for the Swiss communications system are in production. Furthermore, development of first level centers is underway. Here, the work is largely one of construction since, as can be seen by information in reference [1], the main difference from a second level center consists in replacing PLL B by a cesium atomic frequency standard.

REFERENCES

[1] A network timing concept for Switzerland, P. Kartaschoff, P.A. Probst and P. Vörös, 17th PTTI 1985

[2] CCITT recommandations G-701 to G-942 (digital networks, transmissions systems and multiplexing equipment)

[3] Frequency and time, P. Kartaschoff Academic Press 1978 ISBN 0-12-0400 150-S

[4] NBS Technical note 669, the measurement of frequency and frequency stability of precision oscillators

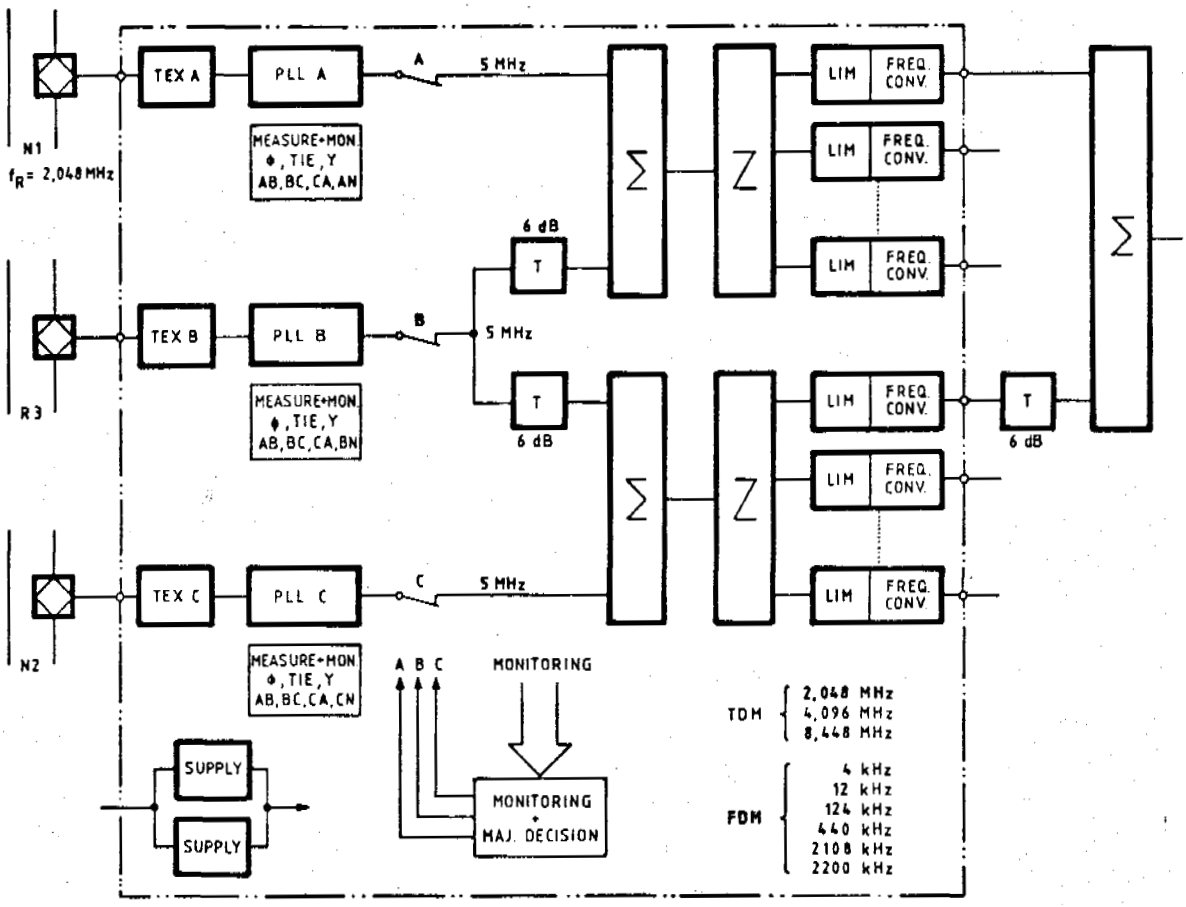

FIGURE 1 : GENERAL SCHEMATIC SECOND LEVEL CENTER

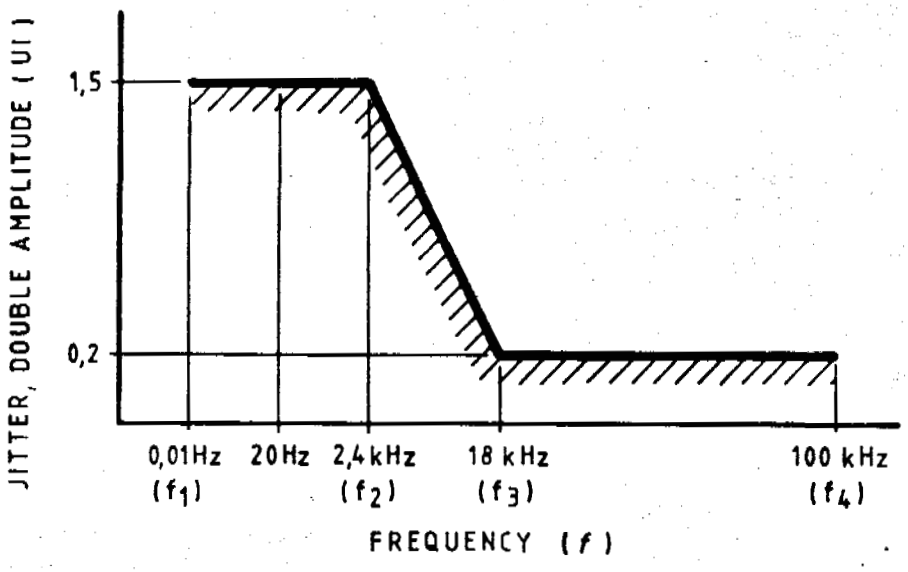

FIGURE 2 : JITTER INPUT SIGNAL

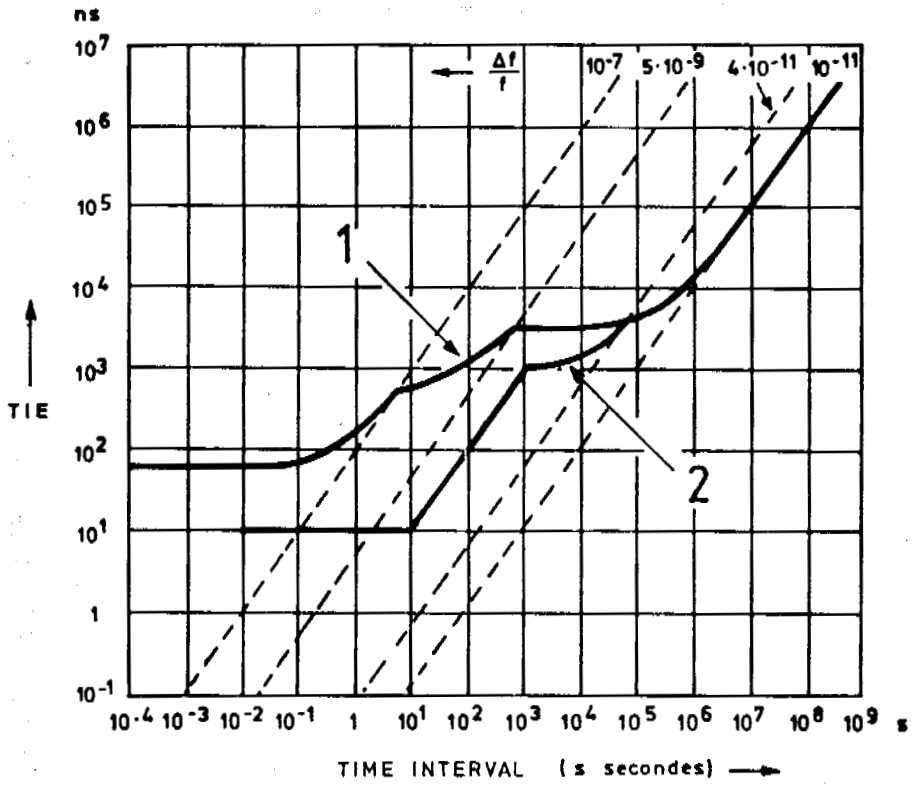

FIGURE 3 : TIE OUTPUT SIGNAL

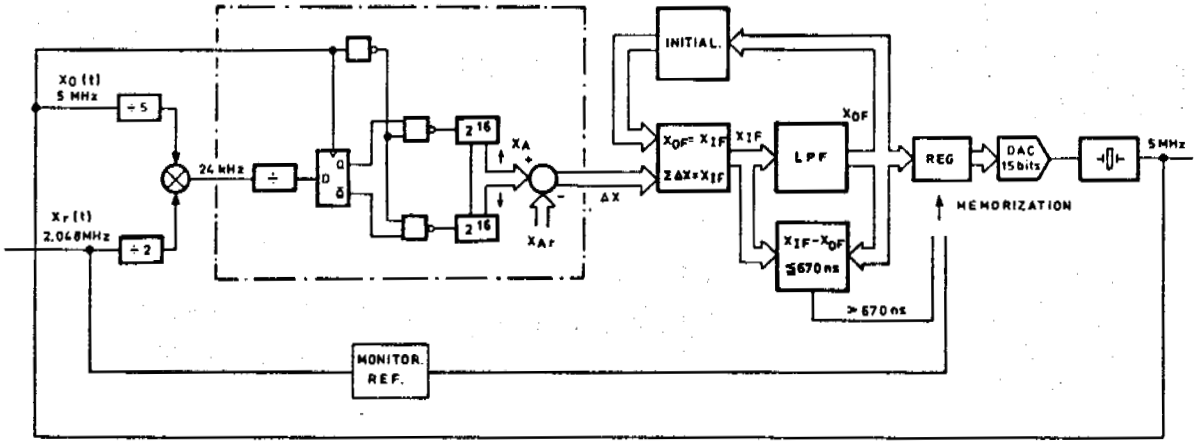

FIGURE 4 : PLL BLOCK DIAGRAM

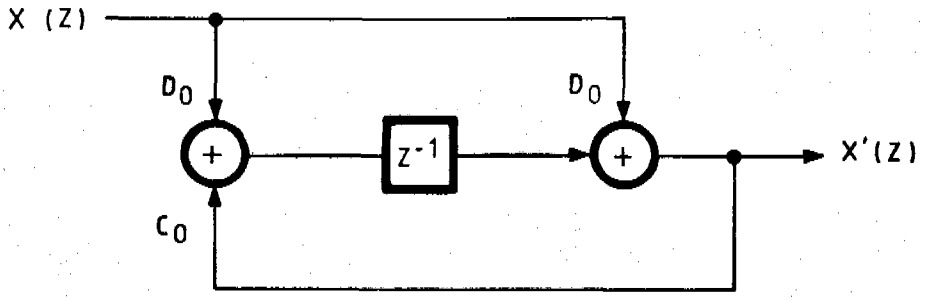

FIGURE 5 : DIGITAL FILTER

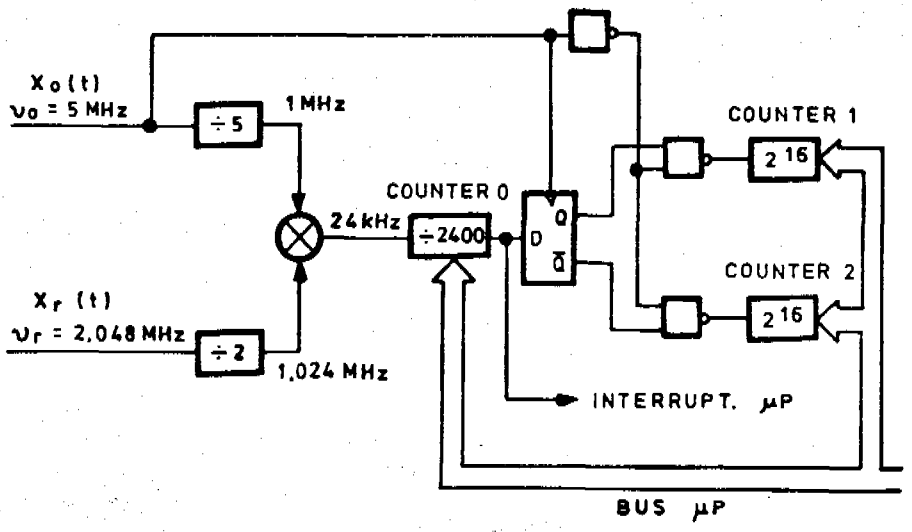

FIGURE 6 : PHASE COMPARATOR

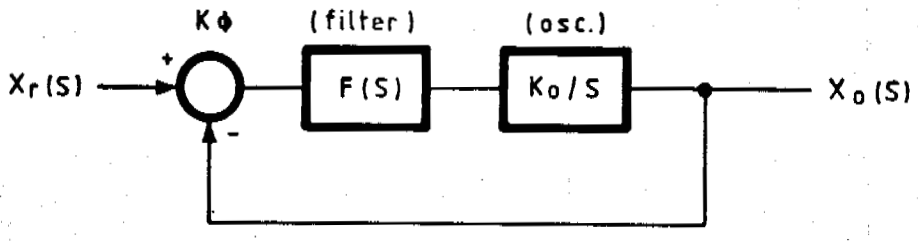

FIGURE 7 : PLL MATHEMATICAL SCHEMATIC

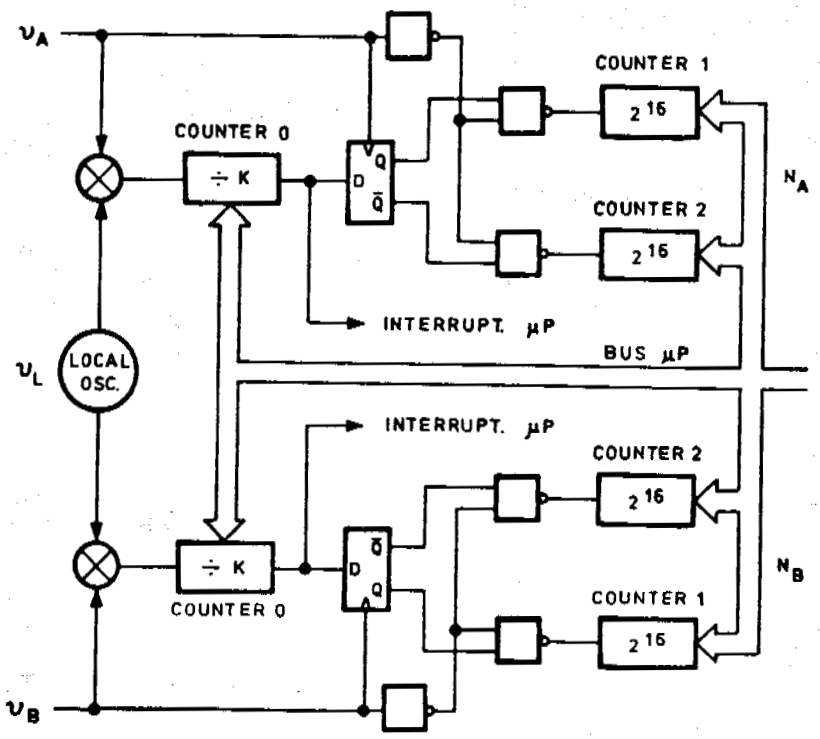

FIGURE 8 : MEASUREMENT OF TIE

QUESTIONS AND ANSWERS

DAVID ALLAN, NATIONAL BUREAU OF STANDARDS:
I have two questions if I may. Are you ambiguous at the one second level so that the UTC leap seconds don't bother you?

MR. GRAF:
This is a system question and Peter would have a better answer.

MR. KARTASCHOFF:
That is true. What we do is use the UTC frequency and generate a local time scale.

MR. ALLAN:
In the true sense of the word, synchronization means obtaining the same time in the different parts of the system. What you are doing is syntonization, the obtaining of the same frequency in the different parts of the system.

MR. GRAF:
That is right, it is syntonization.