DESIGN APPROACH FOR A MICROPROCESSOR-BASED GPS TIME TRANSFER RECEIVER

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ABSTRACT

This paper describes the design concept and characteristics of a self-contained microprocessor-based GPS time transfer receiver. A prototype of this unit is currently in the test phase. It employs two-bit digital baseband correlation rather than analog IF correlation of the signals with the reference code. The correlator, numerically controlled oscillators (NCO) and code generator are implemented in a special-purpose digital signal processor. The time is recovered in the digital code tracking loop, and final corrections are applied in the control processor. By means of asynchronous sampling techniques for the digital correlator and NCO, the time transfer resolution limit is 2^{-N} part of a code chip period, where N is 32 for a 32-bit accumulator in the NCO. Other features of this design are: drift-free digital mechanization, high reliability of digital circuits, flexible control capability of the microprocessor, and potential for a high degree of digital VLSI chip development leading to compact, low-cost units.

A description is given of the process by which the precise measurement is made between user clock and received signal code. The user-clock-derived sample times in the code tracking loop yield high-resolution uncorrected time sample words. These uncorrected time words are corrected for range to the satellite, satellite clock error, ionospheric error, and relativistic errors. They are then differenced with the user clock to yield user-clock error estimates.

User-clock outputs consist of 1-pps, time readout, and direct digital outputs of time and time error of the user clock.

Test data on random error of the approach are also presented.

INTRODUCTION

The GPS receiver described in this paper consists of a baseband RF converter, digital signal processor, and general-purpose microprocessor. The design approach and components have been developed at Interstate Electronics during the past four years as part of an internally funded GPS applications research program. The goal of this research effort is to develop a reliable, low-cost, and highly accurate modular system that can be configured to satisfy a wide range of requirements in the areas of timing, tracking, and navigation.

Our design approach is primarily digital in that the received signal is converted to baseband and digitized before any signal processing is attempted. We intend to achieve reliability and low cost by employing the latest gate-array and custom-VLSI (Reference 1) techniques. System accuracy is achieved through use of digital correlation techniques (Reference 2) with asynchronous sampling to attain very high measurement resolution, and by using long (i.e., 32-bit) word lengths.

This paper emphasizes the characteristics of the digital signal processor that provide the capability of extracting time from the received signal directly as a numerical value.

Evaluation of this GPS time transfer technique is currently in progress at Interstate, and the results of initial tests of the system's tracking accuracy are included in the paper.

BACKGROUND

Our work with GPS receivers began in the middle of the last decade with development of the Flight Test Support System (FTSS) for the Navy's Trident I (C4) strategic weapon system (Reference 3). The FTSS employed the early GPS satellites for metric (postflight analysis) tracking and time division multiple access (TDMA), pseudorandom-noise (PRN)-coded ground transmissions for range safety tracking. Many of the digital-baseband processing techniques we are now using for GPS processing originated in the FTSS.

We subsequently developed a breadboard GPS system that was used for test and evaluation at our facility about two years ago. This GPS receiving system employed clear/acquisition (C/A)-code, one-bit digital baseband correlation and was an all-digital system (Reference 2) except for the RF converter, which converted the received signal to baseband for digitization. The system's central processing unit was a Digital Equipment Corporation PDP-11 computer.

The time transfer receiver described here is a microprocessor-based system using a Motorola Corporation MC68000 as its central processing

unit. This version is a combined C/A- and P-code GPS receiver, with the P-code capability added to determine and compare the time-transfer accuracy and reliability achievable with each code, and to satisfy requirements for other applications.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the GPS time transfer receiver. The RF converter is a straightforward, double-conversion device for L1. The carrier numerically controlled oscillator (NCO) drives the baseband converter to *tune* the receiver to the signal plus Doppler. (The structure of this second-order phaselocked loop is described later.) The digitizer (Figure 1) has been mechanized as either a one- or two-bit (Reference 2) analog-to-digital converter sampling at a rate slightly higher than twice the code chip rate.

The correlator processes the digitized in-phase (I) and quadrature (Q) data to generate a tracking-error signal. In response to the delay tracking error, the delay tracking filter drives the code NCO and code generator. This loop is the time transfer mechanism (described later in more detail with the clock and its associated components).

The integrated correlation data and loop feedback signals are sampled at 250 Hz.

In our system, the microprocessor accomplishes most of the signal processing. Figure 2 illustrates the algorithms and process flow. Note that the code generator is mechanized in a separate microprocessor (Reference 2) and that basic signal acquisition is not shown.

All computations except clock correction are completed in less than 4 milliseconds. Clock correction operates continuously on a priority basis.

CARRIER AND CODE TRACKING

Figure 3 shows the basic operation of the carrier and code tracking loops.

In acquisition, the carrier NCO and code generator are operated in a search pattern that results in a correlation function being centered in the early/on-time/late correlator output. The on-time correlator complex (I and Q) outputs are used for carrier tracking, and an estimate of the angle of these coefficients yields the carrier-loop phase error. This is analogous to conventional Costas-loop carrier tracking. The carrier-loop error is filtered in the loop filter for second-order carrier-loop tracking. The carrier frequency estimate controls the

carrier NCO and also is scaled to control the code NCO frequency, and to provide dynamic aiding for the first-order code tracking loop.

The code loop derives its delay error signal from the difference of the magnitudes of the early and late correlation coefficients, in the manner of a noncoherent code tracking loop. The code loop is first-order, with aiding from the carrier loop, and controls the delay of the code NCO/code generator directly rather than the more usual process of controlling the code chip frequency. This control mechanism offers some significant advantages in achieving very-high-resolution time transfer measurement.

BASIC APPROACH TO TIME TRANSFER

Figure 4 is a functional block diagram of the GPS time transfer process, the basic element of which is the code track loop that keeps a local reference code synchronously tracking the received code. The initial phase or time delay of the reference code is controlled at the start of each loop iteration (4 milliseconds) by the feedback from the code loop filter. The control word from the loop filter is split into integer and fractional parts in terms of code chip units; the integer part sets the starting chip number of the code generator, and the fractional part sets the starting phase of the NCO.

This control mechanism for the combined NCO/code generator is very precise and eliminates the need for a high-resolution time interval counter to perform the basic time difference measurement between reference time and received code epochs. Figure 5 illustrates how the 43-bit integer delay sets the starting code chip, and a 32-bit control word initializes the NCO starting phase. This, in effect, sets the starting phase to a resolution of 2^{-N} part of a code chip, where N is 32 for a 32-bit accumulator in the NCO.

Figure 6 outlines the form of the NCO for this process. The NCO consists of an accumulator register that can be preset by the fractional chip phase command word from the code loop filter whenever each loop filter iteration begins. The frequency command word is then added to the accumulator on each clock time, causing the accumulator to overflow at an average frequency equal to the desired chip frequency. It is important in this process to maintain an asynchronous relationship between the NCO output frequency and the NCO accumulation rate over the entire Doppler range. When this is done, it is found that only the most significant bit (MSB) from the accumulator needs to be used as an NCO output, and it then advances the code generator a chip on each overflow of the NCO accumulator.

Although it may appear at first that such a code generation process would yield unacceptably high jitter in the code loop, this has not been the case, because of the broad spectral distribution of the NCO phase jitter. We use the same process in the carrier and code loops and see a phase jitter of about 2 degrees rms (for high-SNR signals) in the carrier track loop, as shown in Figure 7. Code track results are shown in Figure 8, which is a time history of the combined code NCO/code generator control words plotted for an actual satellite pass. No smoothing was used on the plotted data, in order to illustrate the resolution of the raw delay measurements.

Referring again to Figure 4, it can be observed that the nominal 4-millisecond loop iteration rate of the code loop is derived from the user clock. On each 4-millisecond loop iteration, an uncorrected time word in units of integer and fractional code chips is extracted from the code loop. This time word consists of the raw uncorrected time measurements that can be corrected for range, ionospheric error, relativistic error, satellite clock error, etc. They can be used as measurement values input to a Kalman filter to model various systematic and random clock errors. User clock error is determined by differencing with the user clock value at the same iteration time mark. The clock can be set to null the error by a combination of setting the clock counter in 200-nanosecond increments and, in finer increments, by phase control of the reference frequency input. Note (Figure 4) that uncorrected time measurements have a different significance, depending on whether the tracking mode is C/A- or P-code. In the P-code mode, the code state represents the time of the week (TOW) in direct unambiguous form. In the C/A-code mode, the TOW establishment and maintenance is somewhat less direct in that it involves a combination of measured C/A delay and resolution of the 1-millisecond C/A-code ambiguity.

DESIGN APPROACH

The components of the signal processor described in Figure 1 are designed to interface with the Motorola VERSAbus*. Figure 9 shows the particular configuration used for the P-code time transfer processor.

The VERSAbus concept provides a dedicated section for the microprocessor functions and a user-definable section.

The microprocessor bus supports a multiprocessor system that can be used to support auxiliary processors for navigation, clock error estimation, and special-purpose I/O and display functions.

Figure 10 is a photograph of the enclosure for this design. Typical circuit boards, which have the physical characteristics of a Motorola EXORmacs* board, are shown in Figures 11 and 12. The RF converter is

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packaged in a module so that it plugs into the enclosure in the same manner as the processor boards. The present design includes a CRT, disk, and printer in addition to the basic control panel.

This modular design approach provides extensive flexibility to define systems for custom applications.

REFERENCES

1. C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley Publishing Company, 1980.

2. P.C. Ould and R.J. Van Wechel, "All-Digital GPS Receiver Mechanization," *Proceedings of the National Aerospace Meeting*, The Institute of Navigation, 8-10 April 1981; also to appear in *Navigation*, Vol. 28, No. 3, Fall 1981.

3. T. Thompson, "Performance of the Satrack/Global Positioning System, Trident I Missile Tracking System," *Proceedings of the 1980 IEEE Position, Location, and Navigation Symposium*, pp. 445-449.

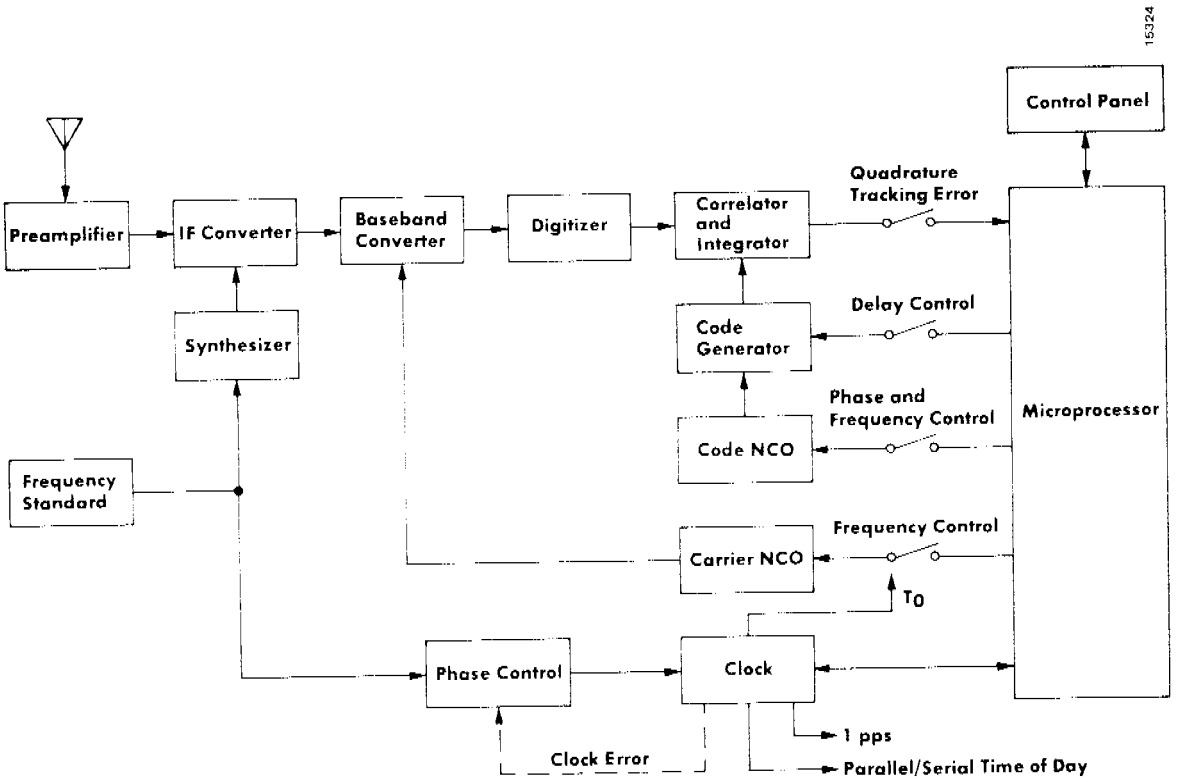

Fig. 1-Functional block diagram of GPS time transfer receiver

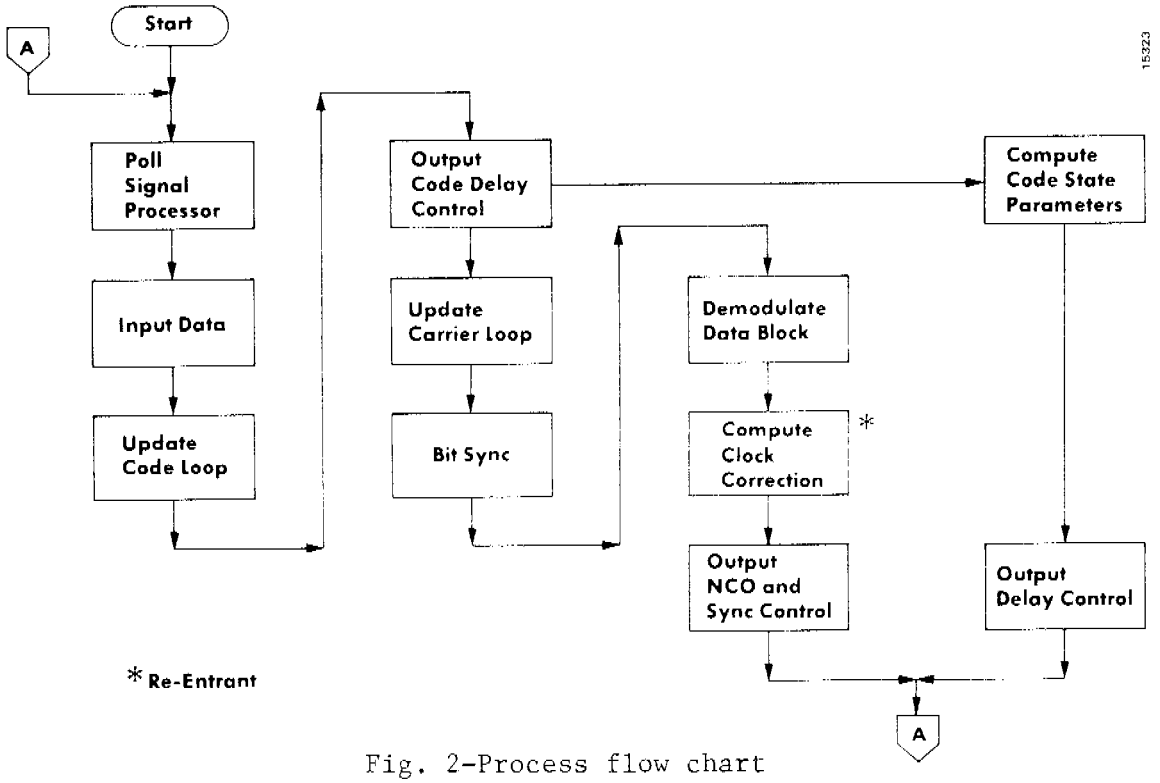

Fig. 2-Process flow chart

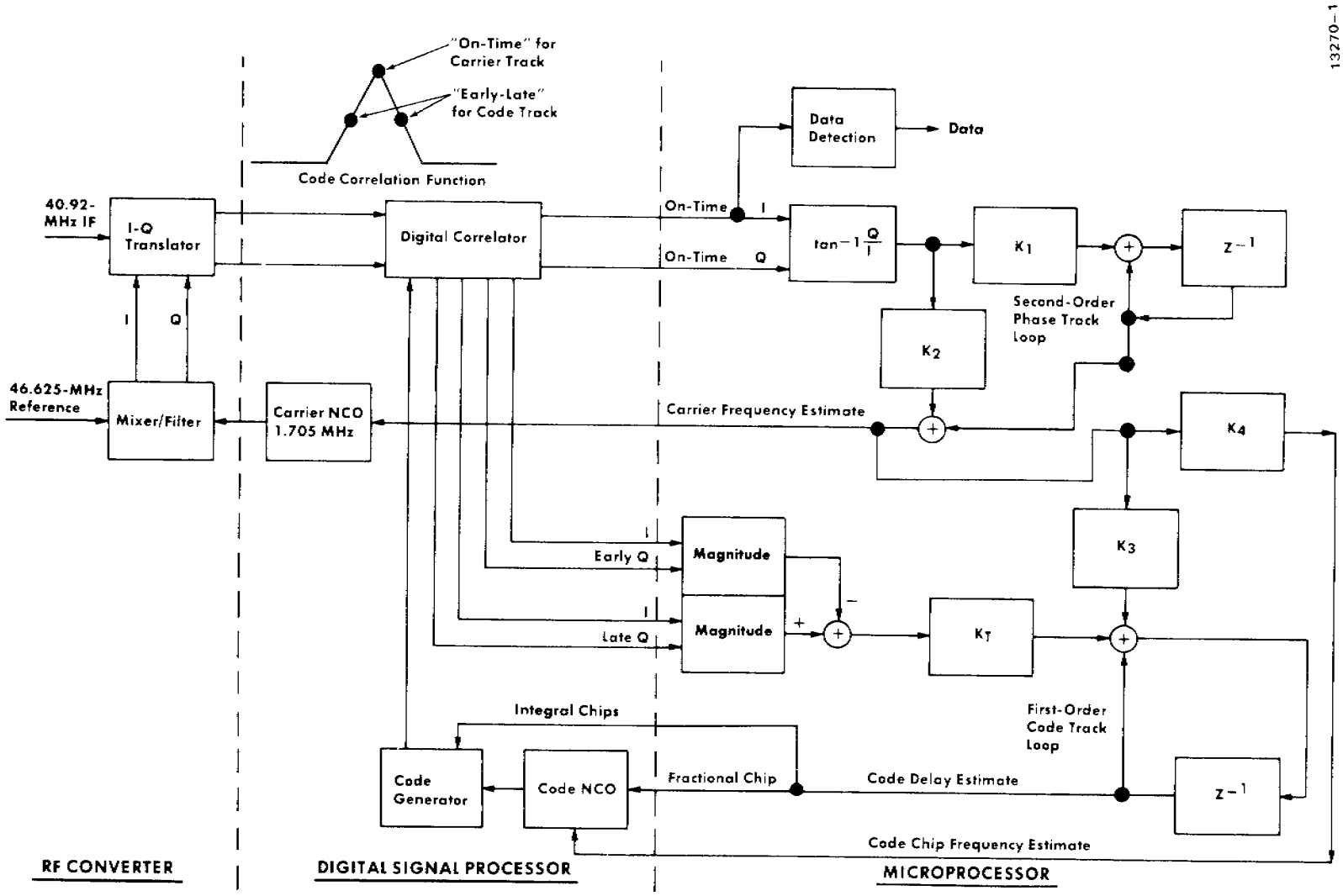

Fig. 3-Operation of carrier and code track loops

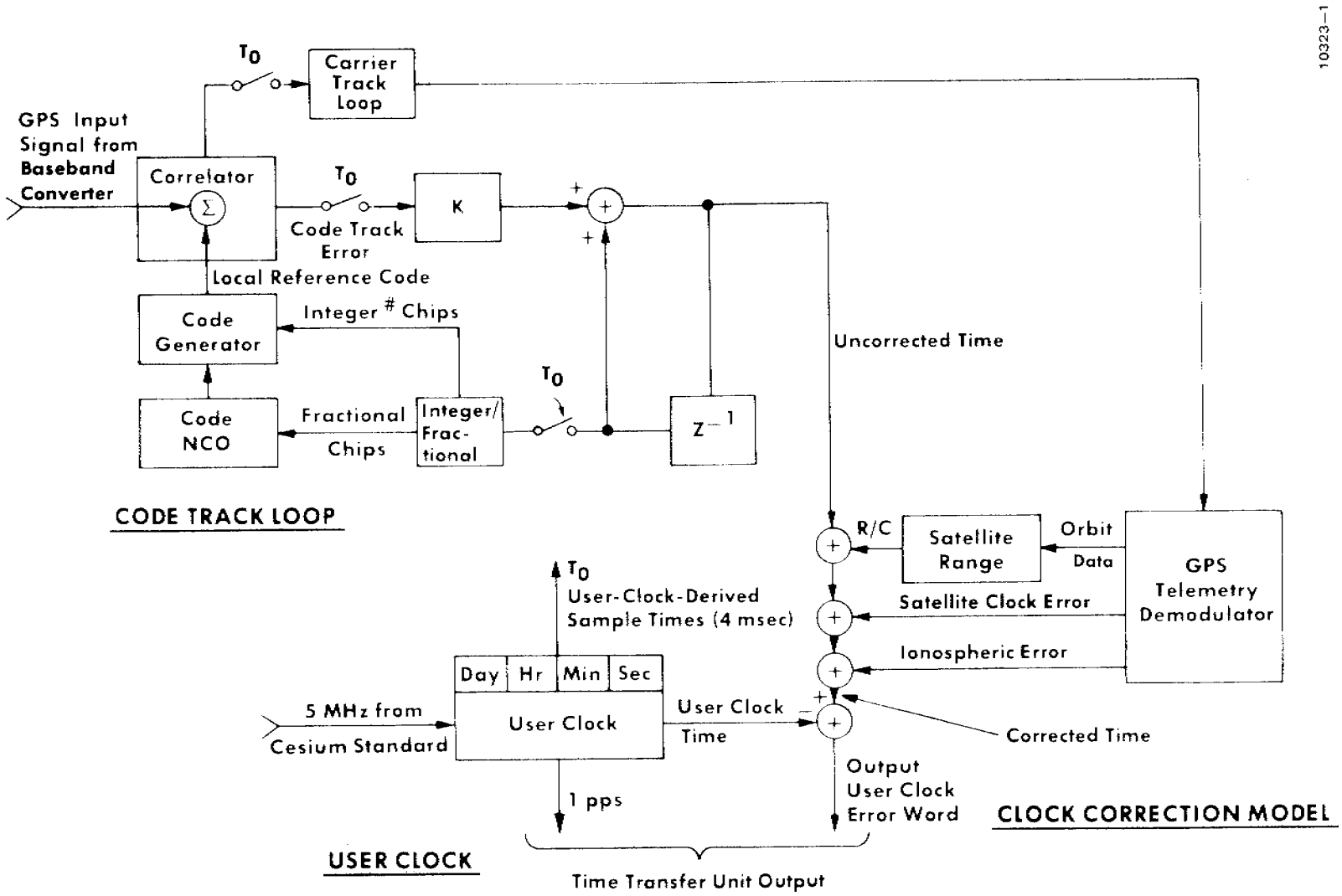

Fig. 4-Simplified block diagram of GPS time transfer process

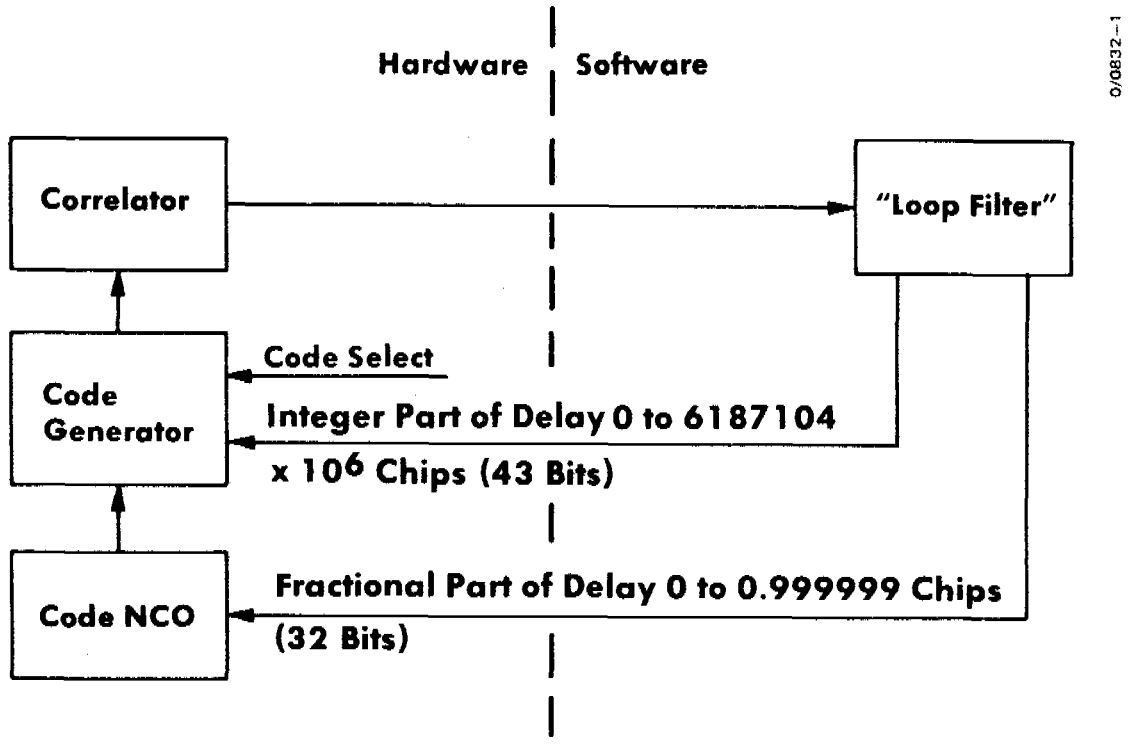

Fig. 5-NCO/code generator control

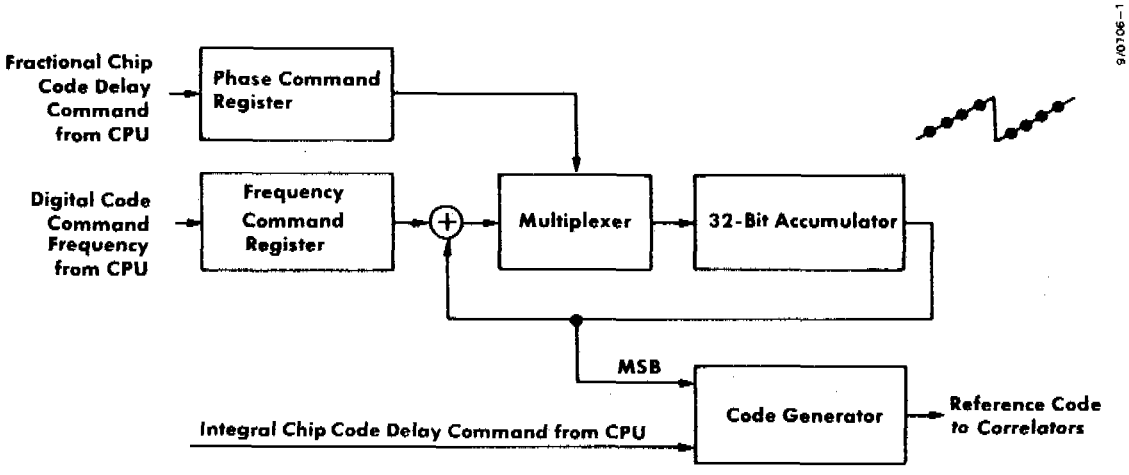

Fig. 6-Code NCO function

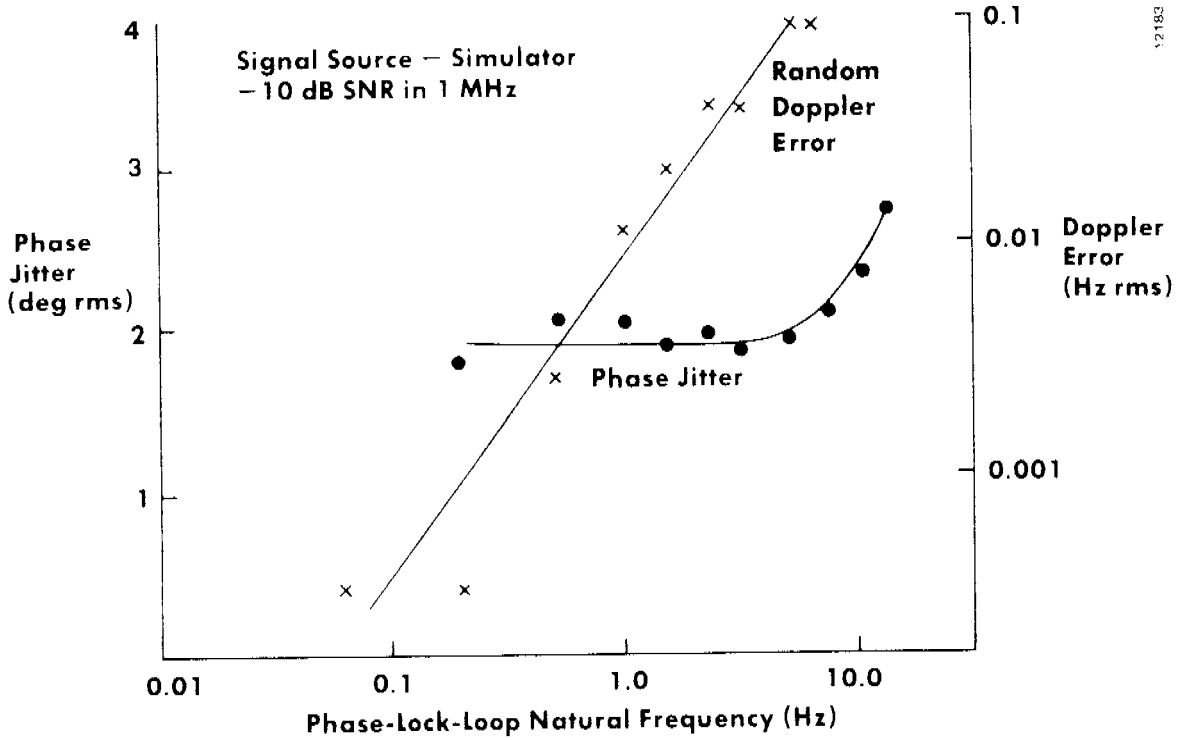

Fig. 7- Measured phase jitter and random Doppler error vs loop bandwidth

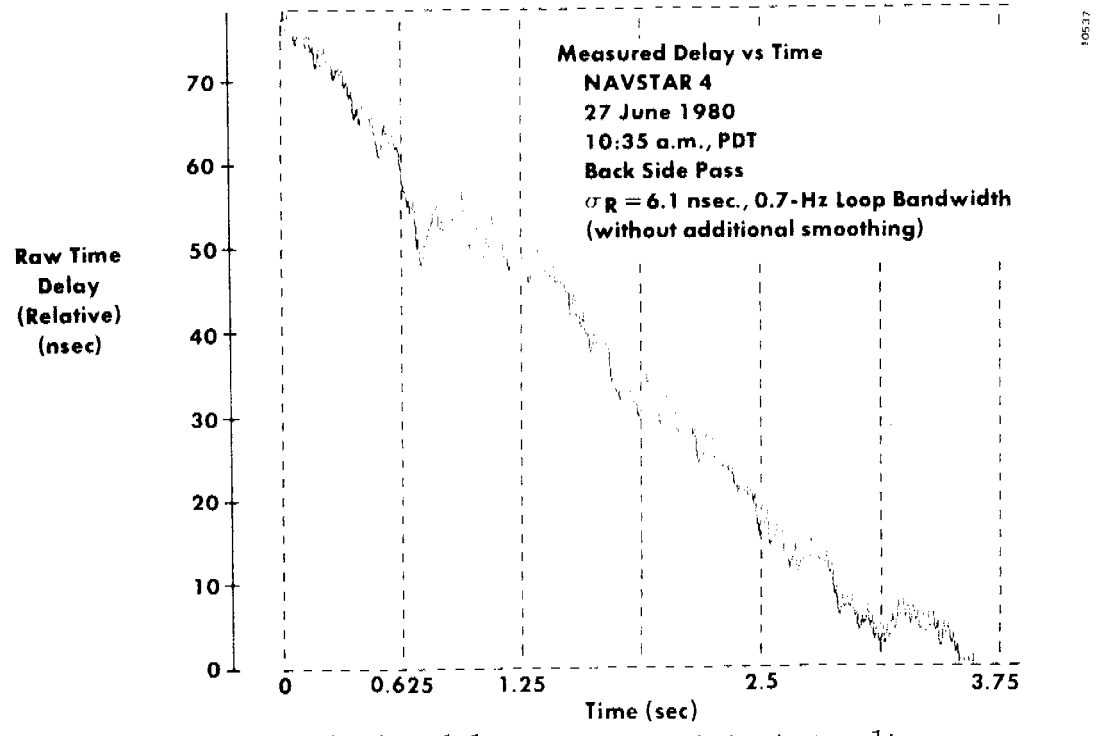

Fig. 8-Typical time-delay measurement test results

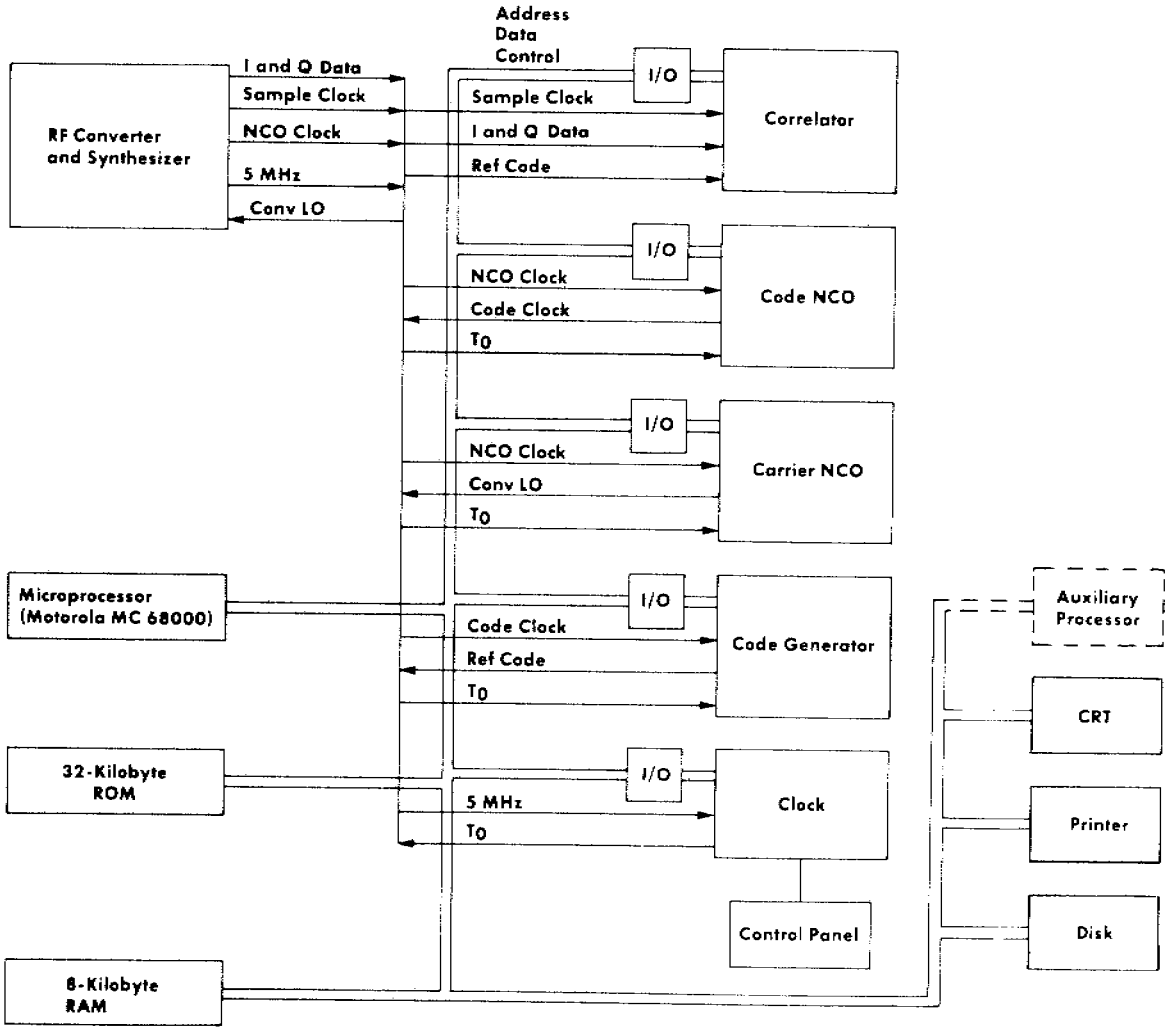

Fig. 9-System architecture

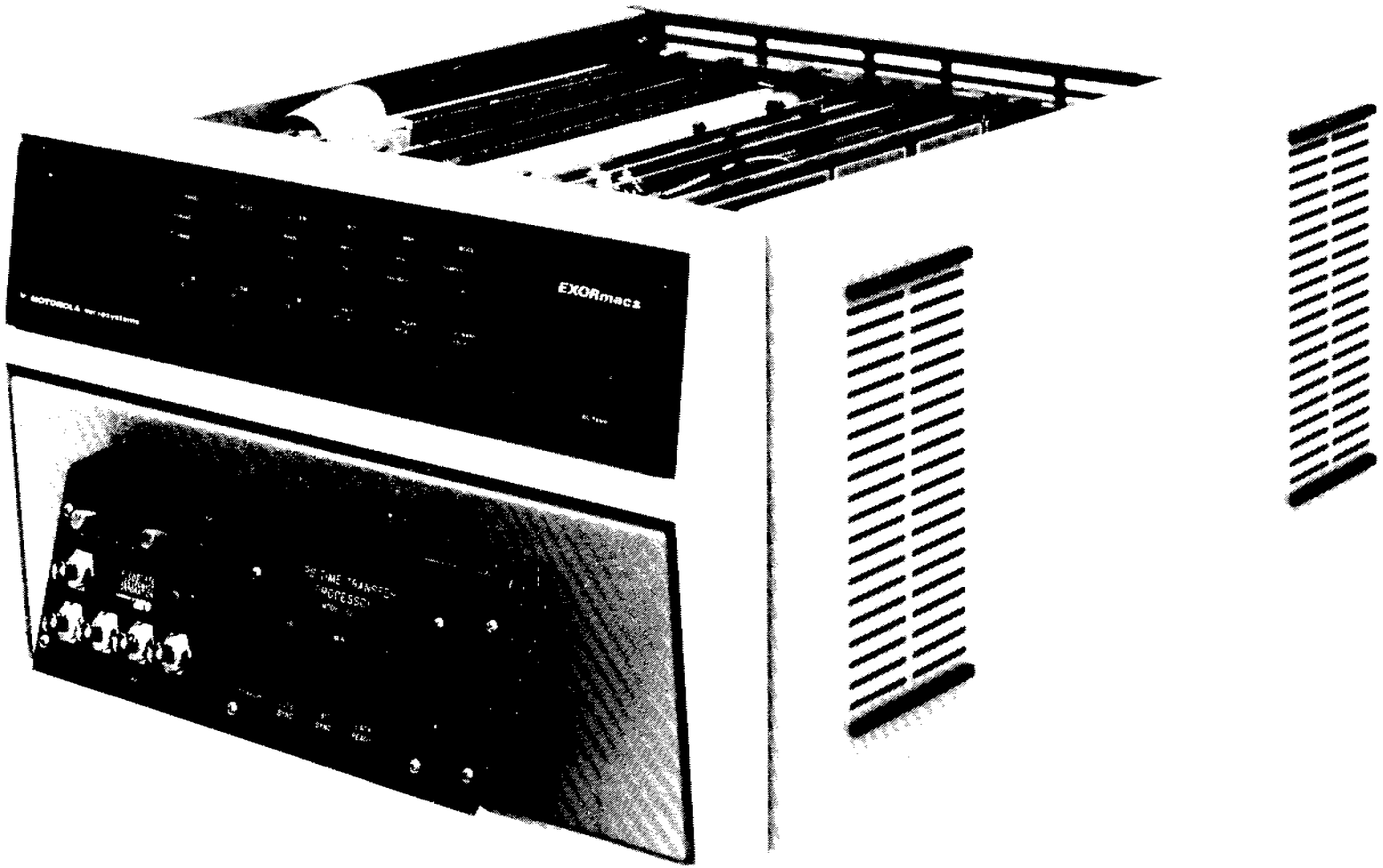

Fig. 10-Time transfer unit chassis

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Fig. 11-Correlator printed-circuit board

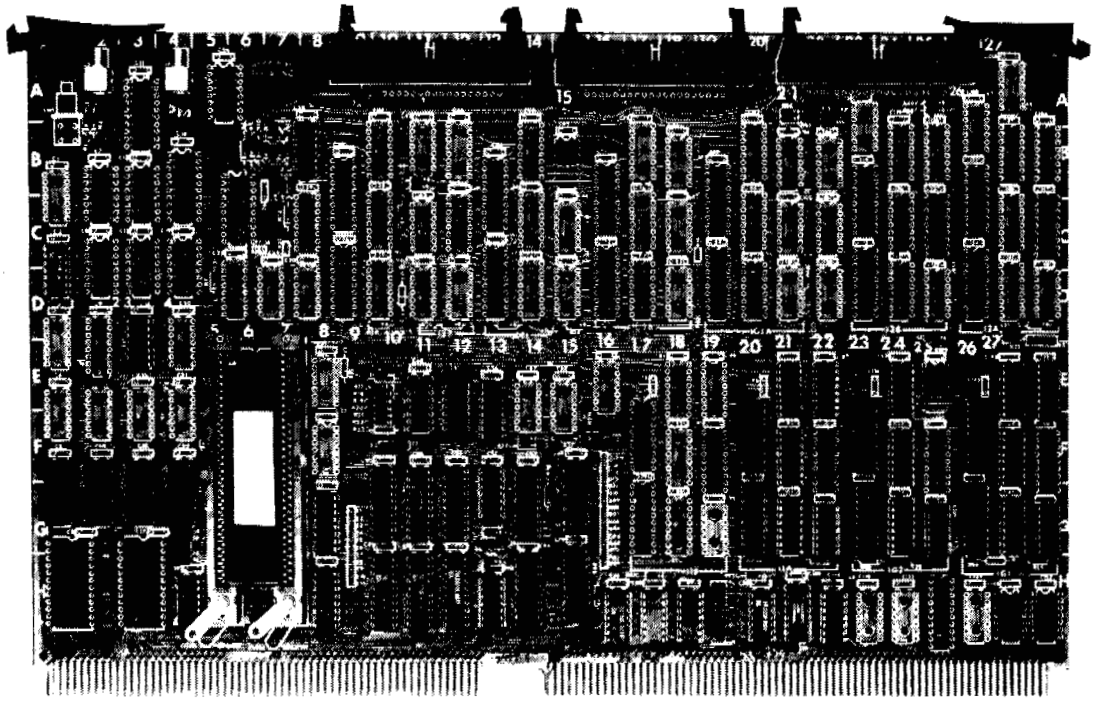

Fig. 12-Code generator printed-circuit board

DR. VICTOR REINHARDT, NASA/Goddard

Do you have any idea when this will be available, and do you have any idea what the cost will be?

MR. OULD:

Available to carry away or observe?

DR. REINHARDT:

Available to carry away.

MR. VAN WECHEL:

Probably another year.

MR. OULD:

We could conceivably do it in six months, but I would hate to promise anything short of a year and that is primarily because we're a very limited staff. We're only talking about three to six people, and right now we're down to the three-people limit, and you are looking at two of them.

And Jim is back, just before we left, the RF Section crashed, and that is his responsibility. And yet that is the three people. So, I'd be sticking my neck out to promise anything short of six months to a year.

DR. REINHARDT:

Do you have any idea of what the cost would be?

MR. OULD:

I'd really rather not say right now. We, you know, being small, Interstate is not a product house, okay. We're in to this development. It is totally funded by the company. We are in to it because we can support the Trident Missile testing. That is our intent. Time transfer for the ranges, et cetera. I had to beg off on it like that.

MR. VAN WECHEL:

Tell him to come and see us afterwards.

MR. OULD:

Come and see me at coffee break.

DR. REINHARDT:

Thank you.

MR. ED CHRISTY, Offshore Navigation

I have two questions. One, were you receiving both the L-1 and L-2 channels in the receiver? And, secondly, you mentioned a synchronous sampling rate in your digitizer. Approximately what frequency of digitization were you employing?

MR. OULD:

Okay. Question one, L-1 only.

Question two, you know 20.462046 megahertz. In other words, it's a 10 to the fourth higher than the chip rate.

MR. CHRISTY:

And you digitized this to 16 bits at that rate?

MR. OULD:

No, we're digitizing to one bit at that rate.

MR. VAN WENCHEL:

Can I say something here?

MR. ALLAN:

Yes, please.

MR. VAN WENCHEL:

That chip rate is chosen to be outside of the Doppler range, that is the idea of the asynchronous sampling so that the sample rate never becomes coherent with the chip rate. If it ever becomes coherent, especially with one bit quantization, you get in big trouble because you have very course quantizing of the phase.

So, you choose it to be just outside the Doppler range, and that's why the one part in ten to the fourth.