EFFECT OF VARIOUS FEATURES ON THE LIFE CYCLE COST OF THE TIMING/SYNCHRONIZATION SUBSYSTEM OF THE DCS DIGITAL COMMUNICATIONS NETWORK

D. B. Kimsey
Harris Corporation
Melbourne, FL

ABSTRACT

This paper reports the results of one task of a study, the purpose of which includes evaluating the advantages and disadvantages of implementing a set of optional timing/synchronization features in the future DCS digital communications network. The task reported on in this paper examines the effect on the life cycle cost of the timing subsystem when these optional features are included in various combinations. The features include mutual control, directed control, double-ended reference links, independence of clock error measurement and correction, phase reference combining, self-organization, smoothing for link and nodal dropouts, unequal reference weightings, and a master in a mutual control network.

An overall design of a microprocessor-based timing subsystem was formulated. The microprocessor (8080) implements the digital filter portion of a digital phase locked loop, as well as other control functions such as organization of the network through communication with processors at neighboring nodes. Other components of the subsystem include: extended-range linear phase detector, overhead interface, frequency standard, frequency or phase correcting apparatus, elastic buffers, and frequency synthesizers. A packaging scheme based on double-sided printed circuit cards was chosen. The particular packaging scheme was familiar to the author and is not claimed to be optimal for the application.

Seventeen timing subsystem configurations containing various combinations of the features were designed in enough detail to obtain reasonably reliable parts counts and estimates of the number of lines of code required for the 8080 routines. A hypothetical 200-node network (believed to be representative of a worldwide defense communications network) was used as the basis

for the life cycle cost analysis. For each of the seventeen configurations, the acquisition and life-cycle costs were computed based on 200 installations and a 20-year maintenance time.

The hardware acquisition and life-cycle costs were calculated using the RCA PRICE program (Programmed Review of Information for Costing and Evaluation). PRICE is a proven parametric cost estimating model which provides reliable estimates of system development, production, and maintenance costs. Software costs were calculated manually based on previous experience with development of 8080 software. Results of the pricing are presented in tabular form for each comparison.

INTRODUCTION

Various optional features may be included in the design of a synchronization subsystem to improve its performance. A companion paper [1] reports the performance effects of including such features. The features include mutual control, directed control, double-ended reference links, independence of clock error measurement and correction, phase reference combining, self-organization, smoothing for link and nodal dropouts, unequal reference weightings, and a master in a mutual control network.

The hardware and software implementations of the Timing Subsystem features are addressed in this paper. Seventeen Timing Subsystem configurations possessing these features in all practical combinations were designed and their life-cycle costs were determined. The costs of these configurations may be used in conjunction with the performance evaluations in [1] to evaluate performance versus cost trade-offs.

The Timing Subsystem consists of all components not included in the radios, modems, multiplexers, data terminals, etc., which are necessary to provide timing for and to synchronize data transfer between said equipments. The broad categories of these components are: local reference, buffers, timing generation and distribution, and optional disciplining circuitry.

Conceptual Design

Figure 1 shows the assumed multiplexer hierarchy used for the design analysis. It should be noted that a new generation of equipments may be desirable for use in the future synchronous DCS. The Timing Subsystem was designed around the present equipment specifications as much as practical, and the resulting Timing Subsystem costs may be somewhat higher as a result.

Figure 2 is a generalized block diagram of the Timing Subsystem. The system depicted here contains the maximum hardware and can implement all of the optional features. The detailed implementation of each of these components is described below.

The elastic buffer absorbs rate variations between the received timing and the local clock. An elastic buffer is placed between each of the two channels of the digital radio and the two corresponding TD-1193 Demultiplexers. (Only one is shown for brevity.) These buffers could be placed lower in the demultiplexer hierarchy, resulting in a larger number of smaller, slower buffers. An analysis of optimum buffer placement was not included in this effort; they are assumed to be between the radio and highest-level demultiplexer for ease of analysis.

Approaches which discipline a clock based on time of arrival of link timing signals require a sync extractor and phase detector. The sync extractor searches the mission bit stream for the TD-1193 sync patterns. The phase detector measures the time differences between the predicted and actual arrival times of these sync patterns. The time differences (phase errors) are inputs to the phase-locked loop which serves as the local time reference.

The processor inputs these phase errors and calculates the difference equations which implement the digital loop filter. The output samples from this filter discipline the nodal clock. They may control a VCXO (voltage controlled crystal oscillator) via a D/A (digital-to-analog) converter, or may discipline a crystal or atomic standard by shifting its phase via an outboard phase shifter. The nodal clock drives the frequency synthesizers which produce all phase-related timing required by the multiplexers, radios, modems, etc., and all demultiplexers which are lower in the hierarchy than the elastic buffers.

Timing approaches which employ overhead information require an overhead interface which allows information to be exchanged between processors on opposite ends of the link. It is assumed that this information is transmitted through a low-speed channel (300 b/s) of the orderwire multiplexer (LSTDM).

Each of the features described below was analyzed to determine its hardware and software requirements.

Implementation of Features

Directed control requires at least one sync extractor and phase detector in the system. For single-ended systems, the input to this circuitry is multiplexed so that it may connect to any one of the incoming links. This feature also requires a loop filter (processor) and means for controlling the local clock.

Double-endedness under Directed Control requires that the phase error measurement be made on each end of the link and that the master transmit its measured phase error to the slave via the overhead channel. The local node must contain a sync extractor and phase detector for the link to which it is slaved, and a sync extractor and phase detector for each neighboring node which is slaved to the local node. Further, the local node must contain an overhead receiver for the link to which it is slaved, and an overhead transmitter for each neighboring node which is slaved to the local node.

Double-Endedness under Mutual Control requires an overhead transmitter and receiver for each connecting link.

This feature also requires an additional computation (subtraction and division by 2) to be performed by the processor. Under Mutual Control, this computation is required for each connecting link.

Independence of clock error measurement and correction is only implemented after implementing both Directed Control and Double-Endedness. No additional hardware is necessary. The Master transmits its measured-but-uncorrected error (relative to the ultimate master) to the slave along with the measured phase error used for double-endedness. The slave subtracts this number from the result of its double-endedness calculation. Thus, only a minute amount of additional software is required. It should be noted that the Master node could combine these two numbers and transmit them as one number, thus requiring no additional bandwidth.

Phase reference combining is implemented only after implementing Directed Control, Double-Endedness, and Independence of Measurement and Correction. The local node derives timing from all nodes not lower in the hierarchy, and therefore must contain a sync Extractor and phase Detector for each of these links. Further, all nodes not higher in the hierarchy derive their timing in part from the local node. Since a double-end measurement is used, a sync extractor and phase detector are required on these links. Thus, a sync extractor and phase detector are required for each link.

The usual overhead transmission required for double-endedness, plus the measured-but-uncorrected phase error and a variance estimate, must be received from all nodes not lower in the hierarchy. The same three information types must be transmitted to all nodes not higher in the hierarchy. Thus overhead receivers are required on all links connecting to nodes not lower in the hierarchy, and overhead transmitters are required for all links connecting to nodes not higher in the hierarchy. For example, if the local node connected to three nodes higher in the hierarchy, three nodes of the same level, and four nodes lower in the hierarchy, it would require six receivers, and seven transmitters.

Additional software is required to implement Phase Reference Combining.

Rule 11, as described by Stover [2] requires the three data types to be exchanged in both directions on all links. This additional information is used for diagnostic purposes only, and is not required for implementing Phase Reference Combining. If Rule 11 is implemented, then overhead receivers and transmitters are required on all links, and additional software is required.

Self-organization requires overhead information to be passed in both directions over all links, i.e., the processor at the local node has full duplex communication with the processors at all neighboring nodes. Thus, an overhead receiver and transmitter is required on each link.

Additional bandwidth and processing are also required. For a Directed Control System not containing Phase Reference Combining, each node selects the best link to serve as its reference based on three data types: nodal rank, distance from master, and link demerit. This scheme is used in the earlier Time Reference Distribution [3] and adheres to rules similar to those of Darwin and Prim [4]. If Phase Reference Combining is included, the self-organization feature is implemented differently. The local node does not have to select the best link for its reference since it is always deriving timing from all neighbors not lower in the hierarchy. However, it must know at all times which of its neighbors are higher, lower, or on an equal level within the hierarchy. Two information types, INFO 1 and INFO 2, are employed for this determination.

Mutual control requires a sync extractor and phase detector on each incoming link. In addition to the loop filter software (which is of equal complexity with that required for Directed Control) the Mutual Control feature requires a weighted average of the phase errors derived from the individual links.

HARDWARE/SOFTWARE REALIZATIONS

The various components shown in Figure 2 were designed in enough detail to determine a parts list plus space and power requirements. A standard packaging scheme widely used at Harris ESD was selected as the basis for design. No claim is made that this packaging scheme is optimal for this particular application. This scheme employs 4.5 inches x 5.25 inches double-sided printed circuit (PC) cards which plug into motherboards via 80-pin connectors. A drawer was designed to meet the EMI requirements which have been specified for such equipments as the digital radio and various multiplexers. Two motherboards (each holding up to 23 cards) can be mounted horizontally in the front of the drawer, with enough room in the rear for power supplies.

Two drawers were necessary to house the circuitry for most configurations. It was deemed desirable to separate the components which would be common to all approaches from those which would be configuration dependent. Components common to all approaches are the frequency synthesizers, distribution amplifiers, and elastic buffers. These components were packaged in a single drawer herein called the Basic Drawer, which is constant across all configurations. This drawer was included in the cost figures to keep the cost of the various features in perspective; its cost may be easily factored out to more closely compare the costs of the various approaches used in the second drawer (herein called the Disciplining Drawer).

With the exception of the frequency synthesizers, which contain some ECL (Emiter-Coupled Logic), the designs incorporate the more economical and less power consuming low-power Schottky TTL (Transistor-Transistor Logic). Both drawers contain power supplies and motherboard wiring sufficient to support the PC cards required for seven terminating links (the assumed maximum). It was assumed, however, that the average node would only interconnect with four other nodes. Thus the costing was accomplished assuming a main frame capable of supporting seven links, but populated with PC cards to support four links. The following paragraphs describe the implementations of the individual components.

Phase Detector

Figure 3 depicts the sync extractor and phase detector circuitry. The clock output from the digital radio and the local 10 MHz reference are divided down to a common 8 kHz where the phase comparisons are made.

Phase difference is measured by counting cycles of the 10 MHz reference between the rising edge of the 8 kHz wave derived from the link timing, and the falling edge of the 8 kHz wave derived from the local 10 MHz reference as shown by the diagonal arrows in Figure 3.

The detection of synchronization patterns occurring at some submultiple of 8 kHz (depending on the selected output rate of the TC-1193) results in pulses from the sync detector synchronizing the countdown chain to the received framing. A countdown chain from the local reference controls the time of departure of the local TD-1193's frames by synchronizing both the TD-1193 and the transmit portion of the digital radio to the local clock.

Accurate phase measurements are obtained by averaging the counts obtained in several successive measurements. Results from [1] indicate that a phase measurement needs to be read out no more often than 1.5 times per second, or every 0.667 ms. This would allow in excess of 5,000 successive measurements to be averaged. Averaging is simply accomplished by allowing the counts to accumulate in the accumulator

counter until readout time, and dividing by the appropriate constant. At zero phase error, an average of 625 counts will be accumulated for each measurement. If the interval counter is configured to accumulate 5,000 or more such measurements, the resulting granularity of measurement is approximately 2 ns which is better than the asymmetry of the link and the associated equipments and is thus more than an adequate measurement granularity. This phase detector has an extended range of ±62.5 μs. The sync extractor requires one PC card, and the phase detector requires two cards.

Loop Filter and Overhead Processor

In order to implement a filter with a time constant on the order of several days, a digital (as opposed to analog) filter is a necessity. An 8080 microprocessor was chosen to implement this filter. The processor card designed is a self-contained computer including 1K bytes of Programmable Read-Only Memory (PROM) and 1K bytes of Random Access Memory (RAM). This single card is sufficient to perform the loop filter function. An analysis of software requirements is presented in [1].

Computations and bookkeeping required for implementing the overhead functions can be handled by the same processor used for the loop filter. Memory requirements for these features are presented in [1]. When more than 1K bytes of program storage is needed, a 4K byte PROM card is added to the system.

Technology advances in this area can quickly obsolete the results of cost/performance studies. As of this writing, 2K byte and 4K byte PROM IC's are becoming available which can replace the 1K PROM on the processor card. Intel has recently announced an 8K byte mask programmable read-only memory (ROM).

Local Reference

The assumed crystal reference is a 5 MHz oscillator having a drift of 1×10^{-10} per day. It is a self-contained, rack-mountable unit with its own power supply and stand-by battery system. A voltage input of ±5 volts will deviate the 5 MHz output by $\pm 2 \times 10^{-8}$. The short term stability is 1×10^{-11}. Many manufacturers, including Hewlett-Packard, Austron, Vectron, and Frequency and Time Systems, Inc., offer very similar references of this type with approximately $3,000 price tags. A frequency doubler is used to obtain the 10 MHz.

The crystal reference is disciplined with the output voltage of a D/A converter. A frequency resolution of at least 10^{-11} and a range of 4×10^{-8} require 4,000 quantization steps resulting in a 12-bit requirement for the D/A. This range allows the oscillator to drift for

200 days before the center frequency must be mechanically adjusted. This is the approach which was costed. Use of a $\pm 3 \times 10^{-7}$ adjustment range with a 16-bit D/A would permit the same resolution with a reset interval of 8 years, which exceeds the 5 year MTBF of the reference. However, this arrangement would have a sensitivity of 150 μvolt per quantization step on the voltage input. It would be extremely difficult to prevent noise pickup of this amplitude from modulating the reference.

The assumed Cesium Clock is a Hewlett-Packard Model 5061A with the standby power supply and high performance tube options; total price is $22,750. This is a self-contained reference having an accuracy of $\pm 7 \times 10^{-12}$. The reference is disciplined by shifting its phase with an Austron 2055A Phase Microstepper costing $3,550. The Rubidium standard is a Hewlett-Packard Model 5065A with the standby power supply option; total cost is $8,575. This is a self-contained reference having a drift of $\pm 1 \times 10^{-11}$ per month. For disciplined approaches, its phase is shifted with the Phase Microstepper.

Overhead Interface

The Transmitter and Receiver portions of the Overhead Interface are shown in Figure 4. A total of 55 bits of information is required for implementing all optional features. Triplicating this figure results in 165. Adding 35 bits for framing and time of day information results in a total of 200 bits. Transmitting this information 1.5 times per second results in a 300 b/s data stream which may be transmitted via a standard 300 b/s channel of the LSTDM and the Digital Radio Orderwire. This information would only occupy 0.16 percent of the 192K bandwidth allocated for the orderwire.

The Transmitter accepts the information words 8 bits at a time from the 8080, serially transmits each word three times, and generates periodic framing information to allow separation of data on the receiving end. The Transmitter occupies one PC card.

The Receiver converts the serial stream to parallel, accumulates three successive words, votes to correct errors, and presents the parallel data to the 8080. A sync correlator detects the presence of the sync pattern and initializes the sequencer to pick out the words at the proper time. The Receiver occupies two PC cards.

Frequency Synthesizers and Distribution Amplifiers

The function of the frequency distribution system is to generate phase-related rates to clock all equipments which are to operate synchronously with the local clock. Such equipments may include all devices in the transmit hierarchy from data terminal equipment to the digital Radio, and all devices lower in the receive hierarchy than the elastic buffers.

built less expensively if the MUX and DEMUX do not have to operate from independent timing.

The 12.928 MHz data rate from the Digital Radio poses no difficult design problem for the Elastic Buffer. For an independent clock approach employing Cesium clocks and a 24-hour buffer reset interval, the required buffer size (at 12.928 MHz) would be 46 bits. For a Rubidium clock with a 10^{-11} per month drift, 6 month recalibration interval, and 24-hour buffer reset interval, the required buffer size is 270 bits. If disciplined nodes containing crystal clocks can be controlled to within 10 μs of the Master (within 20 μs of each other) then ±259 = 518 bits are required during normal operation. A node with a good crystal clock will drift an additional ±56 bits during the first 24 hours after being severed from the network. Provided this is enough time to get the link back up, a total of 630 bits are required based on the above assumptions.

Figure 6 is a block diagram of a 1024-bit buffer designed to operate at 12.928 MHz. For relatively small buffers commercially available FIFO's (First-In-First-Out Memories) are perhaps the best approach. These IC's contain the control circuitry for moving data bits forward whenever one is extracted from the output. The FIFO in this configuration need only operate at 1.616 MHz. Bits from the 12.928 MHz stream are serially accumulated and stored broadsize (eight at a time) at 1/8 the original rate. The FIFO array can be implemented with either four 64 x 4 IC's or with four 32 x 8 IC's. Both types are available which can operate at the indicated rates. Handshaking signals are available to allow the IC's to be cascaded. The additional circuitry in Figure 6 is required to initialize the buffer (inhibit output clock until it half fills) and to monitor overflow and underflow. Two of these buffers occupy one PC card.

LIFE CYCLE COST ANALYSIS

It was desired to determine the cost of adding each one of the optional features to a basic timing approach. However, it is not possible to examine the cost of each feature individually. Rather, due to commonality of required components, it is more feasible to cost all practical configurations which include the features in various combinations. The list of configurations simulated in [1] was chosen for costing, so that performance versus cost trade-offs may be made. It became readily apparent that many of the configurations were practically identical with respect to cost. Estimating cost differences between such configurations was beyond the precision of the methods used for costing, and such configurations were combined into one. This resulted in reducing the 16 configurations presented in [1] into ten slightly more general configurations. The independent clock approach was added for completeness, resulting in eleven configurations which were costed.

DCEC specification R220-77-2 describes such a system which operates from the 1 MHz outputs of the AN/GSQ-183 Loran Receiver. Table 1 is a list of rates from that specification along with the number of required outputs of each rate. A balanced low-level driver (MIL-188-114) must be used for each output. This system is being procured for use in the interim communication network (DCS II), and might possibly be useable for the future DCS.

The assumed design generates the rates of Table 1 from the output of the 10 MHz local reference. Each of these rates, as well as the 10 MHz, is a multiple of 8,000 b/s. The phase of these rates should be such that if each one (including the 10 MHz input) is divided down to 8,000 b/s, then the 8,000 b/s waveform from each countdown chain should be in phase. The rising edges of this 8,000 b/s waveform (or a submultiple thereof) should be used to initiate the frame departure in the TD-1193 and Digital Radio.

Figure 5 depicts the design of the frequency distribution system. Each family of rates is generated by a VCXO and countdown chain. The VCXO's are locked via a broadband phase-locked loop to the 10 MHz reference. Four PC cards were required to implement these phase-locked loops.

The line drivers were implemented with commercial devices having voltage swings similar to those of MIL-188-114 balanced drivers. Devices which conform rigidly to the MIL-188-114 specification are not commercially available and must be special-made. Some companies (such as Sperry) have developed hybrid circuits which can be produced on special order. Typical cost is $80 each. Table 1 implies that 220 such devices are required. This number of drivers required 18 PC cards in the assumed design.

Elastic Buffer

The Elastic Buffer absorbs rate variations between received data and the local clock. They may be placed anywhere in the Demultiplexer hierarchy as long as the point where timing is derived is higher in the hierarchy than the buffers. Demultiplexers higher in the hierarchy than the buffers derive their timing from the associated incoming links, and those lower in the hierarchy receive timing from the nodal clock.

Since all demultiplexers lower in the hierarchy than the buffers are synchronous with each other and with the multiplexers, channel outputs from such demultiplexers may be routed to channel inputs on any multiplexer for retransmission on another link. This is a strong argument for placing the buffers as high in the hierarchy as possible. Placing them between the radio and the TD-1193 makes tandeming at any level possible, including routing one of the radio channels directly to another radio for transmission. A multiplexer/demultiplexer set can be

These configurations are listed in Table 2 using the same configuration numbers as in [1] for clarity.

Software and Hardware Requirements

Software costs were computed based on number of lines of code. A line of 8080 code expands into one, two, or three bytes (or no bytes if a comment statement) with the average being slightly greater than 2 bytes per line. Twenty percent was added to the requirements presented in [1] to accommodate diagnostic software. Table 3 lists the software requirements in terms of bytes and lines of code. For configurations requiring more than 1K bytes of memory, the PROM card is added to the system.

As previously stated, the synthesizers, distribution amplifiers, and buffers were placed in a separate drawer (the Basic Drawer). This drawer is included in all configurations. Table 4 is a breakdown of its contents. A fractional motherboard indicates only part of it is wired. The motherboard wiring and power supplies will support the maximum (Max/Box) number of PC cards expected. Costs were based on the average number of PC cards.

All configurations, except Independent Clocks, contain a second drawer (the Disciplining Drawer). Table 5 is a breakdown of the components contained in this drawer for all configurations. The motherboards and power supplies vary in size with the configurations, and in each case support the maximum number of links. Table 6 is a breakdown of the PC cards whose quantities vary between configurations. Costs are based on the average number. The choices of numbers in some cases are rather subjective and are based on assumptions of the number of neighbors higher, equal, or lower in the hierarchy.

Costing Methodology

The Software and Hardware costing were performed separately. The RCA PRICE program was used for Hardware costs. At the time of the costing, the PRICE Software model was not available. The Life-Cycle Cost of a system is divided into three parts: Development, Production and Maintenance for the life of the equipment.

Development costs include equipment design and construction of prototypes. These costs are nonrecurring; i.e., they are independent of the quantity of systems to be built. Production costs include tooling up for production, material and labor for building each system, and labor for testing finished systems. Tooling includes procuring or building special equipment used for fabricating and testing the systems. Production costs are proportional to the quantity of systems, but the relation is not linear. Due to a "learning curve," the cost of

production on per system basis decreases with the number of systems. Much of the tooling is up front; however, retooling generally is necessary due to wear and breakage. Maintenance costs include test and repair labor costs, transportation, supply management, and purchase of piece parts.

Acquisition costs simply consist of development costs plus the costs to produce the desired number of systems. When considering Life-Cycle Costs, the Production Costs are modified to include production of spares and production (or purchase) of test equipment to support the system in the field for a specified number of years.

Generally, software costs are considered to be nonrecurring. The costs simply consist of writing the code. If the software is the same in all systems, the software costs are independent of the number of systems. A reasonable cost for developing code of this type is $15 per line. For the system under consideration, the programs must be "burned" into the PROM IC's for each 8080 or PROM card. This process is mechanized and may be considered to be part of the fabrication process. These costs are included in the hardware production costs by assuming the complexities of these cards to be slightly higher than otherwise would have been assumed. Thus no additional production costs for software were assumed.

Software maintenance is a euphemism invented in recent years to describe the costs of continually rewriting programs which were not written properly in the first place. Many of these "errors" result from simply not anticipating every possible situation with which the software might have to deal. Even after "thorough" testing, residual errors may become apparent only after very long periods of operation. As a result, some software support may be required for the life of the system. A figure of $5 per line per year has been determined as a typical figure for such support.

The Life-Cycle Costs for the hardware configurations were computed using the RCA PRICE (Programmed Review of Information for Costing and Evaluation). There are two programs involved: PRICE 83B computes Acquisition Costs, and Price L1 modifies the production costs and adds in maintenance to complete the Life-Cycle Costs. PRICE is a proven parametric cost estimating model which provides reliable estimates of system acquisition costs (development and production). The PRICE 83B program generates design to unit production cost, based upon variations in designs, performance, schedules, reliability, economic escalations, etc. The price inputs are primarily physical characteristics of the design concept. These include weight, volume, manufacturing complexity, platform, quantity, development schedule and production schedule. The outputs feature recurring and nonrecurring costs for development and production as well as a unit production cost value for each entry.

PRICE 83B also develops inputs for the PRICE L1 model for Life-Cycle cost (LCC).

The Life-Cycle Costs of a system of 200 nodes were computed based on a system lifetime of 20 years. The software costs were computed by the simple formulas stated above. Table 7 is a breakdown of the software costs for the various configurations.

Hardware costs were computed by a very detailed process. The hardware was described in detail to PRICE 83B which computed Acquisition costs. This process was performed by personnel who are very experienced with the operation of the PRICE Model. These descriptions were performed at the PC card level and were checked for reasonability. The PC cards were combined in the various combinations with purchase items (items such as power supplies and references for which catalog prices were used) to form the different configurations. Another output of PRICE 83B is the LC file which includes unit costs, computed MTBF and MTTR values, and other pertinent factors used by PRICE L1 to compute the Life-Cycle Costs. Editing this LC file gives the user the opportunity to provide all the information he can about the system. For example, the predicted MTBF's of purchase items were overridden at this point with actual values from the manufacturer. MTBF's for designed equipment were also checked and altered if unreasonable.

The L1 Model was then exercised on the LC file using the force structure of Fig. 7. The support philosophy adheres to DoD Directive 4151-16 which states that there shall be three echelons of support. Simple repair is performed at the organizational shop, and consists of fault isolation to an LRU (Line Replaceable Unit), replacement with a spare and shipment to a higher level for repair. Generally, repair to piece part is performed at an Intermediate shop if not too complex, and at a Depot otherwise. Since most DCS nodes will probably be located at major military installations, the Intermediate shop is considered to be a general repair shop local to the base. It was assumed that 25% of the nodes would be remote, so that a total of 150 Intermediate shops were used. A Depot was assumed for each of the three services who will support DCS.

CONCLUSIONS

Table 8 is a breakdown of the components costs for Configuration 16 (using crystal clocks). Table 9 gives the Life-Cycle Costs of the various configurations. These costs are based on crystal clocks for the disciplined approaches. Configuration 16 is repeated for Cesium and Rubidium. Configuration 17 is also given for both Cesium and Rubidium but not Crystal.

The prices obtained in Table 9 may be compared with the simulation

results for cost versus performance trade-offs. Comparing the costs of disciplined approaches using crystal clocks, they are all very close (about 25 percent total variation). A surprising result was that the Life Cycle Cost of most disciplined approaches using crystal clocks came out slightly higher than that of Independent clocks using Cesium clocks.

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4. G. P. Darwin and R. C. Prim, U.S. Patent No. 2,986,723, "Synchronization of a System of Interconnected Units."

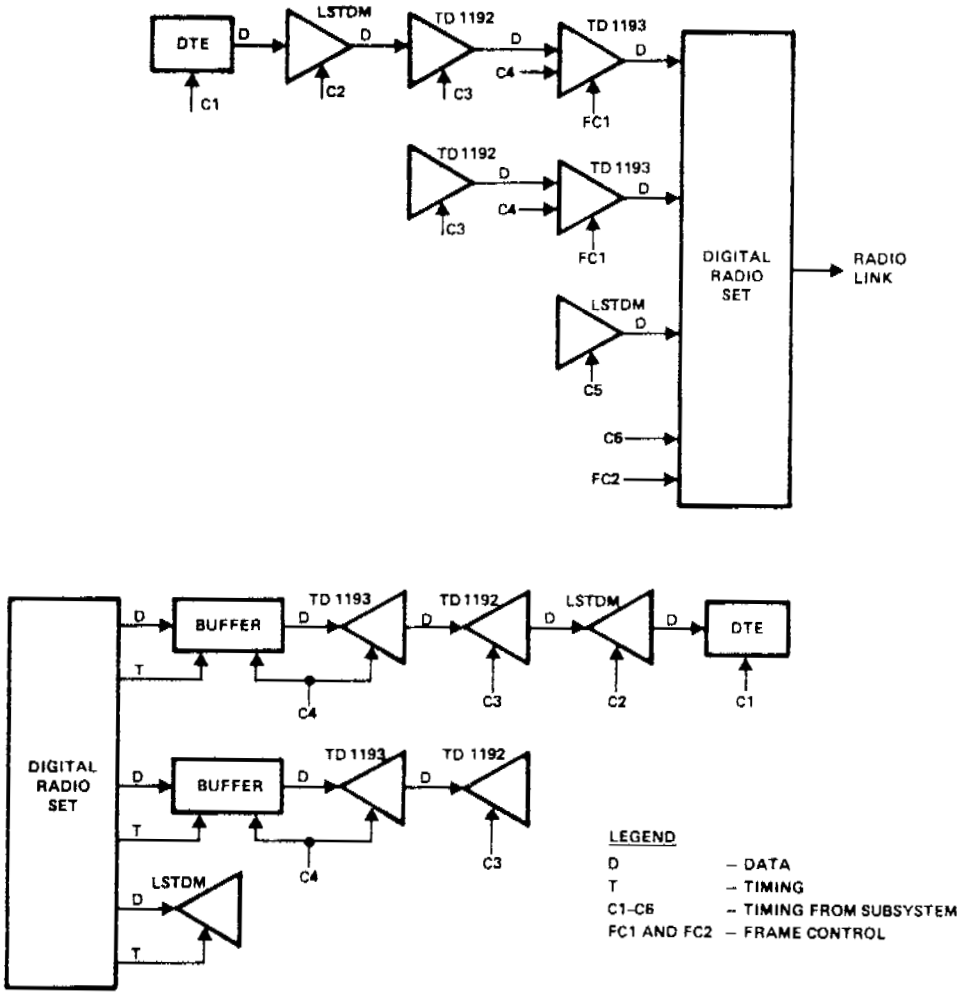


Figure 1. Transmit and Receiver Configurations

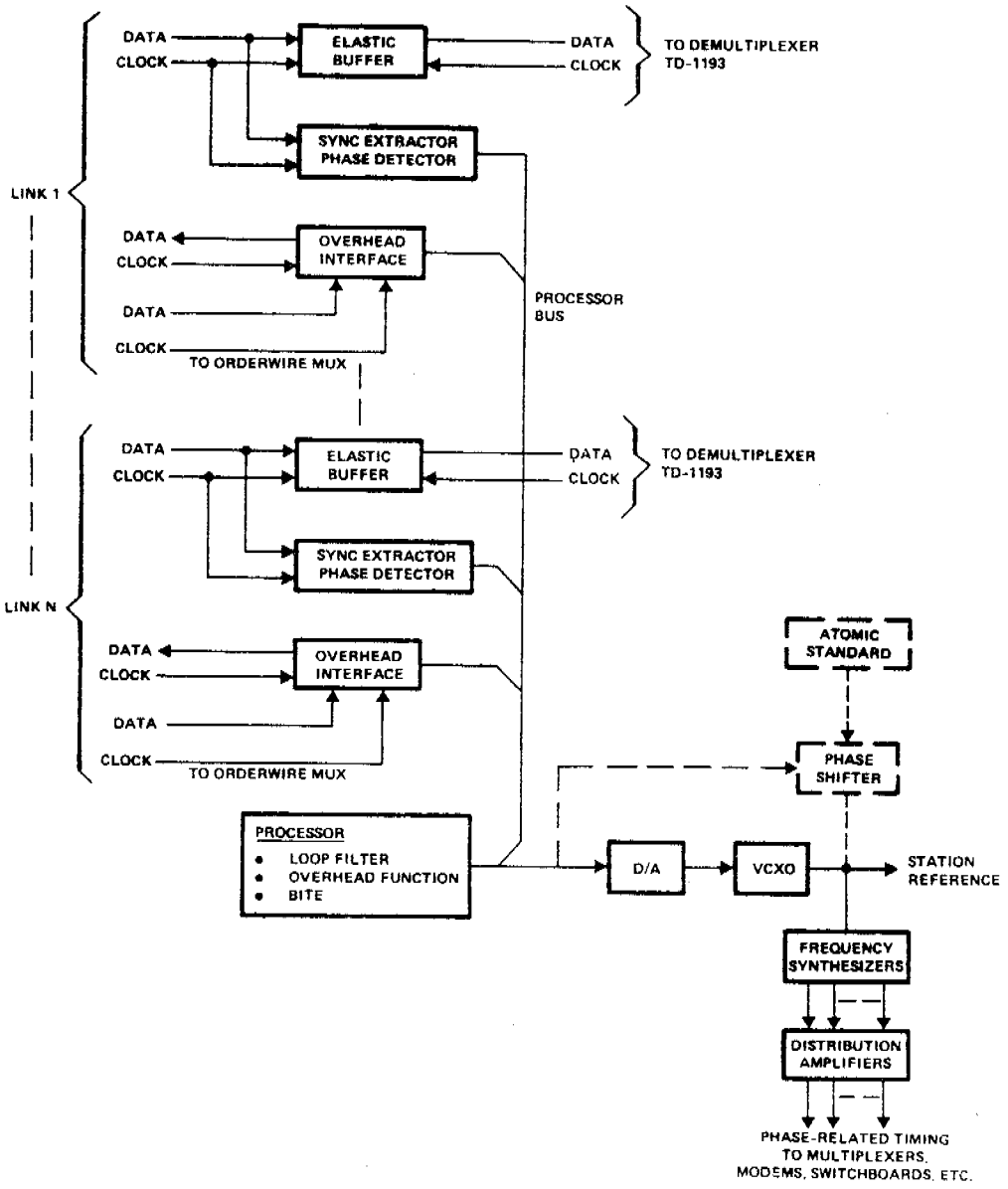


Figure 2. Timing Subsystem

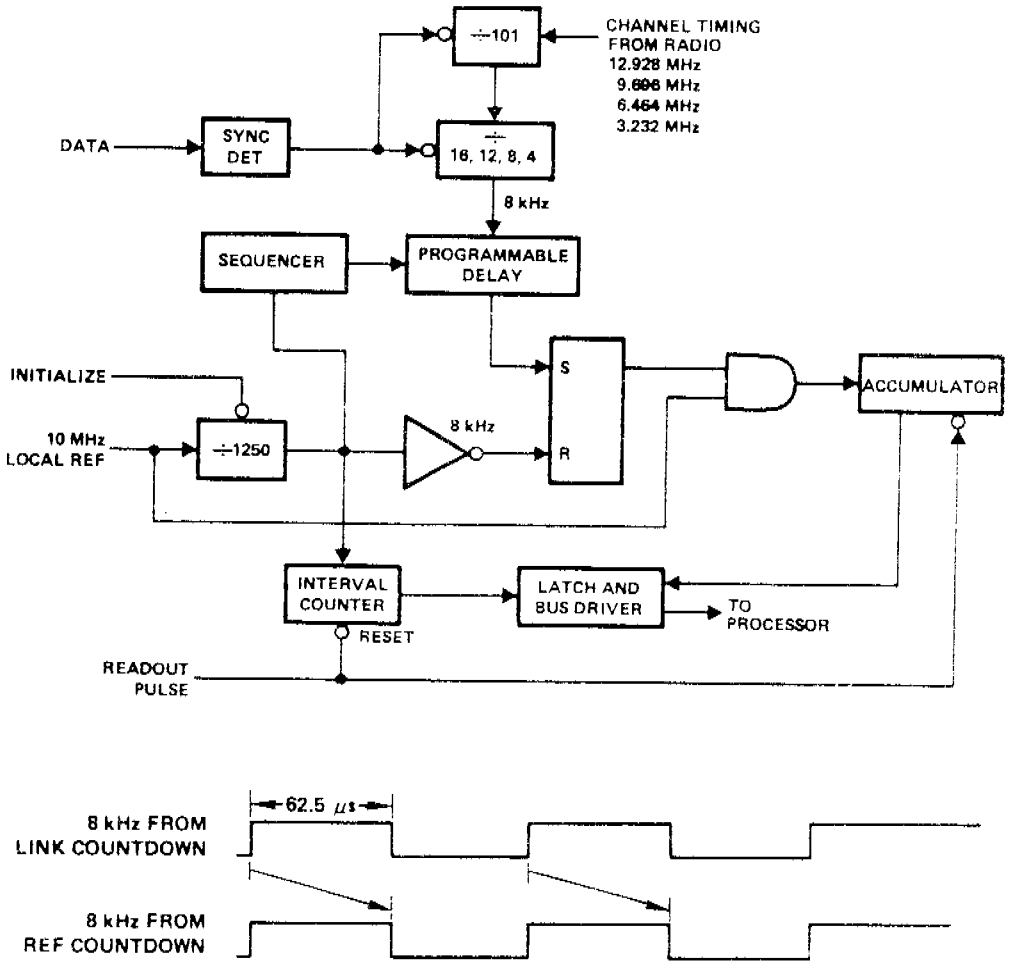


Figure 3. Phase Detector and Example Measurement

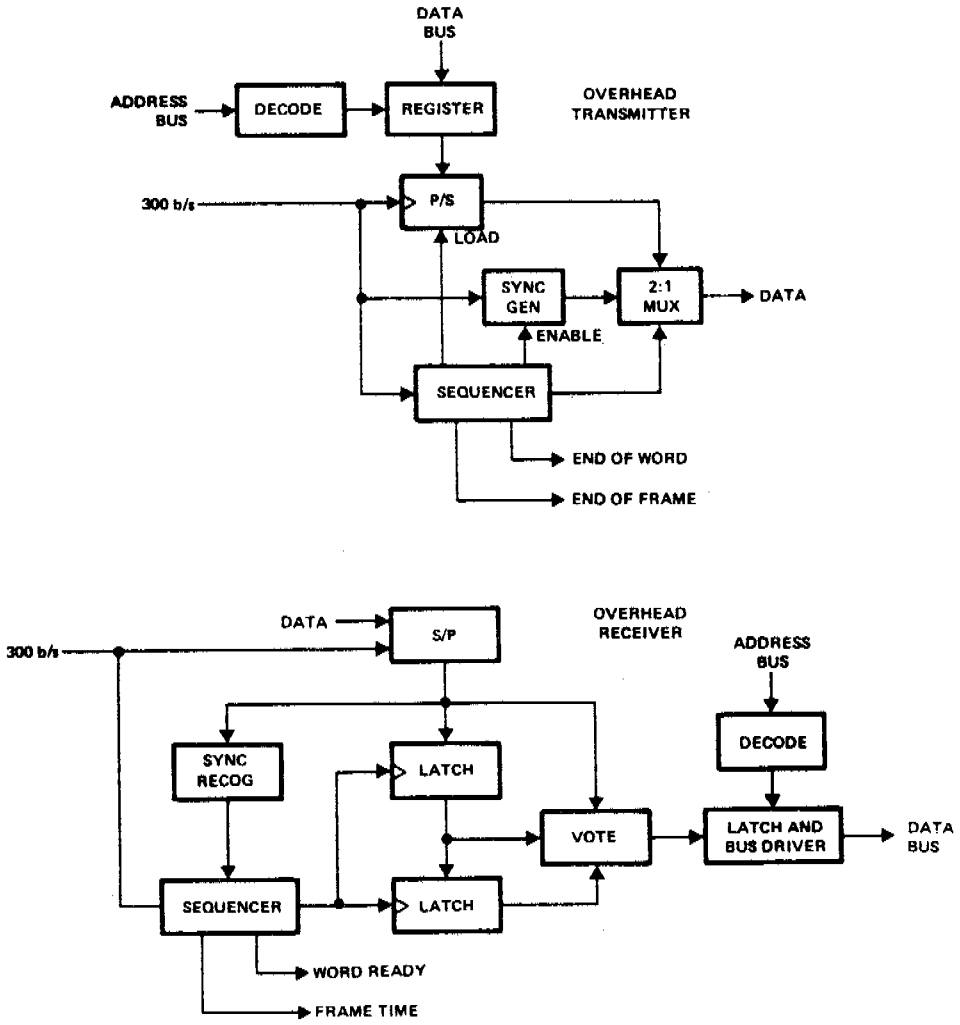


Figure 4. Overhead Interfaces

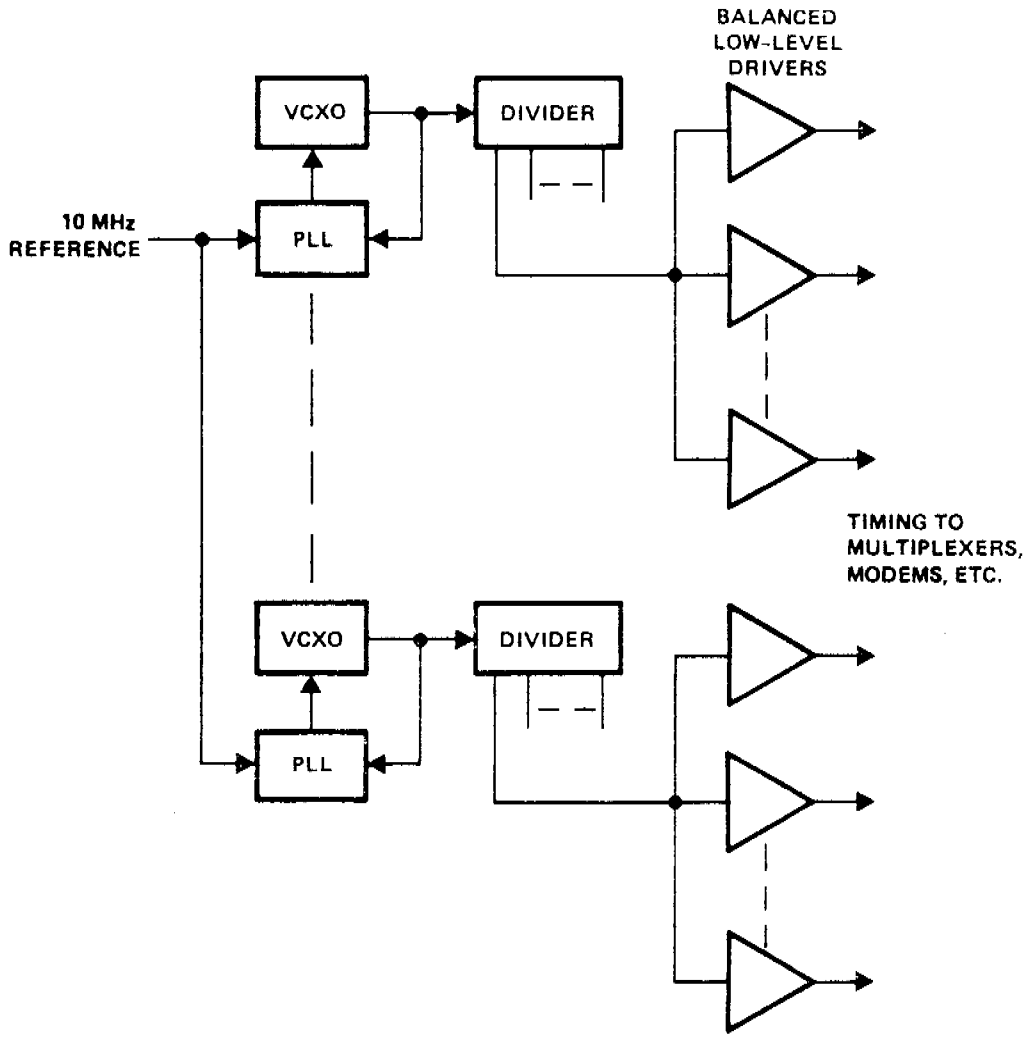


Figure 5. Frequency Synthesizers and Distribution Amplifiers

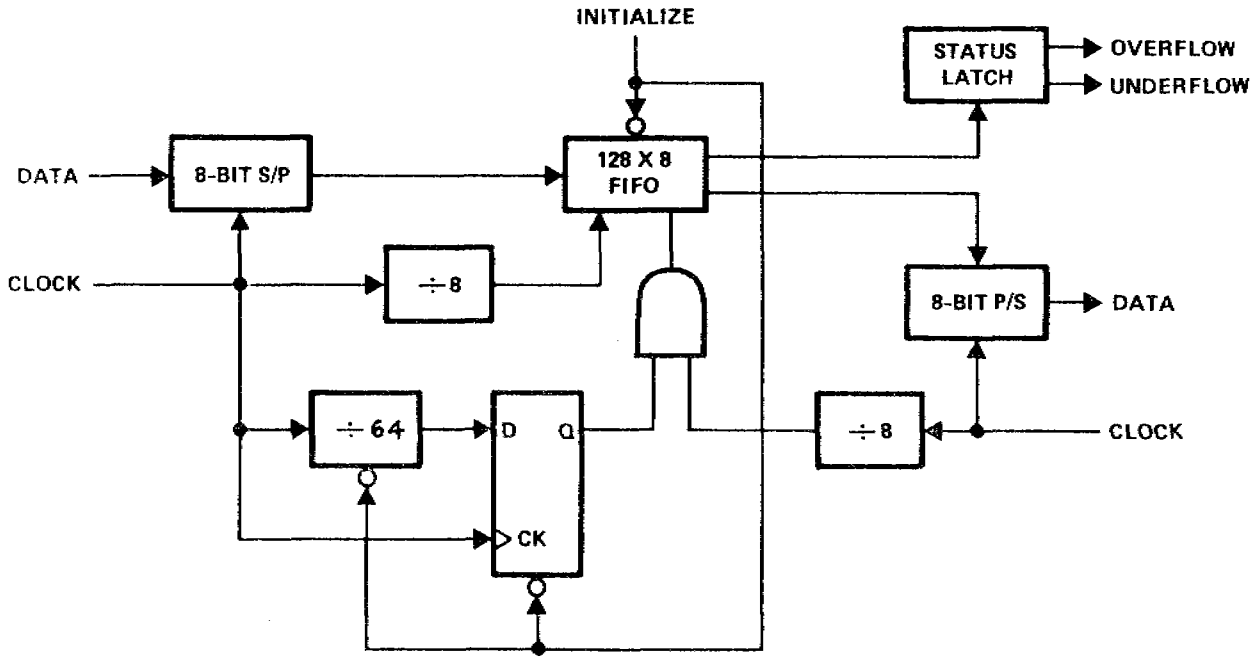
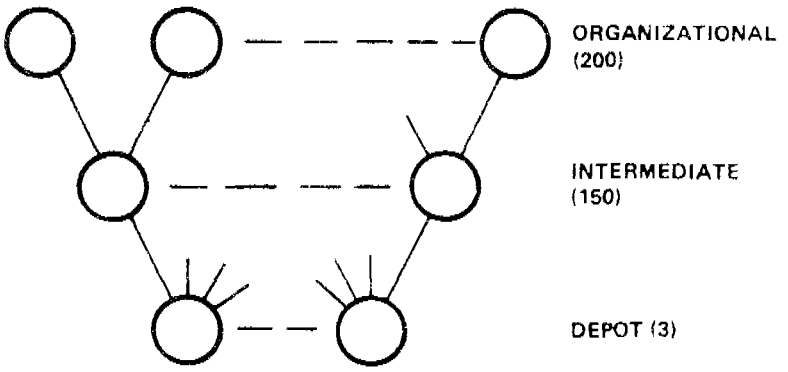


Figure 6. 1024-Bit Elastic Buffer



- SUPPORT YEARS – 20
- EQUIPMENT USAGE – 730.5 HOURS/MONTH (CONTINUOUSLY)
- PRICE 83B CHOOSES MTBF FOR DESIGNED ITEMS
- CATALOG VALUES USED FOR MTBF FOR PURCHASED ITEMS
- FOR RELIABLE ITEMS, NO SPARES AT INTERMEDIATE

Figure 7. LCC Assumptions

Table 1. Clock Frequencies and Maximum Number of Outputs Per Frequency

Clock Frequency Rates	Maximum Number of Outputs per Frequency Rate
16 kHz	25
32 kHz	10
56 kHz	15
64 kHz	10
128 kHz	15
256 kHz	15
512 kHz	10
1024 kHz	10
1544 kHz	60
2048 kHz	10
3.232 MHz	10
6.464 MHz	10
9.696 MHz	10
12.928 MHz	10

Table 2. Configurations for Costing

1-2.	Directed Control (Single-Ended)
3-7.	Mutual Control (Single-Ended)
8.	Directed Control, Double-Ended
9-10.	Mutual Control, Double-Ended
11.	Directed Control, Double-Ended, Independence of Measurement and Correction
12.	Directed Control, Double-Ended, Independence of Measurement and Correction, Phase Reference Combining
13.	Directed Control (Single-Ended), Self-Organizing
14.	Directed Control, Double-Ended, Self-Organizing
15.	Add Self-Organizing to Configuration 11
16.	Add Self-Organizing to Configuration 12
17.	Independent Clocks

Table 3. Software Requirements

Configuration		Lines	Bytes
1-2	Dir. Con., Sngl.	240	500
3-7	Mut. Con., Sngl.	360	760
8	Dir. Con., Dble.	440	920
9-10	Mut. Con., Dble.	630	1320
11	Dir. Con., Dble., IMC	480	1010
12	Dir. Con., Dble., IMC, PRC	1100	2310
13	Dir. Con., Sngl., SO	420	880
14	Dir. Con., Dble., SO	630	1320
15	Dir. Con., Dble., IMC, SO	670	1410
16	Dir. Con., Dble., IMC, PRC, SO	1300	2730
17	Ind. Clk.	0	0

Legend

Dir. Con. - Directed Control
Mut. Con. - Mutual Control
Ind. Clk. - Independent Clock
Dble. - Double-Ended
IMC - Indepencence of Measurement and Correction
PRC - Phase Reference Combining
SO - Self-Organizing
Sngl. - Single-Ended

Table 4. Basic Drawer Contents

Component	Ave./Box	Max/Box
Synthesizer 1	1	1
Synthesizer 2	1	1
Synthesizer 3	1	1
Synthesizer 4	1	1
Distribution Amp.	18	18
Dual Buffer	4	7
Motherboard	1.5	1.5
Supply (+5)	1	1
Supply (-5)	1	1
Supply (±12)	1	1
Drawer	1	1

Table 5. Disciplining Drawer Components

Component	Quantity
Processor	1
Controller	1
D/A	1
Supply (+5)	1 (Size Varies)
Supply (±12)	1
Supply (±15)	1
Motherboard	Varies
Drawer	1

Table 6. Disciplining Drawer Optional Components

	Sync. Ex.		Ph. Det.		OH Rcv.		OH Xmit		PROM
Configuration	Ave.	Max.	Ave.	Max.	Ave.	Max.	Ave.	Max.	
1-2	1	1	1	1	0	0	0	0	0
3-7	4	7	4	7	0	0	0	0	0
8	4	7	4	7	1	1	3	6	0
9-10	4	7	4	7	4	7	4	7	1
11	4	7	4	7	1	1	3	6	0
12	4	7	4	7	4	7	4	7	1
13	1	1	1	1	4	7	4	7	0
14	4	7	4	7	4	7	4	7	1
15	4	7	4	7	4	7	4	7	1
16	4	7	4	7	4	7	4	7	1
17	Not Applicable								

Legend

Sync. Ex. - Sync Extractor (1 card)
Ph. Det. - Phase Detector (2 cards)
OH Rcv. - Overhead Receiver (2 cards)
OH Xmit - Overhead Transmitter (1 card)
PROM - Additional 4K bytes memory (1 card)

Table 7. Software Costs (Thousands)

Configuration	Development	Maintenance
1-2 Dir. Con. (Sngl.)	3.6	24
3-7 Mut. Con. (Sngl.)	5.4	36
8 Dir. Con., Dble.	6.6	44
9-10 Mut. Con., Dble.	9.5	63
11 Dir. Con., Dble., IMC	7.2	48
12 Dir. Con., Dble., IMC, PRC	16.5	110
13 Dir. Con. (Sngl.), SO	6.3	42
14 Dir. Con., Dble., SO	9.5	63
15 Dir. Con., Dble., IMC, SO	10.1	67
16 Dir. Con., Dble., IMC, PRC. SO	19.5	130
17 Ind. Clk.	0	0

Table 8. Cost Breakdown for Configuration 16

	Qty	Dev	Prod	Support	Total	
Synth 1	1	29	72	185	287	
Synth 2	1	31	77	195	303	
Synth 3	1	46	71	188	305	
Synth 4	1	31	75	193	298	
Dist Amp	18	14	399	1403	1816	
Elas Buf	4	21	162	519	702	
Backplane	1	65	458	2	525	
Power 3	1	0	116	138	255	
Power 4	1	0	137	144	281	
Power 8	1	0	24	75	99	
Drawer	1	2	647	163	811	
I&T*	1	6	430	96	532	
Subtotals		245	2668	3301	4214	(Basic Box)
PC1	4	18	103	305	426	
PC2	4	19	103	329	450	
Syncex	4	33	117	406	556	
OHRCV1	4	28	141	454	623	
OHRCV2	4	20	93	288	401	
OHXMTR	4	23	105	360	488	
PROM	1	14	68	132	214	
8080	1	11	60	145	216	
D/A	1	48	90	224	361	
Timer	1	24	59	142	225	
Power 5	1	0	196	154	351	
Power 9	1	0	85	131	216	
Power 10	1	0	37	115	152	
Mother	1	49	375	2	427	
Drawer	1	0	647	163	810	
I&T*	1	6	157	324	487	
Subtotals		293	2436	3674	6403	(Disc Box)
STAL	1	3	1281	129	1414	
I&T*	1	12	416	142	570	
Totals		553	6801	7246	14601	

*Note: I&T means Integration and Test

Table 9. Life-Cycle Costs (In Thousands)

Configuration	Hardware	Software	Total
1-2	11346	28	11374
3-7	12454	41	12495
8	13318	51	13369
9-10	14601	73	14674
11	13318	55	13373
12	14601	127	14728
13	13361	48	13409
14	14601	73	14674
15	14601	77	14678
16 (Crystal)	14601	150	14751
16 (Cesium)	21635	150	21785
16 (Rubdium)	19229	150	19379
17 (Cesium)	13704	0	13704
17 (Rubdium)	11306	0	11306