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AN NBS PHASE NOISE MEASUREMENT SYSTEM BUILT FOR FREQUENCY DOMAIN MEASUREMENTS ASSOCIATED WITH THE GLOBAL POSITIONING SYSTEM

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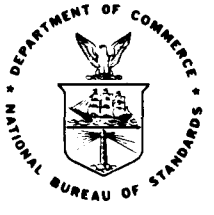

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ABSTRACT

A self-contained system is described which was constructed to perform phase noise measurements for the first phase of the Global Positioning System (GPS). It is capable of evaluating a pair of similar oscillators or a single oscillator and a frequency synthesizer using the phase-lock technique. Three features have been included to simplify the operation of the instrument: internal circuitry automatically detects an out-of-lock condition; an optimized second order phase-lock loop reduces phase error by a factor of 10^5 over a first order loop; selection of operating mode is made by a single front panel switch.

KEY WORDS: Phase-locked loop, phase noise measurement system, spectral density of phase, Global Positioning System.

I. INTRODUCTION

A phase noise measurement system (NBS-PNMS) has been designed and constructed which permits the measurement of the spectral density of phase fluctuations $S_\phi(f)$ of a pair of a pair of (10.23 MHz) oscillators. The basic principles of operation are discussed in Sections I and II. Section III describes the recommended operating procedure. Section IV discusses the interpretation of measurements and Section V gives actual noise floor measurements for relatively low signal levels. The Appendix contains photographs of the instrument and the detailed circuit diagrams.

The block diagram for the measurement system is shown in Fig. 1.

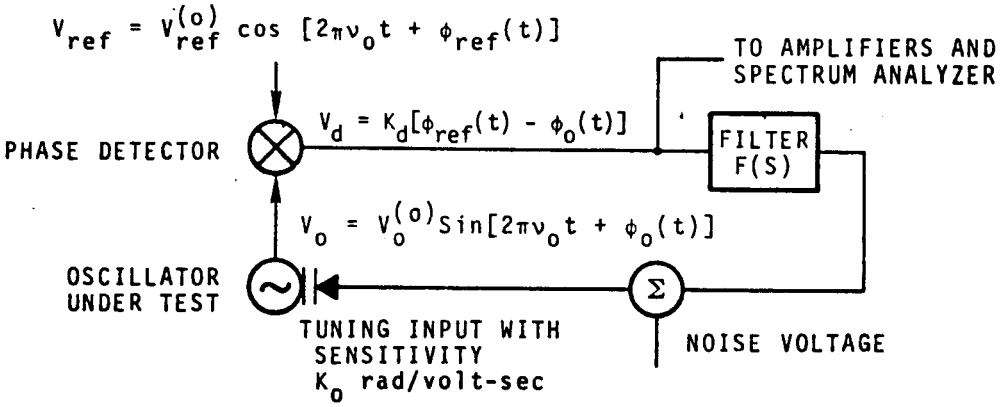

FIGURE 1: Phase-lock loop.

The noise voltage summed into the loop is a schematic way of representing $\phi_n(t)$, the open loop phase noise of the oscillator under test. Phase noise in the reference oscillator is contained in the $\phi_{ref}(t)$ term. This is the general block diagram for any phase-lock loop [1].

The purpose of using a phase-lock loop is simply to guarantee that the two oscillators are on the average in phase quadrature. This condition is indicated by the sine and cosine outputs of the two oscillators. When the oscillators are near quadrature the voltage output of the phase detector is proportional to the difference in phase between the two output signals.

Analysis of the phase-lock loop yields the result [2]

$$\phi_o(s) = \phi_n(s) \left[\frac{1}{1 + G_{eq}(s)} \right] + \phi_{ref}(s) \left[\frac{G_{eq}(s)}{1 + G_{eq}(s)} \right] \tag{1}$$

where $G_{eq}(s)$ is the open-loop transfer function defined by

$$G_{eq}(s) \equiv \frac{K_o K_d F(s)}{s} \tag{2}$$

and $\phi_n(s)$ and $\phi_{ref}(s)$ are the Laplace transforms of the corresponding time varying quantities. We can also calculate the voltage output of the phase detector.

$$V_d(s) = \frac{K_d \left[\phi_{ref}(s) - \phi_n(s) \right]}{1 + G_{eq}(s)} . \tag{3}$$

With the spectrum analyzer we can measure $\langle V_d^2 \rangle$ /Hz and we relate this to the mean square phase fluctuations. We assume that the phase noise of the two oscillators is not correlated.

$$S_{V_d}(\omega) = \frac{K_d^2}{|1 + G_{eq}(j\omega)|^2} \left[S_{\phi_{ref}}(\omega) + S_{\phi_n}(\omega) \right] . \tag{4}$$

Thus if we know the behavior of $G_{eq}(j\omega)$ we can relate the measured spectrum of the voltage at the output of the phase detector to the sum of the spectral densities of the phase noise of the two oscillators.

II. CHOICE OF LOOP FILTER

In the past, for the purpose of measuring phase noise, the loop filter has usually been chosen to be a pure gain. The resulting first order loop has a significant drawback -- the two oscillators are offset from quadrature by a phase shift proportional to the open loop frequency difference between them. In order to maintain system calibration the operator must remove the frequency offset from time to time. This problem can be eliminated by the implementation of a second order loop. Figure 2 illustrates the loop filter used in the NBS-PNMS to achieve the desired frequency response.

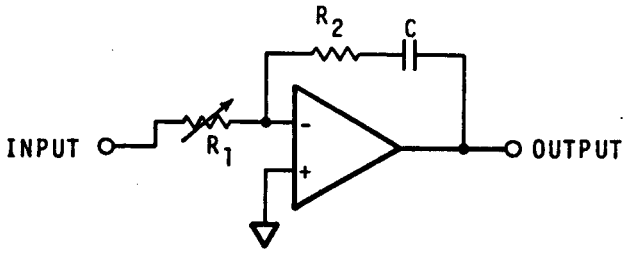

FIGURE 2: Loop filter for second order phase-lock loop.

The transfer function of this filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_2} \tag{5}$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. Figure 3 shows the Bode plot of the frequency response function of this filter.

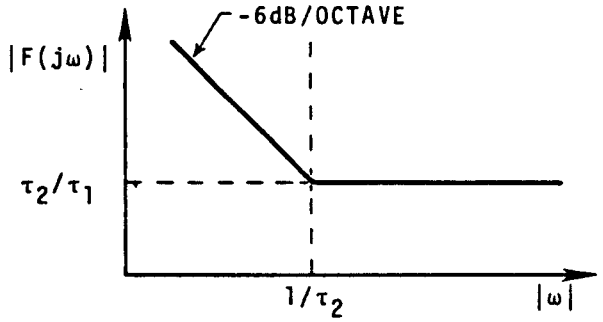

FIGURE 3: Log-log plot of filter transfer function

Substitution of Eq. (5) into Eq. (2) yields the open loop frequency response function.

$$G_{eq}(j\omega) = -\frac{\omega_n^2 + 2j\zeta\omega_n\omega}{\omega^2} \tag{6}$$

where

$$\omega_n \equiv \left(\frac{K_o K_d}{\tau_1}\right)^{1/2} \tag{7}$$

and

$$\zeta \equiv \frac{\tau_2}{2}\omega_n \ . \tag{8}$$

The first requirement which must be satisfied by the loop parameters is that the closed loop is stable. Since the transfer function $G_{eq}(s)$ has no poles or zeroes for $s > o$ a sufficient requirement for the phase-lock loop to be stable is that the slope of the Bode plot of $|G_{eq}(j\omega)|$ be less steep than -12 dB/octave at the point where $|G_{eq}(j\omega)| = 1$ [3]. The Bode plot of $|G_{eq}(j\omega)|$ is shown in Figure 4.

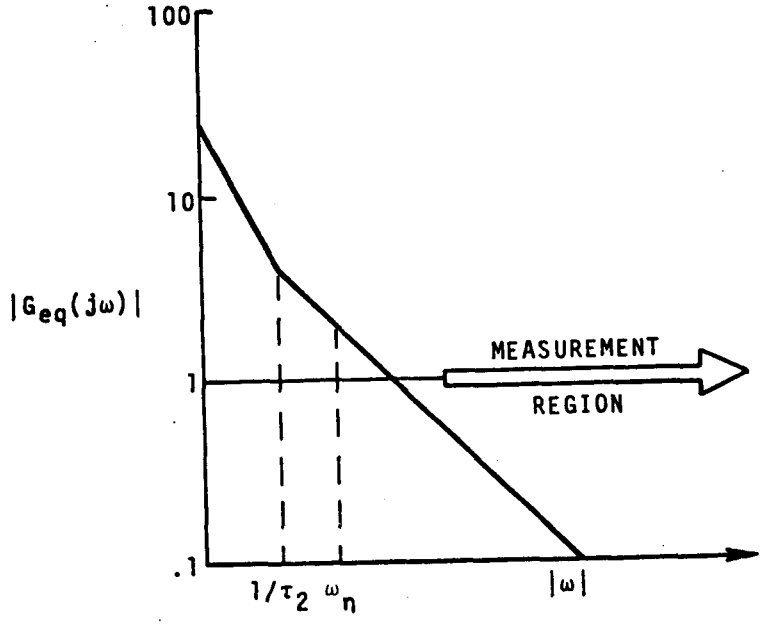

FIGURE 4: Log-log plot of the open-loop transfer function.

It is desirable for the loop to be close to critically damped, i.e., $\zeta = 1$. At critical damping the natural frequency of the loop is related to τ_2 by

$$\omega_{n,\ \zeta = 1} = 2/\tau_2. \tag{9}$$

Under the same conditions the unity gain frequency is

$$\omega_{1,\zeta = 1} = 4.12/\tau_2. \tag{10}$$

The second requirement which must be satisfied by the phase-lock loop relates to the accuracy with which spectral density measurements may be made. Substitution of Eq. (6) into Eq. (4) yields

$$S_{V_d}(\omega) = \frac{K_d^2 \ \omega^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \ \omega^2 \omega_n^2} \left[S_{\phi_{ref}}(\omega) + S_{\phi_n}(\omega) \right]. \tag{11}$$

Since the proportionality factor has a high pass response, it is possible to use an essentially constant calibration to relate $S_{V_d}(\omega)$ and $S(\omega)$. We require that

$$S_{V_d}(\omega) \simeq K_d^2 \left[S_{\phi_{ref}}(\omega) + S_{\phi_n}(\omega) \right]. \tag{12}$$

with no more than 10% error for all Fourier frequencies greater than 2πrad/sec. For the critically damped loop this reduces to a requirement on τ_2:

$$\tau_2 > 1.4 \text{ seconds}.$$

The NBS-PNMS has τ_2 = 12 seconds.

The third requirement on loop performance is that frequency offset between the two oscillators produces negligible phase shift of the oscillators away from quadrature. In the ideal loop the phase error for a frequency error $\Delta\nu$ introduced at time t = o is

$$\phi_{error} = 2\pi\Delta\nu t \ e^{-\omega_n t}. \tag{13}$$

In the actual circuit there is a finite phase error due to the limited loop gain of the amplifier of Fig. 2. In the NBS-PNMS the phase error is reduced by 10^5 compared to its value for a first order loop. Typically the error is less than the residual phase error due to the voltage offset at the mixer output and should be much less than one degree.

III. OPERATION

There are two modes of operation which permit either the comparison of two (equal) oscillators at 10.23 MHz or the comparison of a single 10.23-MHz oscillator with a 5-MHz oscillator and a synthesizer. The operating mode is selected by a single front panel switch.

Equal oscillator mode

Turn the instrument on.

In this mode the total phase noise from two 10.23 MHz oscillators may be measured. The two oscillators are connected to inputs A and B. The input voltage (7 dBm nominal) should be as large as possible but the input current should not exceed 40 mA peak. The beat between the two oscillators may be observed at the amplifier 1 output or, if it is sufficiently slow, on the meter with the meter switch in position AMP 1. The out-of-lock light should be on.

With the Set Up-Lock switch in the Set Up position the varactor input of one oscillator should be connected to the servo-output connector. Before making this connection check to see if the polarity of the dc bias voltage is appropriate for the oscillator to be controlled. If necessary, it may be changed by throwing the SPDT switch mounted on the right side at the front of the interior shield box. The varactor input of the other oscillator should be grounded. Now the time constant switch should be set to minimum and the coarse and fine bias controls adjusted to obtain a beat-period of approximately 10 seconds. Close the Set Up-Lock switch and observe whether the beat disappears and the out-of-lock light goes out. If phase-lock is not achieved with the time constant switch set to minimum, open the loop and readjust the beat period to longer than 10 sec. Then repeat the above procedure. When the loop is locked turn the time constant switch CCW to achieve the desired loop response.

If the required slow beat frequencies are not obtained it may be necessary to (1) feedback to the other oscillator or (2) apply a bias voltage to the oscillator which is not in the phase-lock loop.

Before making any phase noise measurements it is necessary to determine if the time constant of the loop has the proper value, i.e., if the loop is near critically damping. This is done by measuring the step response of the loop which should be an exponential decay with a 1/e time constant of approximately 3 seconds. The step response of the loop may be measured with the following procedure: Connect the output of amplifier #1 to a strip chart recorder or an oscilloscope. With the loop locked and the strip chart recorder running a nominal 10° phase step is introduced by throwing the phase-step switch. The response of the loop is observed on the recorder. It should have the form of a single exponential decay with 3 second time constant and not more than ∿10% overshot.

Synthesizer mode

Operation in this mode is essentially the same as in the equal oscillator mode. Only the differences are described here.

A 10.23-MHz oscillator is connected to input A; a 5-MHz oscillator and a synthesizer are connected to the appropriate inputs (C). The servo output is connected to the varactor input of the 10.23-MHz oscillator. The set up procedure is the same except that the initial 10 second beat period is obtained by adjusting the synthesizer frequency near 11.5 MHz.

IV. PHASE NOISE MEASUREMENT TECHNIQUE

In Section II we established that there is a simple relationship between the spectral density of the voltage fluctuations at the output of the phase detector and the spectral density of the total phase fluctuations in the oscillators under test. We now denote the total phase spectral density by $S_\phi(f)$:

$$S_\phi(f) = S_{\phi_{ref}}(f) + S_{\phi_n}(f). \tag{14}$$

From Eq. (12) we then obtain

$$S_\phi(f) \simeq \frac{S_{V_d}(f)}{K_d^2} \tag{15}$$

where K_d is the sensitivity of the phase detector in volts/rad. There is one measurement amplifier (no. 1) permanently connected to the phase detector and two additional amplifiers which may be connected in series via their front panel jacks. At the output of amplifier #1

$$S_\phi(f) \simeq \frac{S_{V_1}(f)}{K_1^2} \tag{16}$$

where K_1 is the phase sensitivity at the output of amplifier no. 1 and is equal to gain of amp 1 x K_d. If amplfiers 2 and/or 3 are used to make the measurements the additional gain is taken into account in the following manner

$$S_\phi(f) \simeq \frac{S_V(f)}{(K_1 A)^2} \tag{17}$$

Where A is the total gain following amplifier #1.

The spectral density of the output voltage, $S_V(f)$, is measured with a wave analyzer. With such an instrument one measures the rms voltage, V_{rms}, in some known bandwidth. Under the assumption that the spectral density varies slowly within the bandwidth, B, of the wave analyzer it may be estimated to be

$$S_V(f) \simeq V_{rms}^2/B. \tag{18}$$

The final formula for $S_\phi(f)$ is

$$S_\phi(f) = \left(\frac{V_{rms}}{K_1 A}\right)^2 \frac{1}{B}. \tag{19}$$

The measured spectral density of phase combines the phase noise from all the oscillators involved in the measurement. However, sometimes prior knowledge is available which permits further interpretation of the data. In the equal oscillator mode the two oscillators under test often have identical design and construction and are therefore assumed to contribute equally to the measured noise. In this case

$$S_\phi(f, \text{one oscillator}) = \frac{1}{2} S_\phi(f) \tag{20}$$

The phase noise measured using the synthesizer mode is interpreted as the noise of the single oscillator under test. In this case

$$S_\phi(f, \text{one oscillator}) = S_\phi(f)$$

All such interpretations are subject to the restriction that $S_\phi(f)$ exceeds the measured noise of the NBS-PNMS by 6 dB.*

Calibration

Amplifiers 2 and 3 each have a nominal gain of 10 and bandwidth of 40 KHz. The only calibration of the NBS-PNMS which must be performed for each measurement set-up is K_1, the phase sensitivity at the output of amplifier #1. The phase sensitivity is constant to 1 dB up to 10 KHz. The recommended technique for measuring K_1 is summarized below:

With the phase-lock loop open record the beat (output of amplifier #1) between the two oscillators on a strip chart recorder. If necessary change only the bias voltage to obtain a sufficiently short beat period (approximately 10 sec). The distance between adjacent zero crossings on the chart determines π rad and the slope of the line near the zero crossing is K_1 in volts/rad. It is important to use only the region within $\pm \pi/6$ of the zero crossing in order to limit to 5% the error due to the fact that sine $\phi \neq \phi$.

Two other methods may be used to determine K_1 but they have large probability of systematic error and are therefore not recommended for precise measurements. The first of these methods is to measure V_{ptp}, the peak-to-peak amplitude of beat between the two oscillators at the output of amplifier #1 divided by the input phase shift is K_1. Reflections from the phase detector cause this technique to suffer systematic errors.

*In the past the quantity $\mathscr{L}(f)$ has been used to describe the phase noise of an individual device. $\mathscr{L}(f)$ was defined as the ratio of the power per hertz bandwidth in one phase noise sideband offset a frequency f from the carrier to the total signal power. For $\langle\phi^2\rangle \ll 1$ $\mathscr{L}(f) = \frac{1}{2} S_\phi(f, \text{one oscillator})$.

V. INTERNAL NOISE OF NBS-PNMS

Equal oscillator mode

A single oscillator at 10.23 MHz with a power output of approximately 0 dBm was connected to the A and B inputs as shown in Fig. 6.

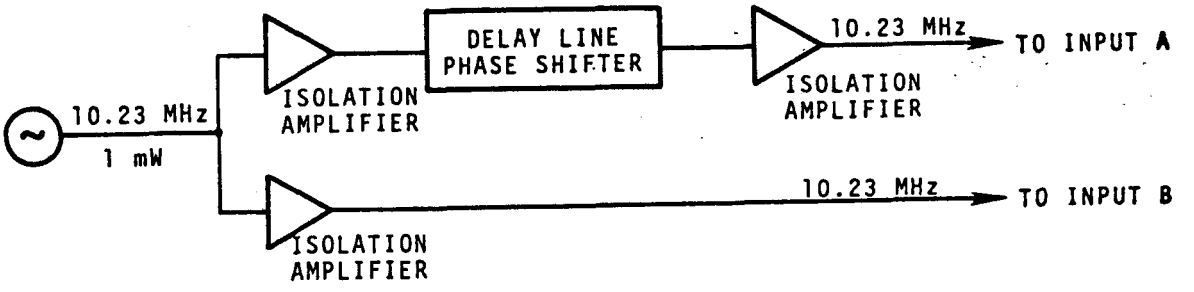

FIGURE 6: Block diagram for equal oscillator mode calibration.

The servo output was connected to the varactor input of the oscillator and the Set Up-Lock switch was in the Set Up position. The phase shifter was then adjusted so that the two inputs were in phase quadrature, i.e., the dc output from the amplifier #1 was nulled. Table I lists the measured phase noise which is the noise floor in this mode.

TABLE I

NBS-PNMS NOISE FLOOR
EQUAL OSCILLATOR MODE (@ 0 dBm drive)

f(Hz)	S (f) dB	$\mathscr{L}$(f) dB
1	-123	-129
2	-126	-132
5	-130	-136
10	-133	-139
20	-135	-141
50	-140	-146
100	-142	-148
200	-145	-151
500	-147	-153
1000	-147	-153
2000	-148	-154
5000	-147	-153

Synthesizer mode

Figure 7 is the block diagram for the measurement of system noise in the synthesizer mode.

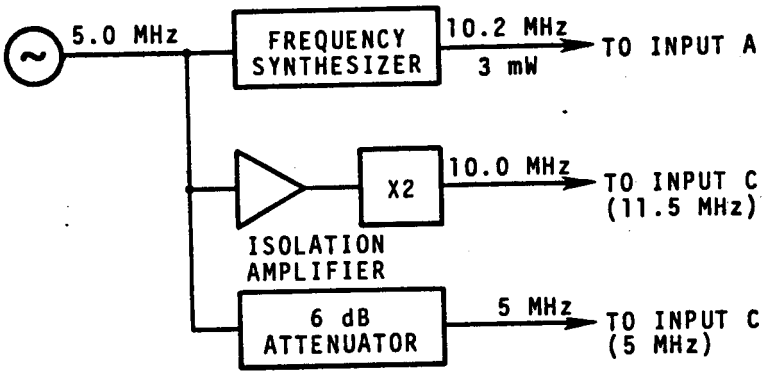

FIGURE 7: Block diagram for synthesizer mode calibration.

The synthesizer at 10.20 MHz is substituted for the 10.23 MHz-oscillator. Internally this signal is mixed with the internally doubled 5-MHz input to produce a 200-KHz beat. The externally generated 10 MHz substitutes for the 11.5-MHz synthesizer. Table II lists the measured phase noise which is the noise floor in this mode.

TABLE II

NBS-PNMS NOISE FLOOR
SYNTHESIZER MODE (@ 3 dBm drive)

f(Hz)	$S_\phi(f)$ dB	$\mathscr{L}(f)$ dB
2	-112	-115
5	-117	-120
10	-120	-123
20	-123	-126
50	-125	-128
100	-126	-129
200	-127	-130
500	-133	-136
1000	-136	-139
2000	-140	-143
5000	-142	-145

SPECIFICATIONS

POWER SOURCE	:	110 Vac	
INPUTS	:	A and B	7 dBm nominal, 40 mA Maximum peak current
		C (5 MHz)	0.7 - 1.25 Vrms
		C (11.5 MHz)	7 dBm nominal, 40 mA Maximum peak current
GAIN/BANDWIDTH:		Thru amplifier #1	$\Delta F_{3dBm} > 20$ KHz
		Thru amplifier #2	$A = 10.0 \pm 0.05$ / $\Delta f_{3\ dB} > 40$ KHz
		Thru amplifier #3	$A = 10.0 \pm 0.05$ / $\Delta f_{3\ dB} > 40$ KHz
BIAS	:	positive or negative, 0 to 10 V.	
PHASE STEP	:	10° nominal	
PHYSICAL SIZE	:	19" relay rack chassis, 5 1/4" high x 17" deep	

REFERENCES

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[2] Cutler, L. S. and Searle, C.L., Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards, Proc. IEEE 54, 136 (1966).

[3] Melsa, James L. and Schultz, Donald G., Linear Control Systems (McGraw Hill, New York, 1969) pp. 208-213.

APPENDIX

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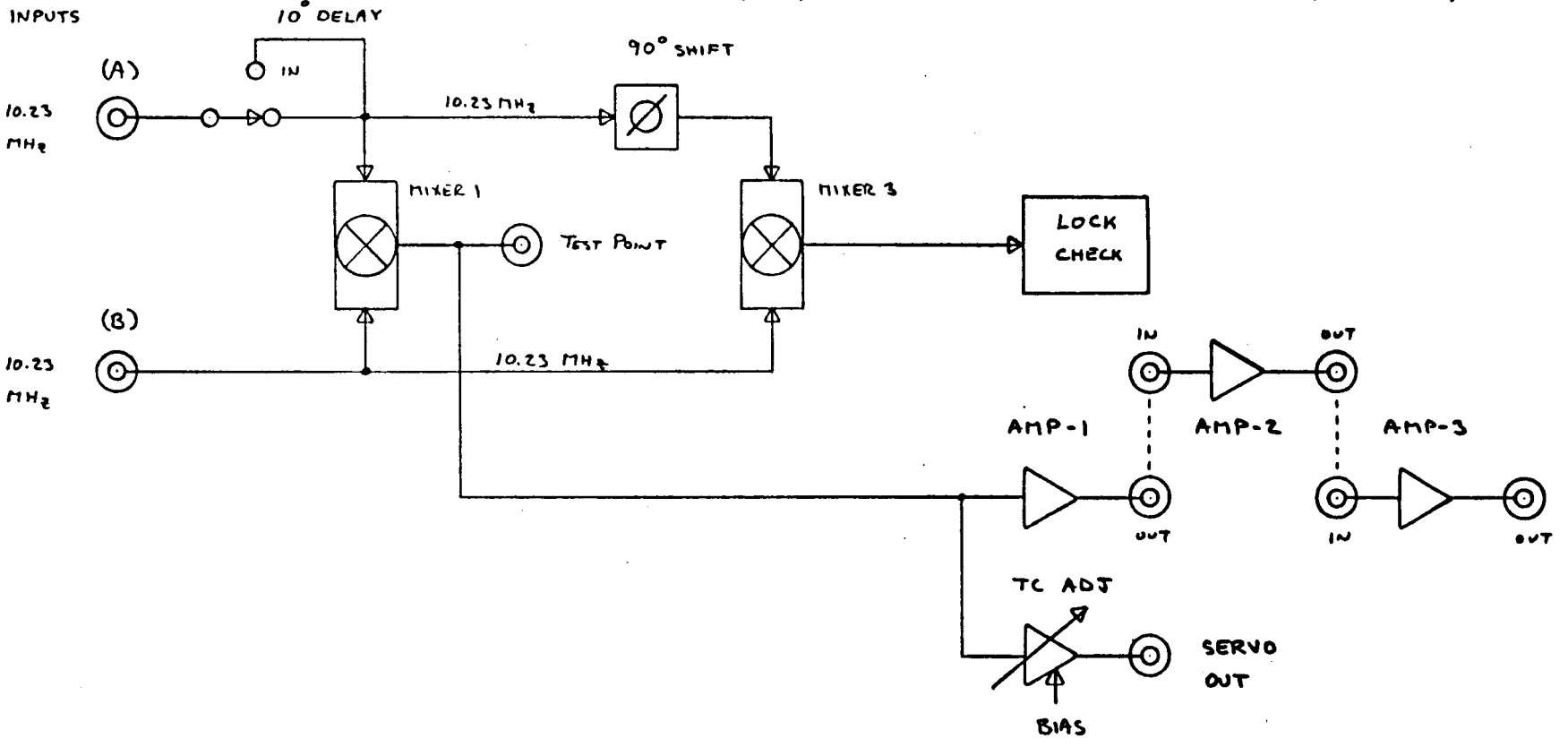

EQUAL OSCILLATOR MODE (A-B)

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		NBS PHASE NOISE SYSTEM SYSTEM DIAGRAM		
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A-1

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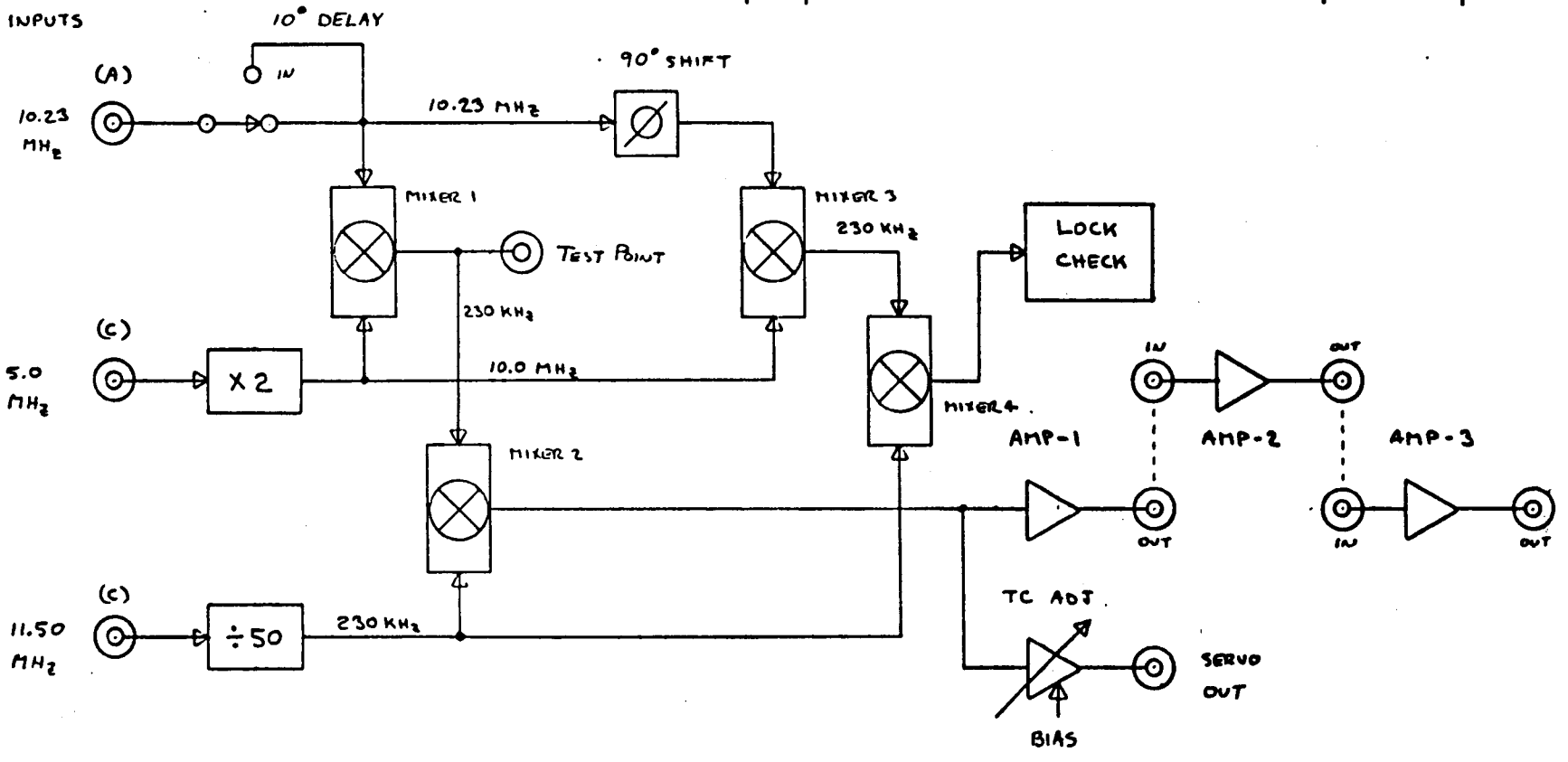

SYNTHESIZER MODE (A-C)

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CHECKED		SCALE	SIZE	DRAWING NO. 75008-B1
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A-2

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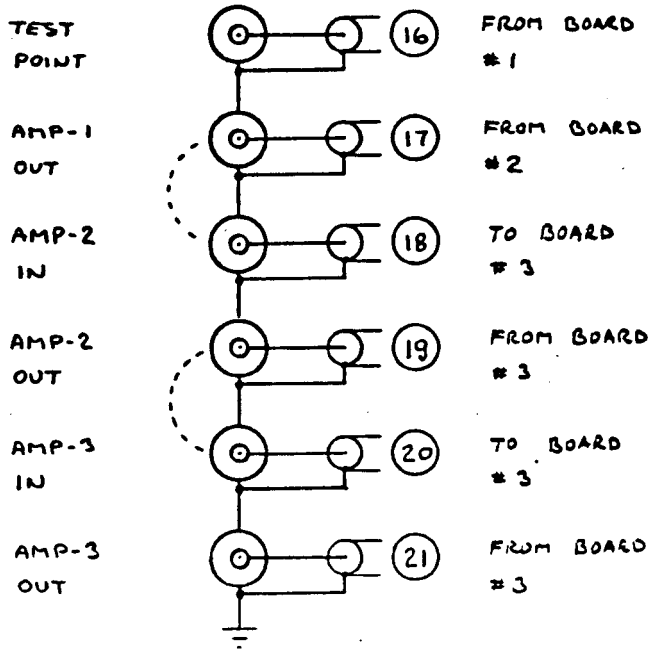
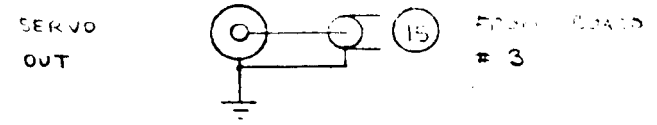
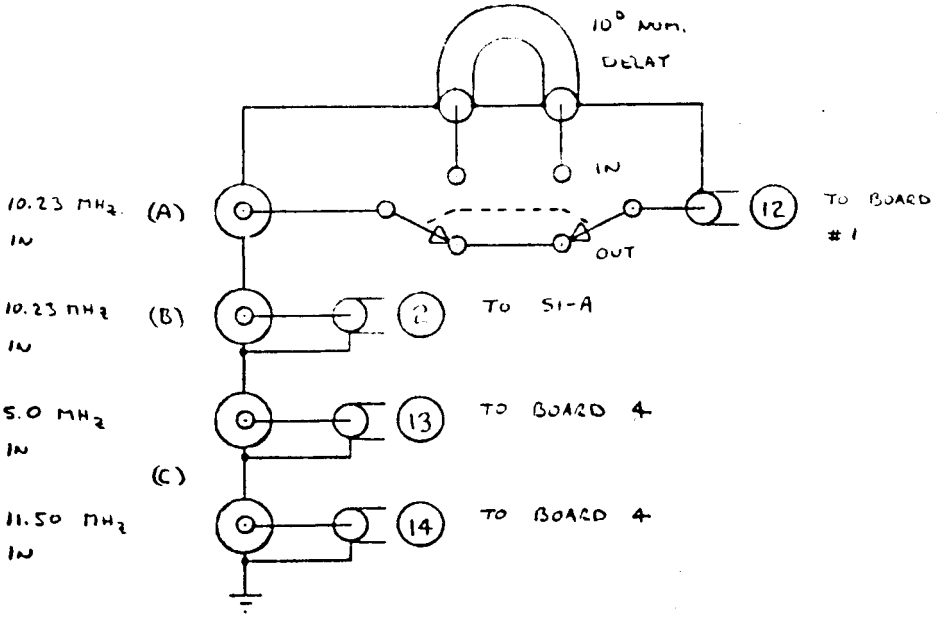
LTR	DESCRIPTION	DATE	APPROVED

FRONT PANEL BNC WIRING







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NBS PHASE NOISE SYSTEM
FRONT PANEL WIRING

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DO NOT SCALE DRAWING		75008 - B2	

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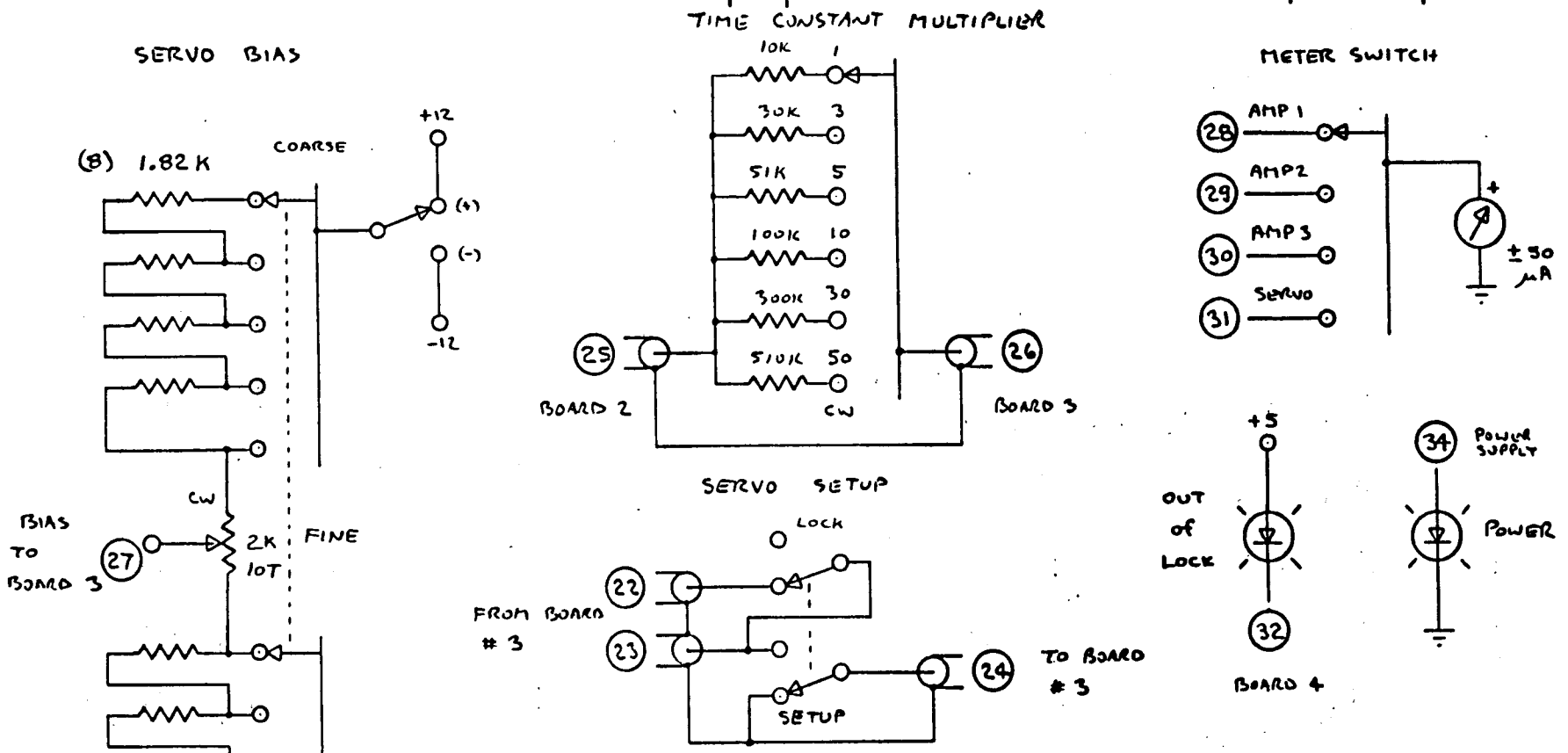

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NBS PHASE NOISE SYSTEM FRONT PANEL WIRING

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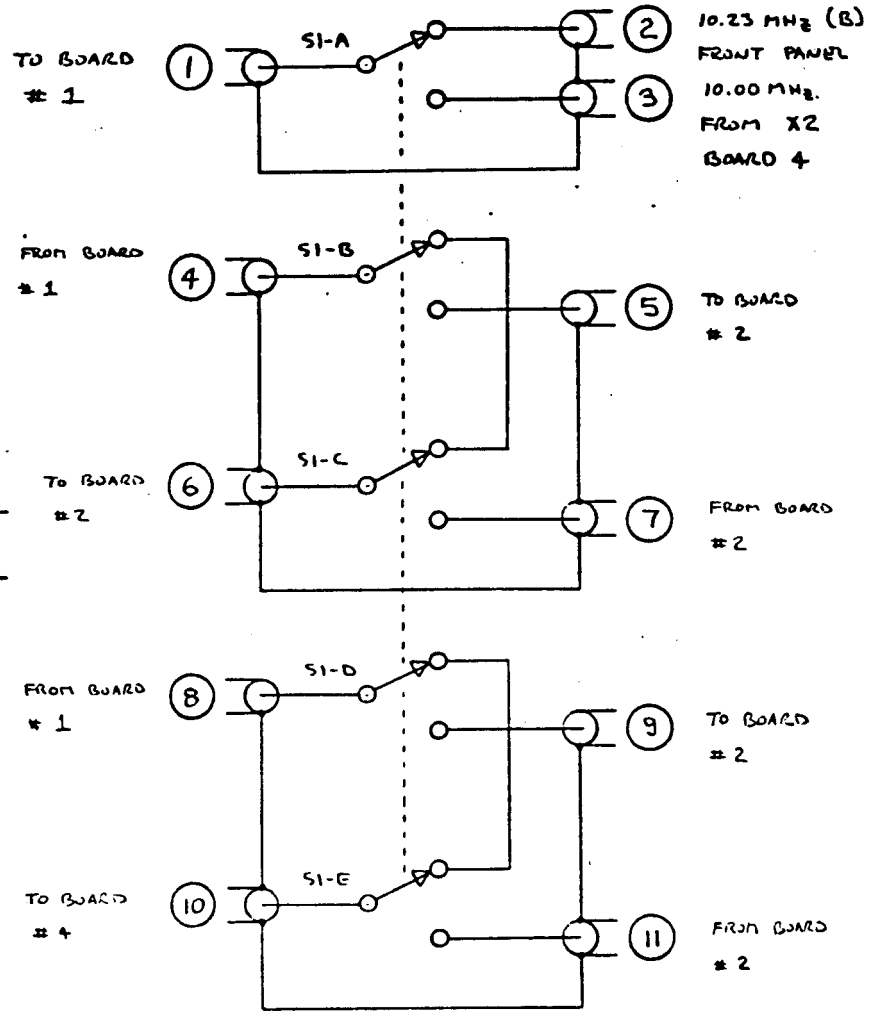
A-4



S1 WIRING

REVISIONS

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TOLERANCES UNLESS OTHERWISE SPECIFIED
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NBS PHASE NOISE SYSTEM
MODE SWITCH WIRING

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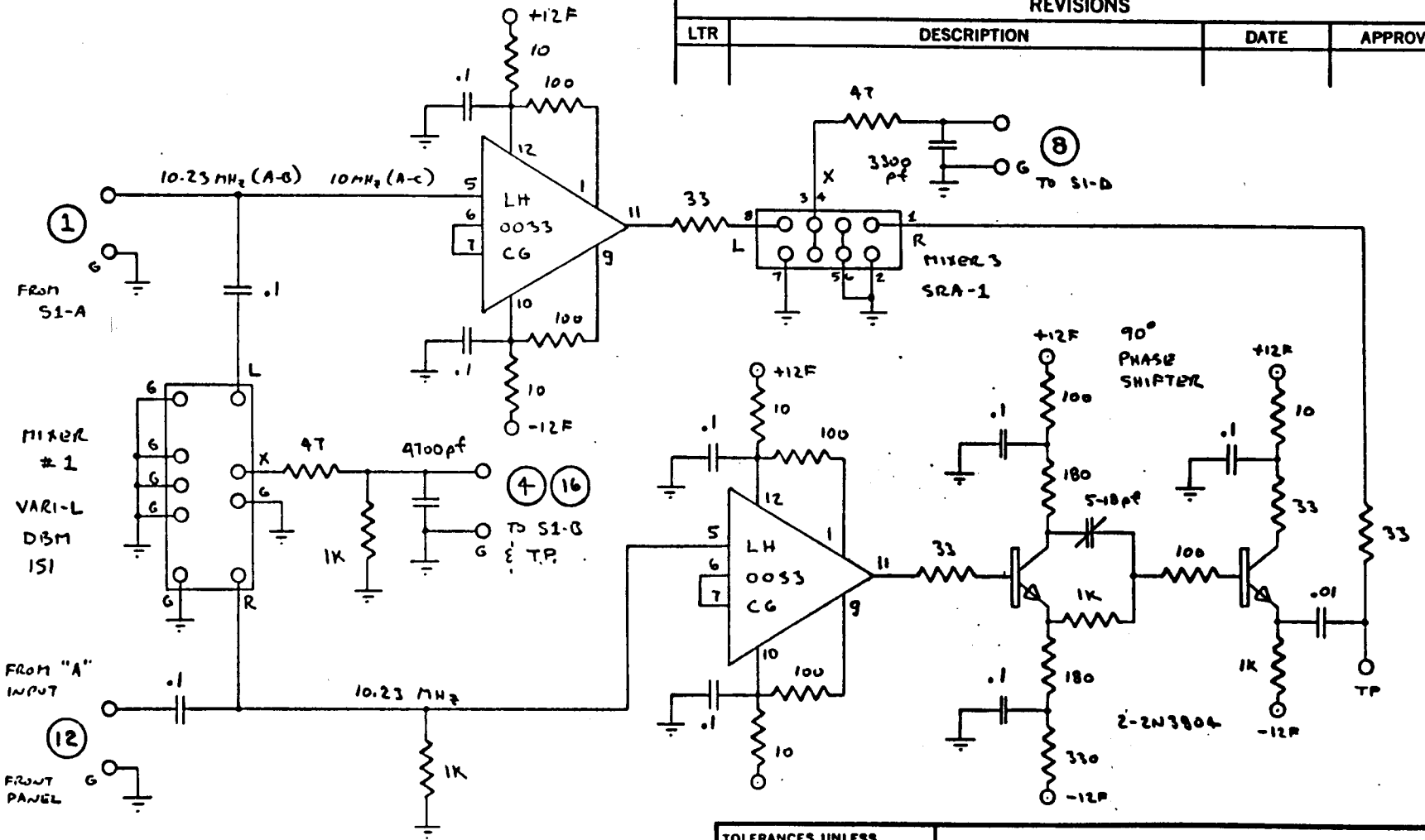

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NBS PHASE NOISE SYSTEM
BOARD 1

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A-6

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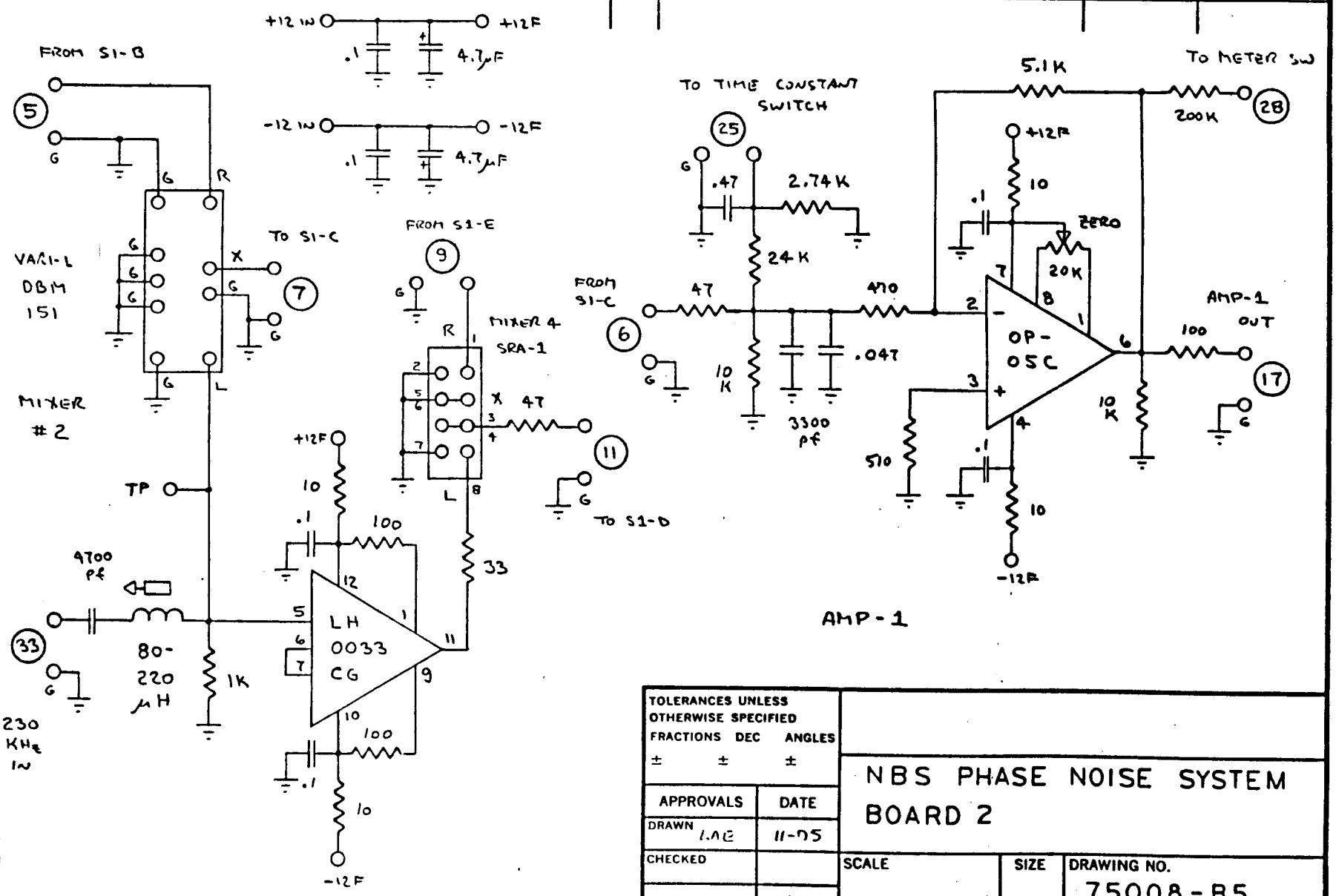

TOLERANCES UNLESS OTHERWISE SPECIFIED		
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NBS PHASE NOISE SYSTEM BOARD 2

SCALE	SIZE	DRAWING NO.
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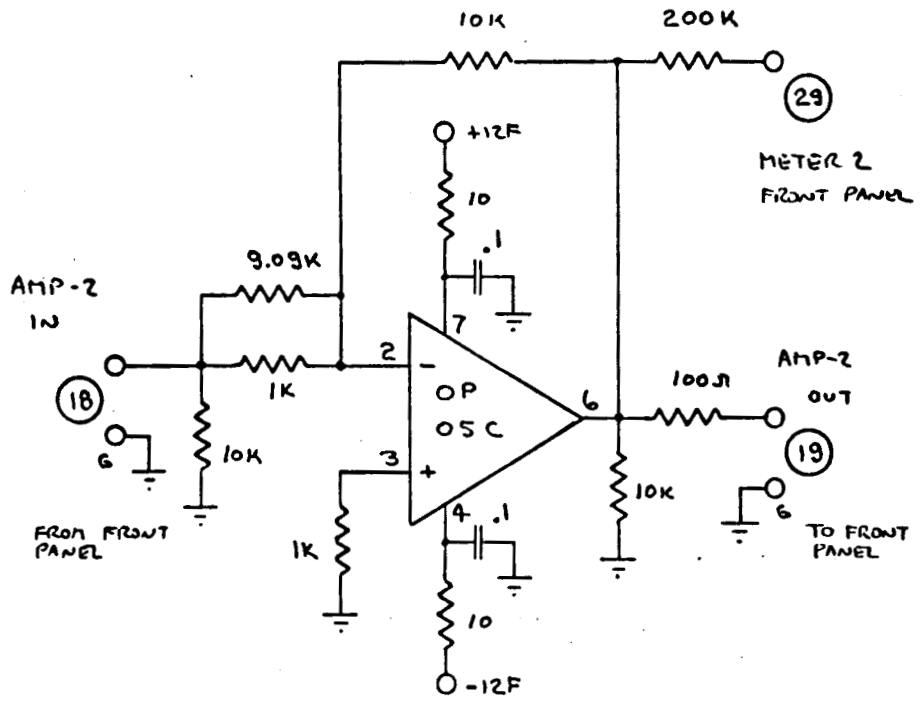
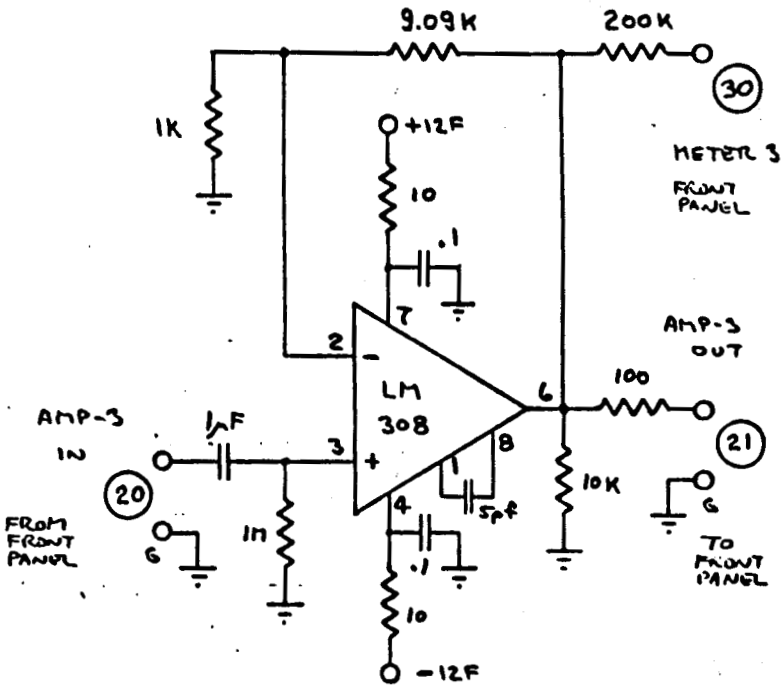
DO NOT SCALE DRAWING — SHEET 1 OF 1

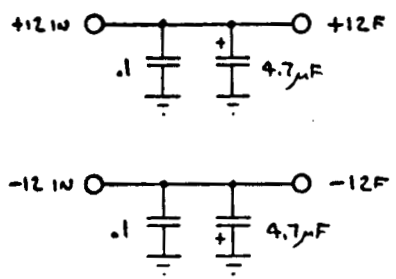
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



AMP-2



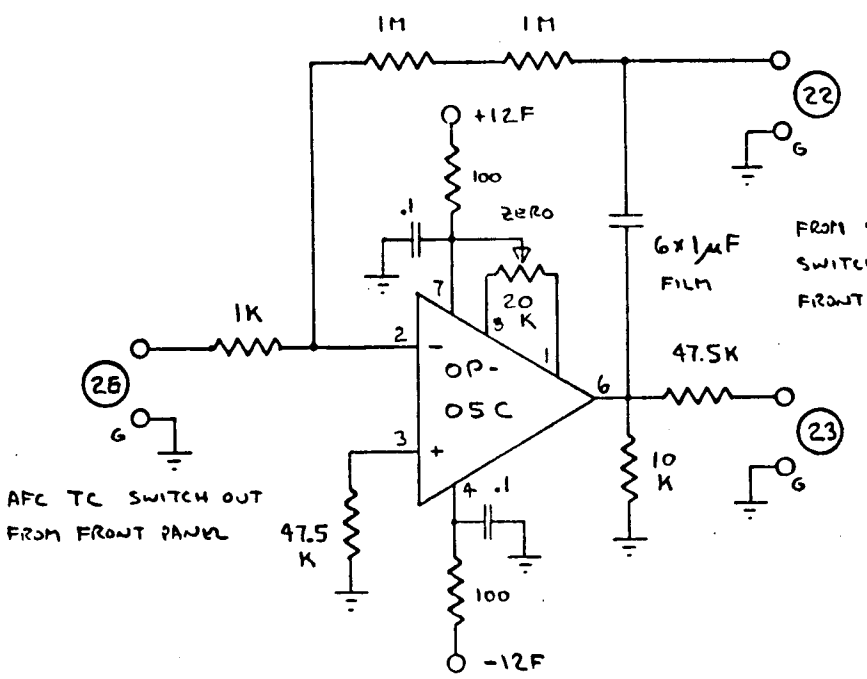
AMP-3



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		NBS PHASE NOISE SYSTEM BOARD 3		
APPROVALS	DATE			
DRAWN LAE	11-95			
CHECKED		SCALE	SIZE	DRAWING NO. 75008 - B6
		DO NOT SCALE DRAWING		SHEET 1 of 2

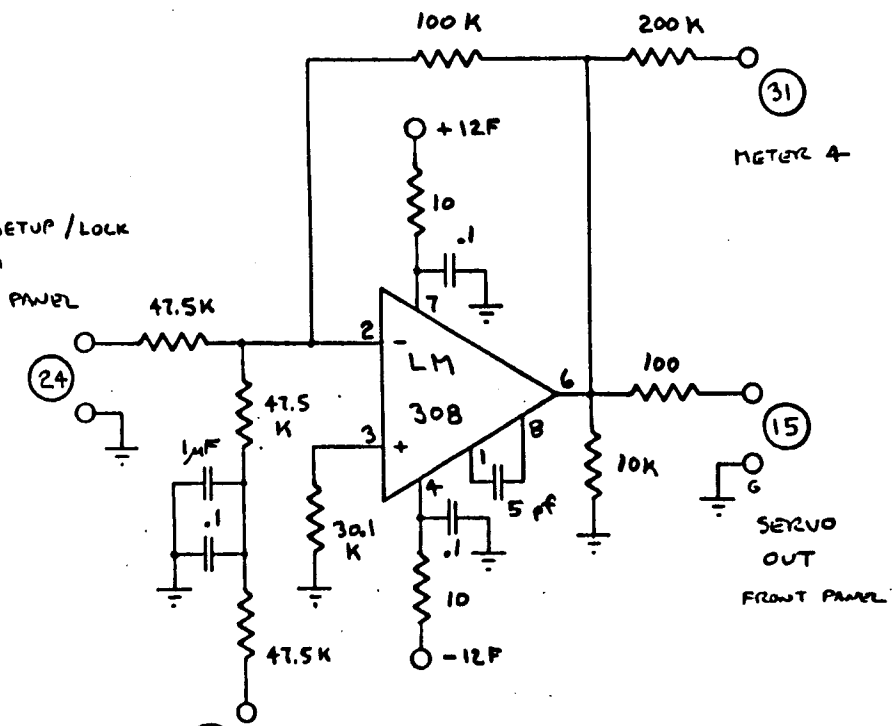
A-8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



AFC INTEGRATOR

FROM SETUP / LOCK SWITCH FRONT PANEL



AFC AMP

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN LAE	11-75
CHECKED	

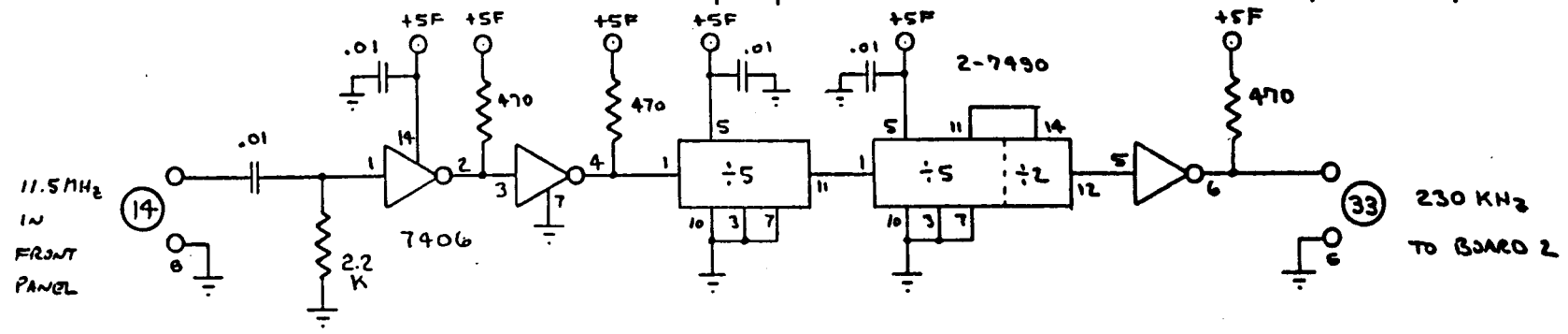
NBS PHASE NOISE SYSTEM
BOARD 3

SCALE	SIZE	DRAWING NO.
		75008-B6
DO NOT SCALE DRAWING		SHEET 2 of 2

A-9

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

÷50



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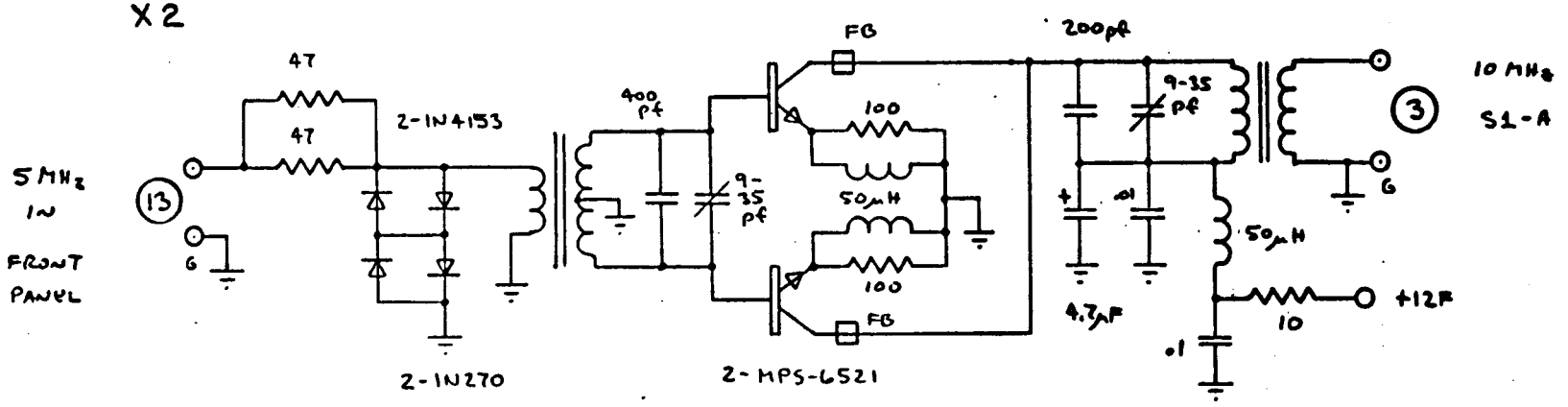
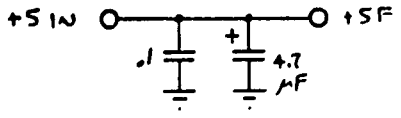


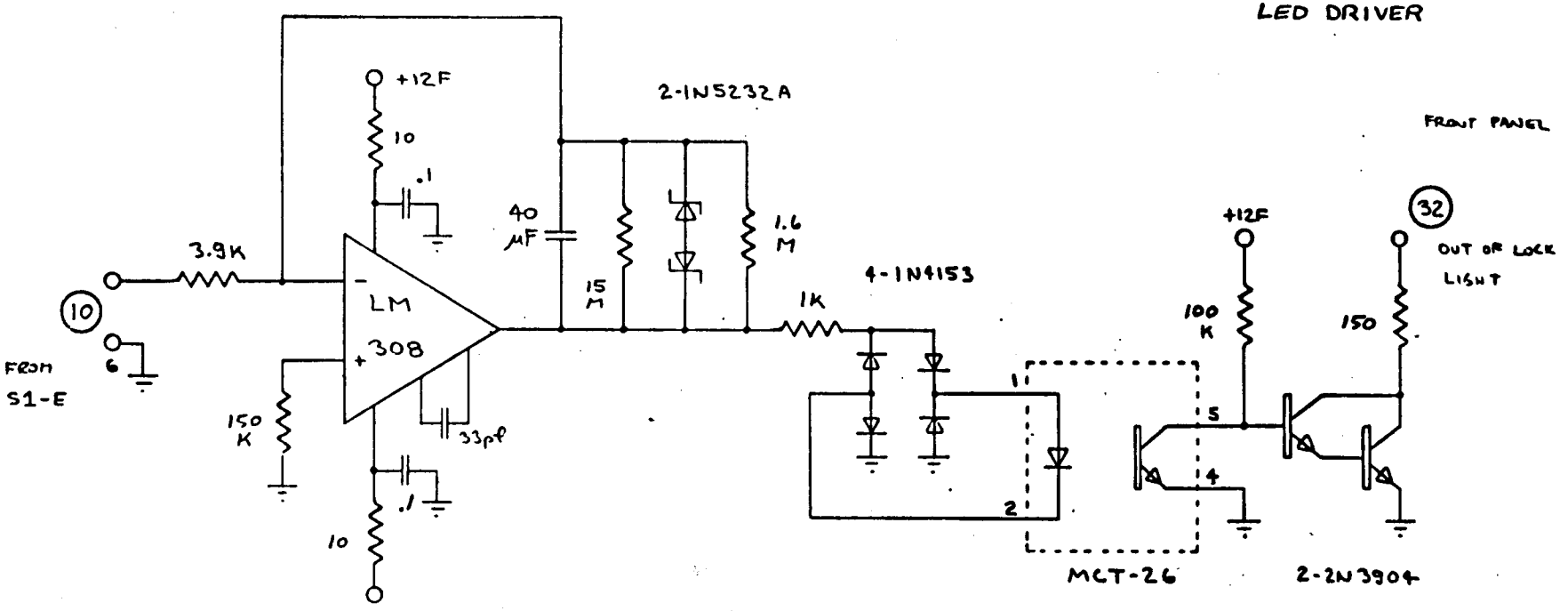


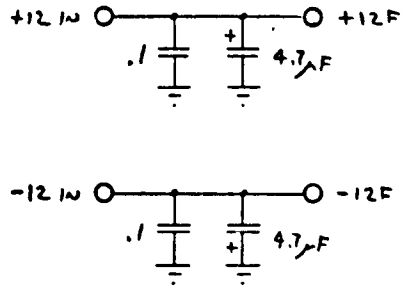
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		NBS PHASE NOISE SYSTEM BOARD 4		
APPROVALS	DATE			
DRAWN LAE	11-75			
CHECKED		SCALE	SIZE	DRAWING NO. 75008-B7
		DO NOT SCALE DRAWING		SHEET 1 of 2

A-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

SERVO LOCK INTEGRATOR

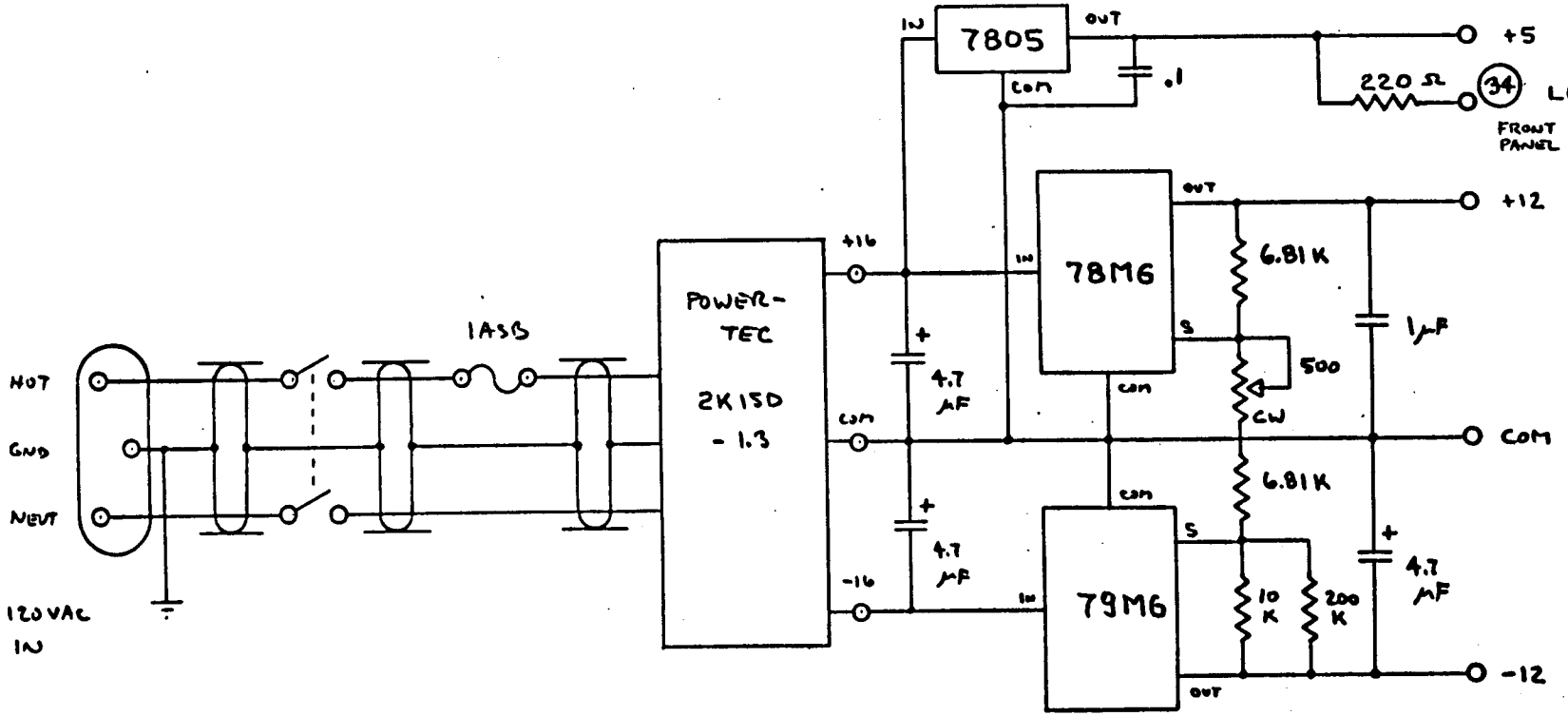




TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		NBS PHASE NOISE SYSTEM BOARD 4		
APPROVALS	DATE			
DRAWN LAE	11-75			
CHECKED		SCALE	SIZE	DRAWING NO. 75008 - B7
		DO NOT SCALE DRAWING		SHEET 2 OF 2

A-11

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



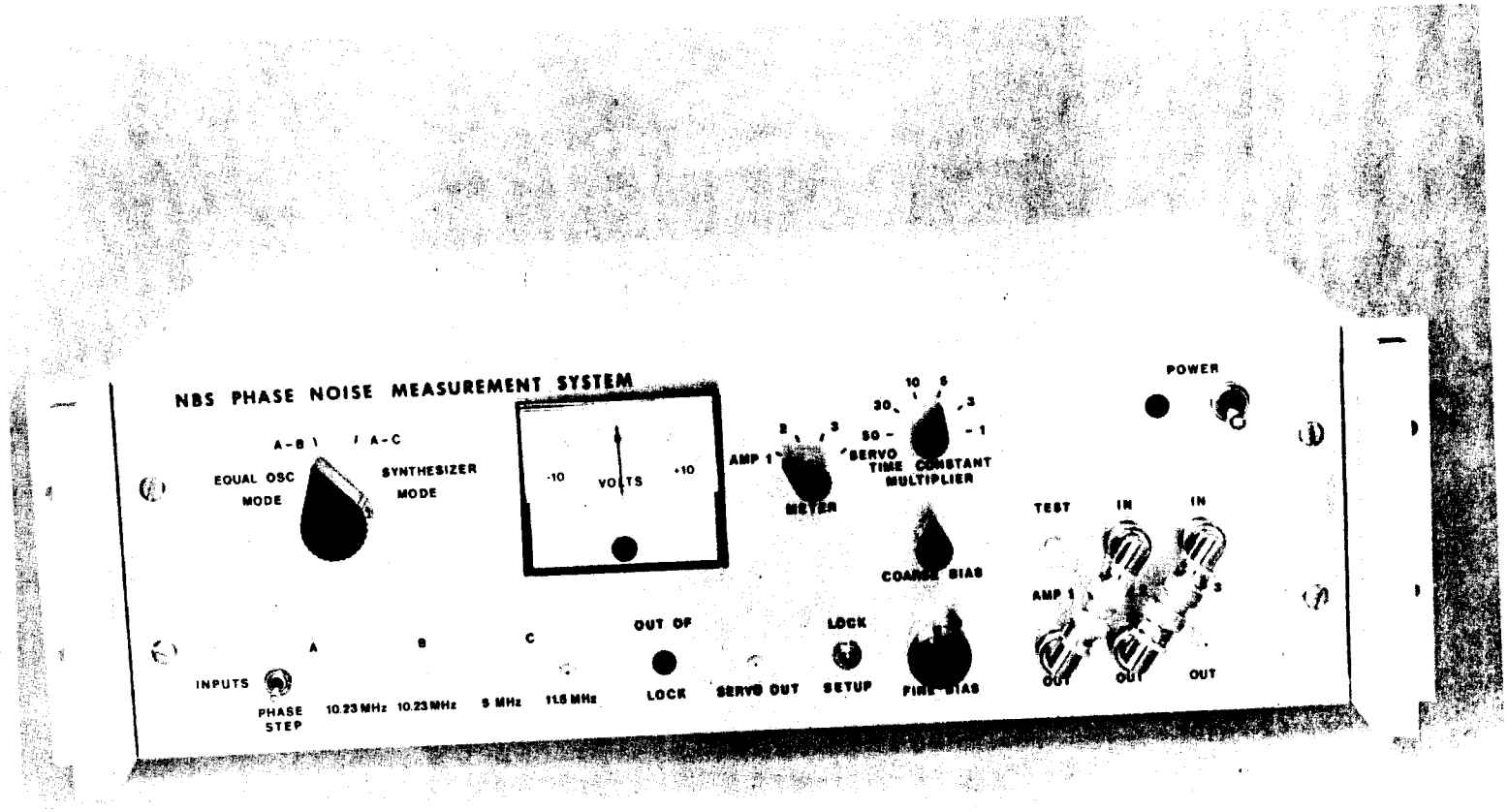
TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN LAE	11-75
CHECKED	

NBS PHASE NOISE SYSTEM POWER SUPPLY

SCALE	SIZE	DRAWING NO.
		75008-B8
DO NOT SCALE DRAWING		SHEET 1 of 1

A-12


NBS PHASE NOISE MEASUREMENT SYSTEM
A-B
A-C
EQUAL OSC MODE
SYNTHESIZER MODE
-10
VOLTS
+10
AMP 1
METER
10
5
30
3
50
1
SERVO TIME CONSTANT MULTIPLIER
POWER
COARSE BIAS
TEST
IN
IN
AMP 1
OUT
OUT
OUT
A
B
C
OUT OF LOCK
LOCK
SETUP
INPUTS
PHASE STEP
10.23 MHz
10.23 MHz
5 MHz
11.5 MHz
LOCK
SERVO OUT
SETUP
FINE BIAS