NBS TECHNICAL NOTE 1003

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Automatic Path Delay Corrections to GOES Satellite Time Broadcasts

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Automatic Path Delay Corrections to GOES Satellite Time Broadcasts

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AUTOMATIC PATH DELAY CORRECTIONS TO GOES SATELLITE TIME BROADCASTS

J. V. Cateora, D. W. Hanson, and D. D. Davis

In support of the environmental data collection by the National Oceanic and Atmospheric Administration's (NOAA's) Geostationary Operational Environmental Satellites (GOES), a time code has been incorporated into an interrogation message from these satellites by the National Bureau of Standards (NBS). This message is directed to data-collection platforms engaged in seismic, tsunami, hydromet and other related monitoring activities. The NBS has developed this time-code system to serve environmental data users who require only a few tenths of a second accuracy as well as those who need a more accurate time reference.

The time code is available continuously from two geostationary satellites and provides a coverage of the Atlantic and Pacific Ocean Basins as well as the North and South American Continents. The time code includes the necessary information to compensate for free-space propagation delays between the master clock located at Wallops Island, Virginia, and the user. Preliminary results indicate a timing resolution of 10 μs.

The time-code system is supported by atomic clocks maintained at Wallops Island, Virginia, the point of origin for all signals to be sent through the satellites. A data-logging system monitors three television networks and Loran-C to provide a comparison link between the Wallops Island clocks and reference standards at the NBS.

A microprocessor "smart" clock has been developed for the user that automatically corrects for path and equipment delays and places its recovered time in synchronism with Coordinated Universal Time (UTC) generated by NBS. This clock, associated recovery equipment, and measured results are discussed in detail in this report.

Key Words: Broadcast; delay correction; microprocessor; satellite; scientific calculations; time of year.

1. INTRODUCTION

A time code has been added by the National Bureau of Standards (NBS) into a communications channel between the National Oceanic and Atmospheric Administration's (NOAA's) Geostationary Operational Environmental Satellites (GOES) and remote environmental data-gathering platforms. The time code is continuously available throughout the entire Western Hemisphere, offering easy accessibility and moderately high accuracy at low cost. The time code contains Coordinated Universal Time (UTC) information and Universal Time (UT1) corrections. In addition to the time code, the satellite's position is included for free-space propagation time corrections. These position data are presently in the form of the satellite's longitude, latitude, and range from the earth's center. The UTC and UT1 information is a permanent feature of these satellites and will remain fixed in format. The satellite position information may undergo changes in form to improve its performance.

2. GOES SYSTEM DESCRIPTION

There are three GOES satellites in orbit, two in operational status and the third serving as an in-orbit spare. The two operational satellites are located at 135°W and 75°W with the spare at 105°W longitude. The earth coverages are shown in figure 1.

The mission for the GOES satellites includes (1) continuous photography of the earth's surface, (2) collection of data on the space environmental Sun/Earth interaction, and (3) collection of remote-sensor data including flood, rain, snow, tsunami, earthquake, and air/water pollution monitoring. It is in this third function that a need for a time code was realized since in many cases, the data are of greater value if labeled with the date as they are collected.

Some of these remote sensors are equipped with both a receiver and transmitter. Upon command from the satellite, these sensors, called data-collection platforms (DCP's), are activated to transmit stored data to the satellite. The satellite relays these data to the NOAA Command and Data Acquisition (CDA) station at Wallops Island, VA, for processing and dissemination to users. The communications channel used to activate this response is called the interrogation channel. This channel is continuously relaying interrogation messages through the satellites. Its format is shown in figure 2.

The interrogation message is exactly one-half second in length or 50 bits, the data rate being 100 b/s. The interrogation message is binary and phase modulates a carrier ± 60 degrees after being Manchester-encoded; i.e., data and data clock are modulo-2 added before modulating the carrier. An interrogation message consists of the first four bits representing a BCD word of the time code beginning on the one-half second followed by a maximum length sequence (MLS) 15 bits in length for message synchronization and ending with 31 bits as an address for a particular DCP. When a DCP receives and recognizes its unique address, it transmits its data to the satellite. Sixty interrogation messages are required to send the 60 BCD time-code words constituting a time-code frame. The time-code frame begins on the one-half minute and requires 30 seconds to complete.

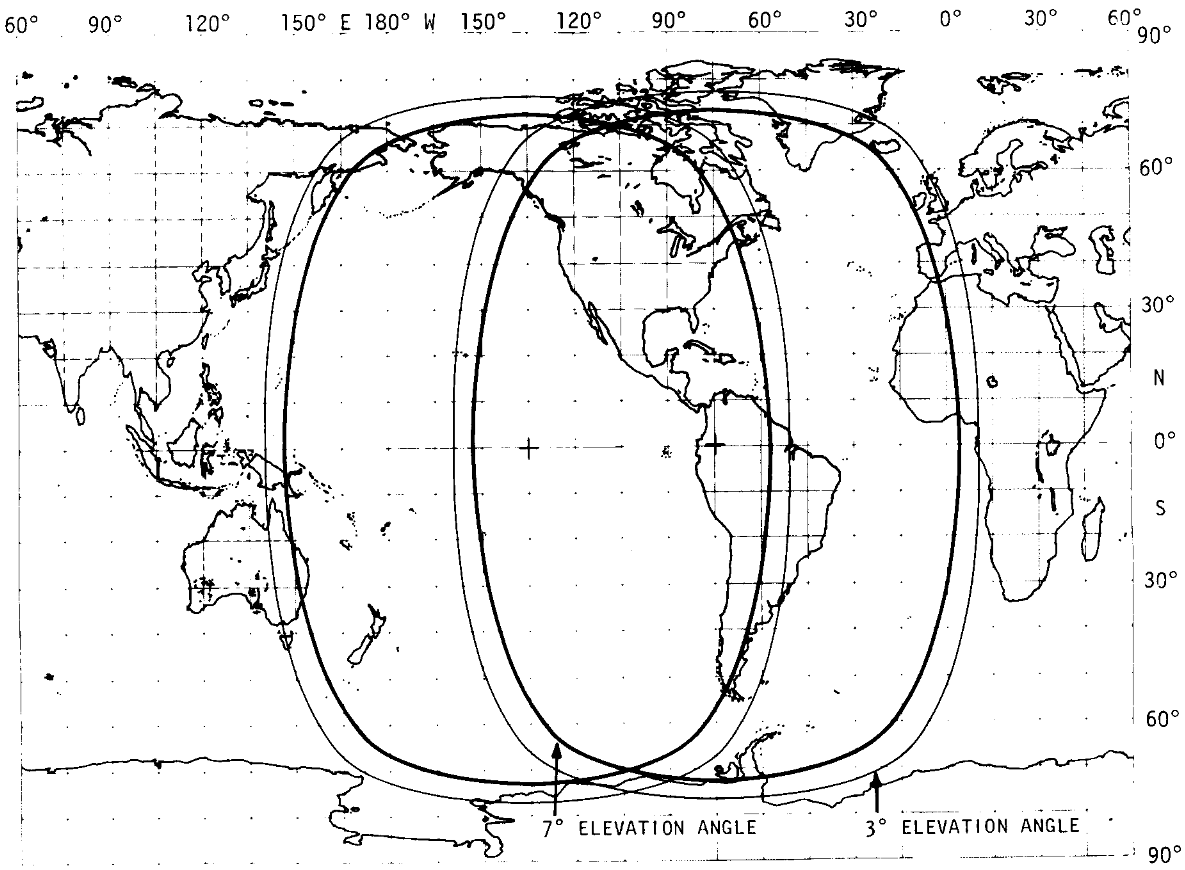

FIGURE 1. GOES COVERAGE

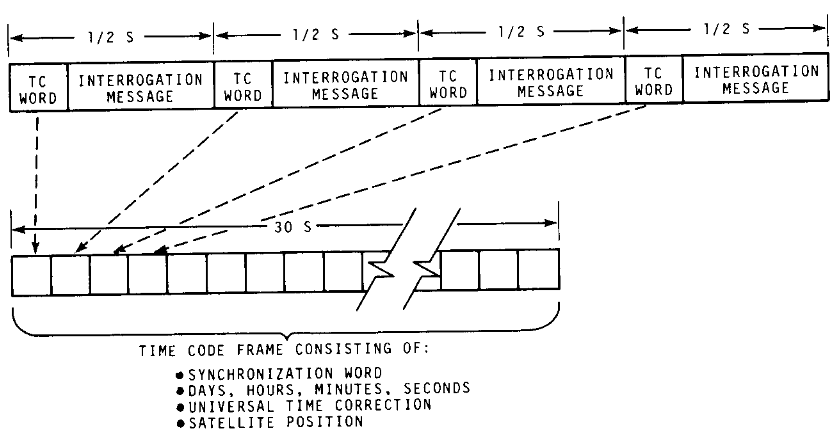

FIGURE 2. INTERROGATION MESSAGE FORMAT

3. TIME CODE SYSTEM

The time code is generated and integrated into the interrogation message at the CDA for transmission to the GOES satellites. The time-code generation system, shown in figure 3, is completely redundant and fully supported by an uninterruptable power supply. There is a communication interface between the equipment and NBS/Boulder using a telephone line. Over the telephone line, satellite position information is sent to the CDA and stored in memory for eventual incorporation with the time code and interrogation message. Data are also retrieved from the CDA via the telephone line to Boulder. These data include the frequency of the atomic oscillators and the time of the clocks relative to UTC as compared to TV transmissions from Norfolk, VA, and to the Loran-C transmissions from Cape Fear, North Carolina. These data are stored for retrieval in a data logger similar to that described in reference [1]. The data logger also measures and stores the time of arrival of the signals from both the Western and Eastern GOES satellites as received at the CDA. Besides the time and frequency monitoring functions, the data logger provides the information necessary for NBS staff at Boulder to remotely determine if and where malfunctions exist and how to correct for them by switching in redundant system components.

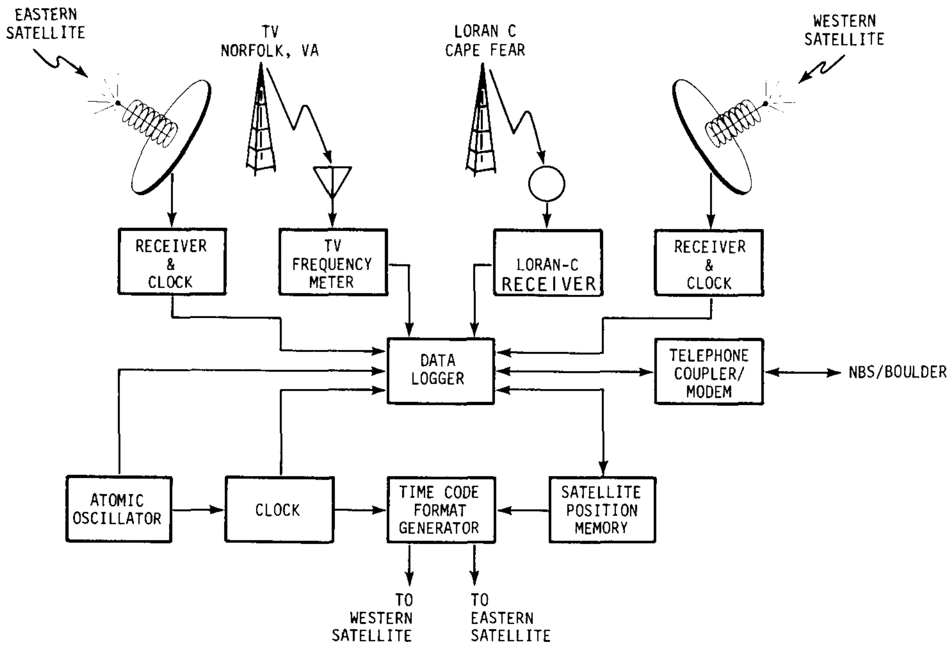

FIGURE 3. TIME CODE GENERATION EQUIPMENT AT THE CDA WALLOPS ISLAND, VIRGINIA

The interrogation message rate, 100 b/s, is generated by the atomic oscillators in the time-code system. The time-code frame repeats every 30 seconds and begins on the one-half minute as shown in figure 4. The time-code frame contains a synchronization word, a time-of-year word (UTC), the UT1 correction, and the satellite's position in terms of its longitude, latitude, and radius. The position information is presently updated only on the half hour.

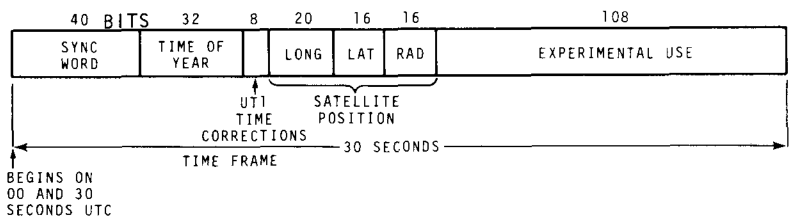

FIGURE 4. TIME CODE FORMAT

The satellite position information is generated at Boulder using a CDC 6600 computer and orbital elements furnished by NOAA's National Environmental Satellite Service (NESS). NESS generates these orbital elements weekly from data obtained from their trilateration range and range rate (R&RR) tracking network. This network is illustrated in figure 5. The tracking data are obtained by measuring the R&RR to the Western satellite from the CDA, and sites in the states of Washington and Hawaii. The Eastern satellite is observed from the CDA, Santiago, Chile, and Ascension Island in the South Atlantic. The sites used in the R&RR network other than the CDA are known as turn-around ranging stations (TARS).

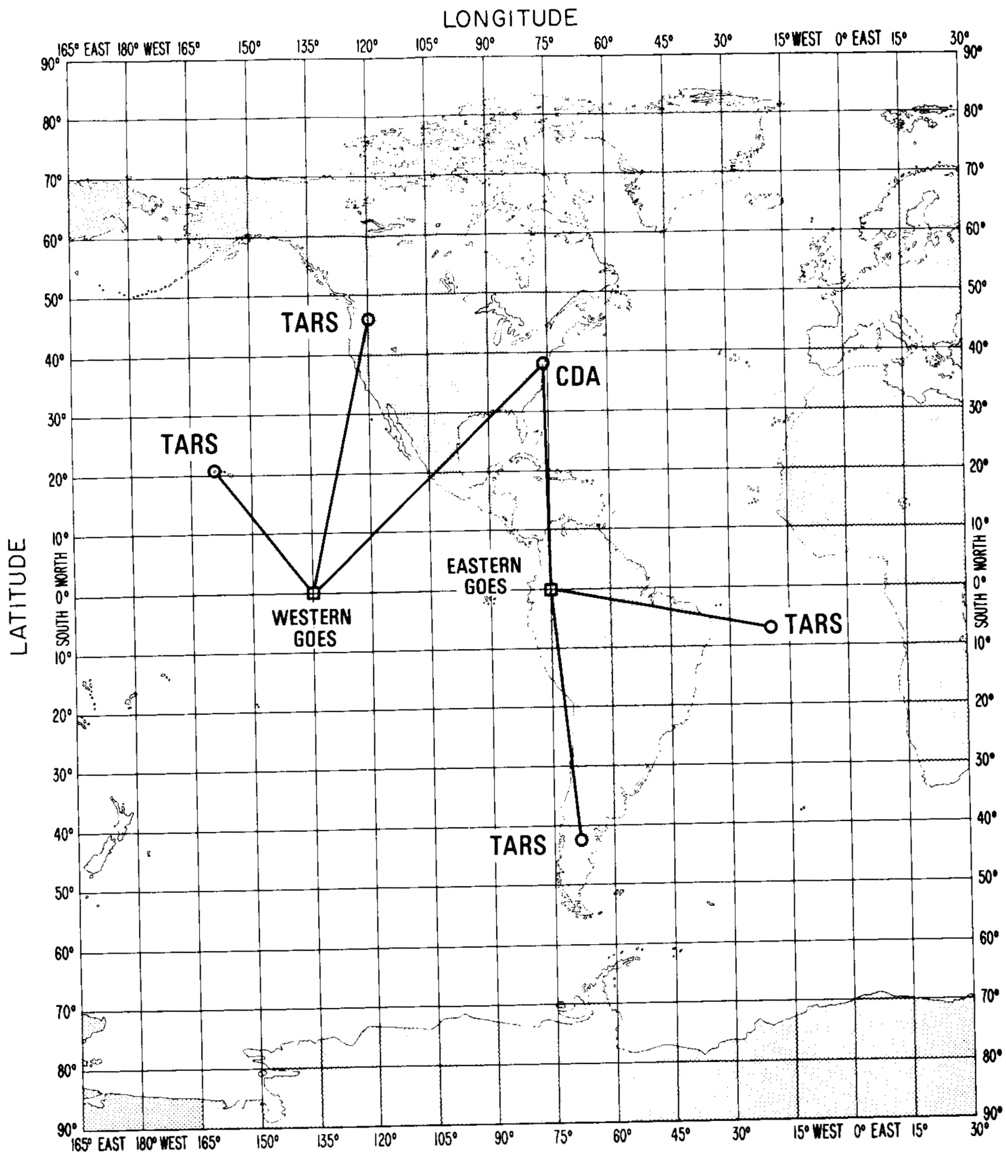

FIGURE 5. TRACKING NETWORK FOR THE GOES SATELLITES

4. RECEPTION

The interrogation channel signals are briefly characterized in figure 6. Typical antennas include simple low-gain helixes or yagis. A block diagram of the receiver is shown in figure 7. It is shown in figure 8 as three modules: an RF/IF module, an local oscillator injection module, and a demodulator module. This receiver is a coherent, synchronous digital receiver utilizing a phase-lock loop for demodulation and local oscillator generation and a bit synchronizer for detection purposes.

	WESTERN SATELLITE	EASTERN SATELLITE
FREQUENCY	468.8250 MHz	468.8375 MHz
POLARIZATION	RHCP	RHCP
MODULATION	CPSK (± 60°)	CPSK (± 60°)
DATA RATE	100 BPS	100 BPS
SATELLITE LOCATION	135° W	75° W
SIGNAL STRENGTH (OUTPUT FROM ISOTROPIC ANTENNA)	-139 dBm	-139 dBm
CODING	MANCHESTER	MANCHESTER
BANDWIDTH	400 Hz	400 Hz

FIGURE 6. INTERROGATION CHANNEL SIGNAL CHARACTERISTICS

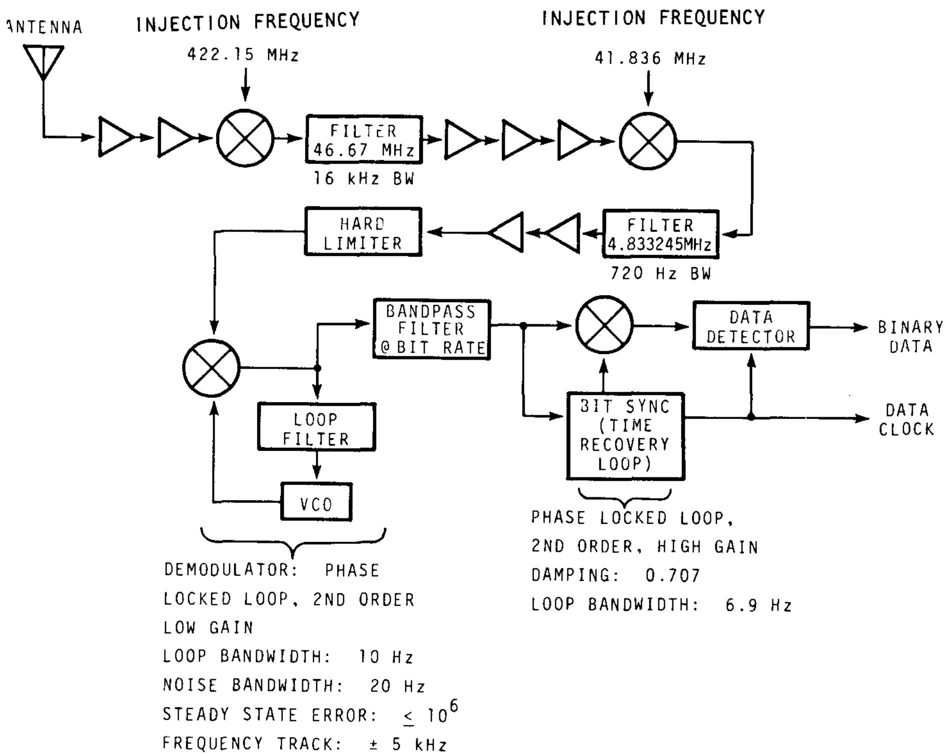

FIGURE 7. INTERROGATION CHANNEL RECEIVER BLOCK DIAGRAM

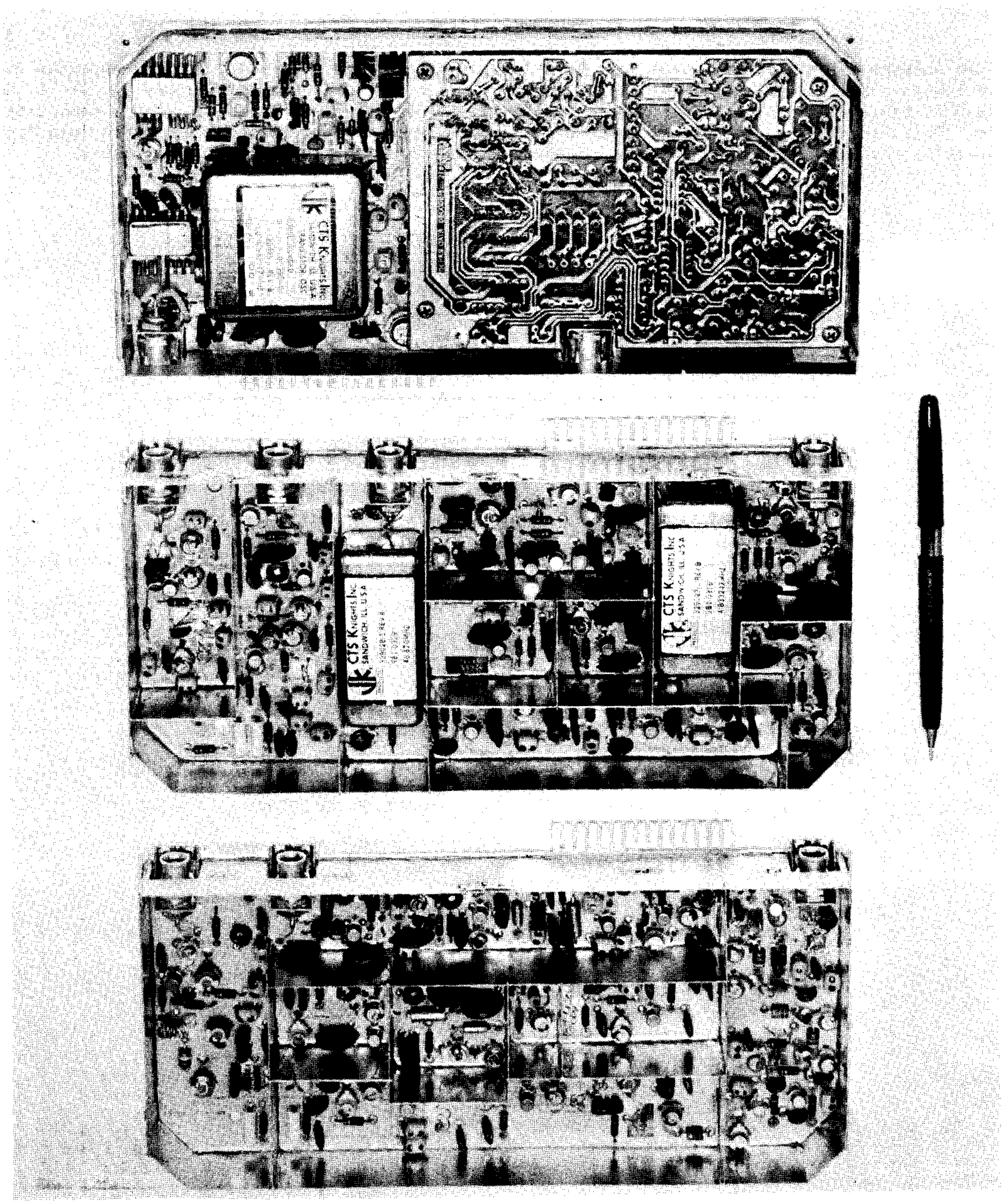

FIGURE 8. INTERROGATION CHANNEL RECEIVER

The outputs of the receiver data, and data clock are the inputs to a decoder clock (see reference [2] for a complete description of this clock). The decoder clock shown in figure 9 uses a four-bit microprocessor to demultiplex the data, extract the proper four bits of the time code every one-half second, and reconstruct the time-code frame. Once decoded, this time is loaded into Random Access Memory (RAM) and updated by incrementing the RAM clock in 10-ms steps by counting the data clock, a 100-Hz squarewave.

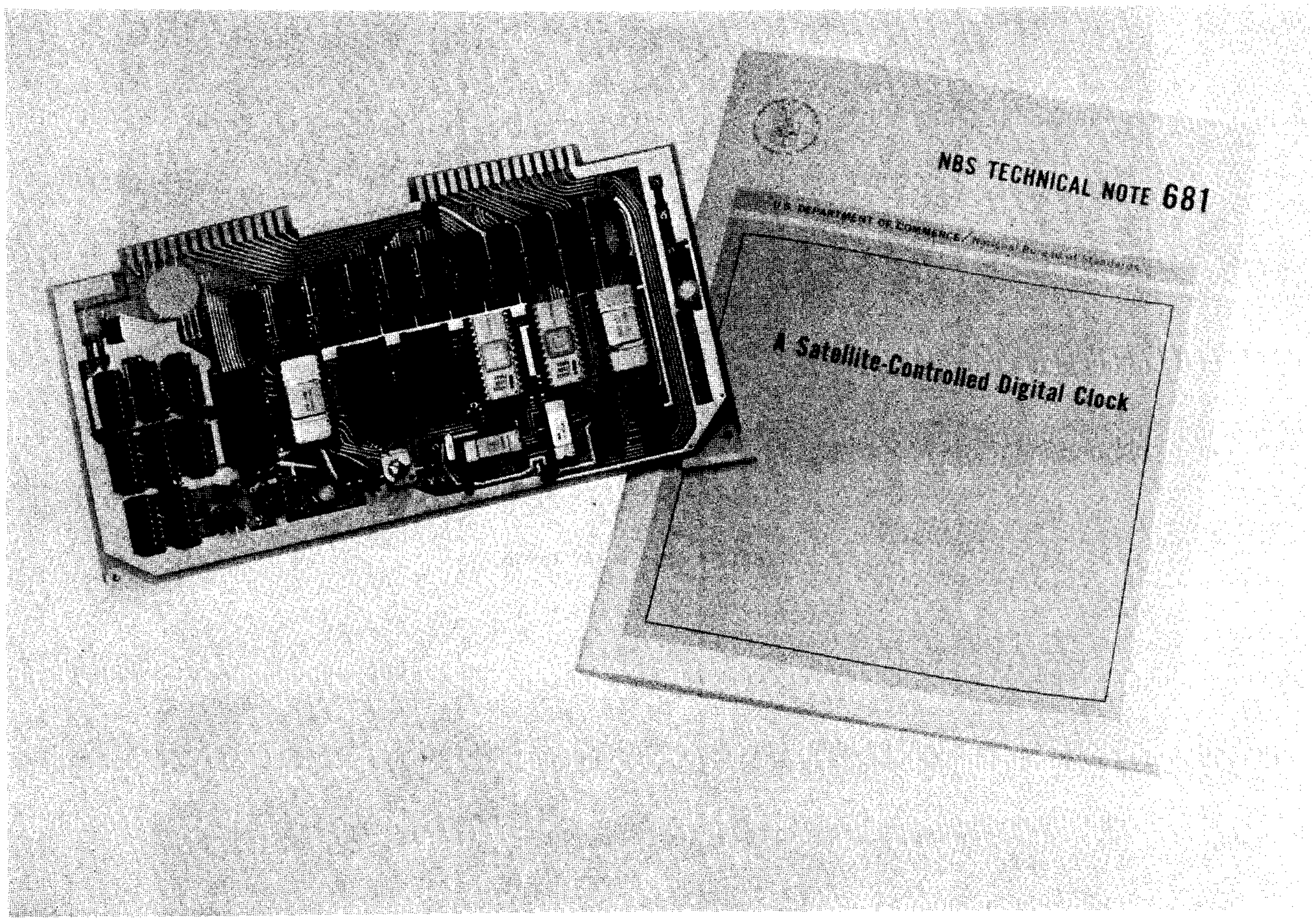

FIGURE 9. DECODER CLOCK

5. DELAY COMPUTATION

A prototype of a "smart" clock is shown in figure 10. The delay calculator is shown in figure 11. This is essentially an addition of a second microprocessor to the decoder clock for the calculation of the free-space propagation delay from the CDA to the clock via the satellite. This delay value is then used with a delay generator to compensate for the free-space path delay.

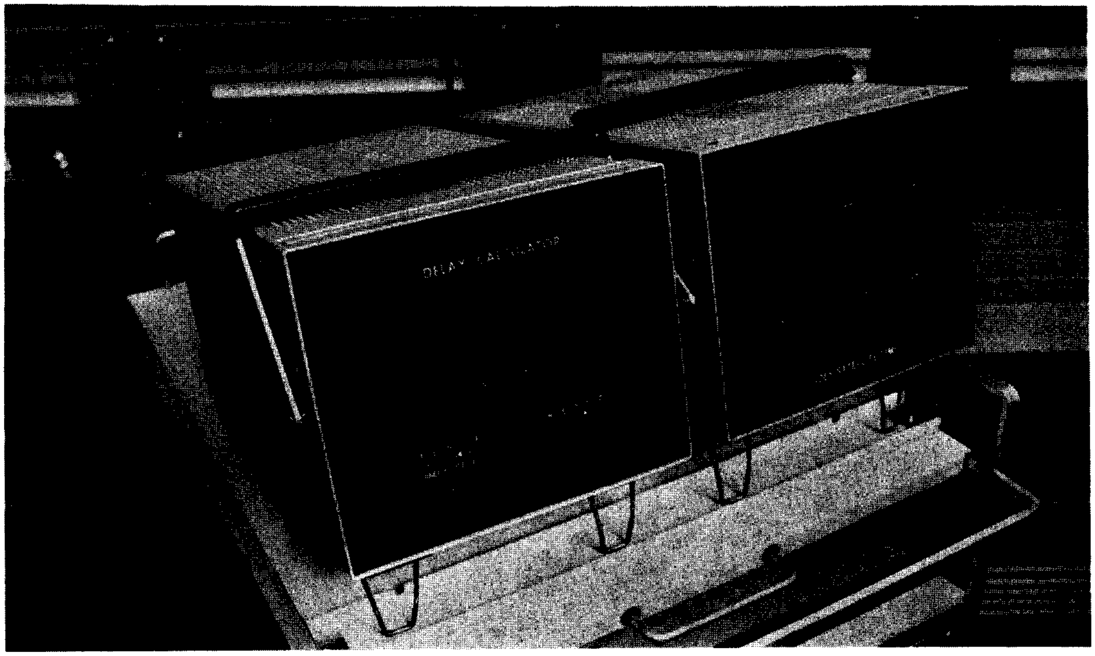

FIGURE 10. SMART CLOCK

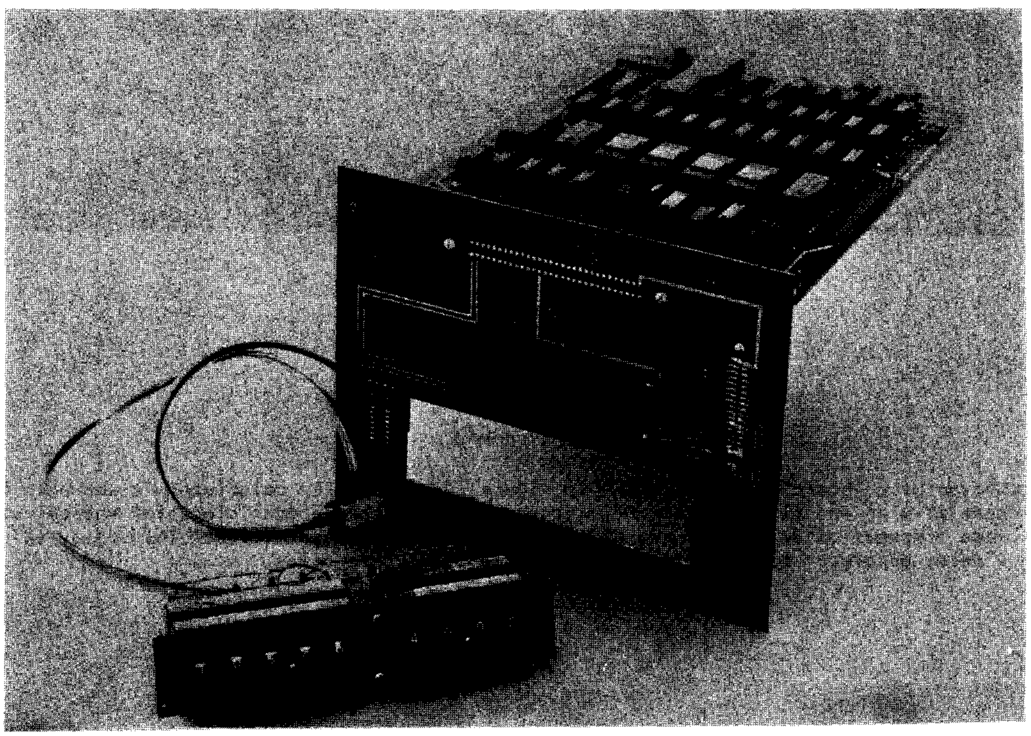

FIGURE 11. DELAY CALCULATOR

The "smart" clock uses the same type of four-bit microprocessor as the decoder clock. The microprocessor is interfaced to a large scale integration scientific calculator array (math chip) to provide the floating point arithmetic and mathematical functions required in the delay calculation. A 1-pps output and satellite position as longitude, latitude, and radial deviation from a reference orbit is obtained continuously from the decoder clock operating on the satellite's transmitted interrogation channel signal. User position is entered into the system via thumbwheel switches, and transmitter position (Wallops Island, VA) is contained in the microprocessor software. The computed delay drives a programmable delay generator to correct the 1 pps from the decoder clock. The resultant output from the programmable delay generator is a compensated 1 pps, adjusted to be in agreement with the master clock at Wallops Island, which is referenced to UTC(NBS). The hardware is a multiprocessor system consisting of two microprocessors plus a slaved scientific calculator chip and a delay generator.

The delay calculation is dependent on knowledge of the broadcasting satellite's position. This position is predicted in advance by a large scale scientific computer operating on orbital elements obtained from NOAA and sent to Wallops Island via telephone land line to be broadcast along with encoded time from each satellite. The delay correction system will work with any satellite in a synchronous orbit as long as the satellite's position is known. A calculation is made and the result is latched into the delay generator once per minute. A complete up and down delay calculation requires the execution of about 200 key strokes representing data and mathematical operations and functions under the control of the microprocessor and its associated transistor-transistor-logic (TTL) components.

6. MATHEMATICAL CONSIDERATIONS

The mathematics of the path-delay calculation require solving for length r in the geometry of figure 12; that is, the free-space propagation path between any point on the earth's surface and a geostationary satellite (see reference [3] for a more complete discussion of the calculation).

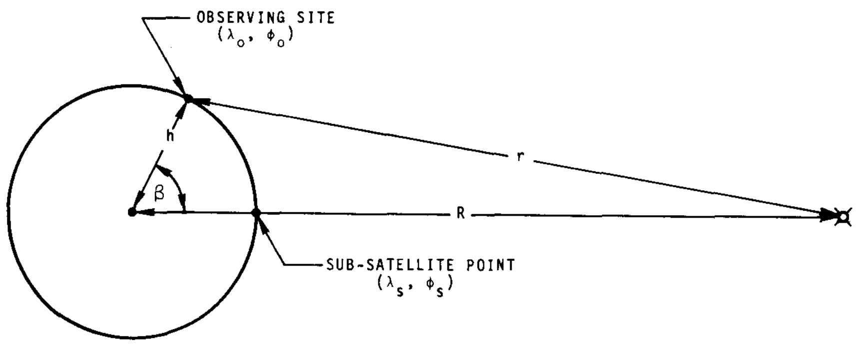

FIGURE 12. EARTH SATELLITE GEOMETRY FOR SLANT RANGE CALCULATION

Referring to figure 12 and using plane trigonometry:

$$r = \sqrt{R^2 + h^2 - 2Rh \cos \beta}, \tag{1}$$

where r is the range from any point on the earth's surface to the satellite, R is the distance from the satellite to the center of the earth, h is the distance from the receiver to the center of the earth, and β is the central angle between the subsatellite point and the given point. The quantity R is a component defining the satellite's position and is provided in the satellite time-code broadcast. The quantity h is related to the geodetic latitude ϕ of a site by the following equation:

$$h = a \sqrt{\frac{1 + \frac{b^4}{a^4} \tan^2 \phi}{1 + \frac{b^2}{a^2} \tan^2 \phi}}, \tag{2}$$

where a = 6378.2064 km, the earth's semi-major axis; and b = 6356.5838 km, the earth's semi-minor axis (see reference [4]).

The geocentric latitude, ϕ' is related to the geodetic latitude, ϕ, by the following equation.

$$\tan \phi' = \frac{b^2}{a^2} \tan \phi \ . \qquad (3)$$

In the following discussion λ indicates longitude, and subscripts s and r denote subsatellite point and any other point on the earth's surface respectively.

Only cos β remains to be computed. The direct solution may be obtained from the triangle consisting of the subsatellite point, the observing point, and the intersection of the z-axis (i.e., the North Pole). Using spherical trigonometry and figure 12:

$$\cos \beta = \sin \phi'_r \sin \phi_s + \cos \phi'_r \cos \phi_s \cos (\lambda_s - \lambda_r). \qquad (4)$$

These equations are programmed directly by storing key stroke sequences in programmable read-only memories (PROM's) and executing them in the scientific calculator array under microprocessor control. The calculation is repeated, first using the transmitter position for the up delay and then using the receiver position for the down delay. The two delays are summed and used in driving the delay generator. The computed delay is subtracted from 300,000 µs[1] and tens-complemented before being output to the delay generator. Tens-complementing is required because the programmable delay generator uses BCD counters which count in the up direction rather than the down direction. The delay generator setting is also multiplied by 1.024 because one count of the delay generator is equal to 1 ÷ 102,400 Hz = 0.9765625 µs. This frequency is derived from the satellite-controlled digital clock (see figure 13).

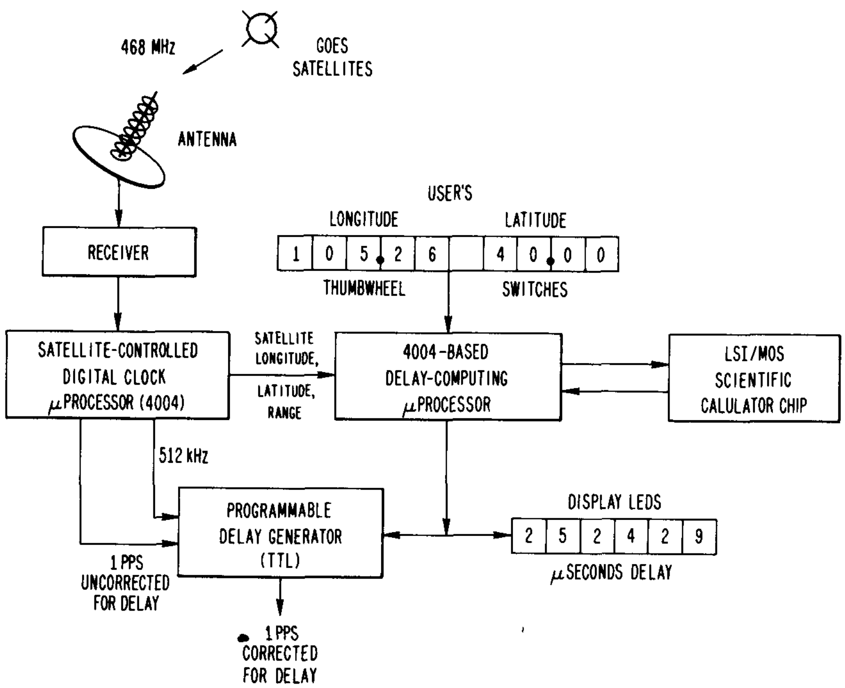

FIGURE 13. AUTOMATIC DELAY CORRECTING SYSTEM BLOCK DIAGRAM

[1]The time at the CDA is advanced by 260,000 µs so it arrives nearly on time at the earth's surface. The delay generator is programmed to delay the decoder clock's 1 pps by 300,000 µs minus the computed free-space path delay, thus guaranteeing a positive (delay) value since negative values (an advance) cannot be implemented. Additional delay can be made through software to compensate for transmitter (CDA), satellite, receiver, and decoder-clock delays, when known, to place the corrected 1 pps in synchronism with the clock at the CDA.

7. SYSTEM HARDWARE

Early in the development effort a decision had to be made about the method to use for the delay calculation; that is, whether the calculation should be implemented through software or hardware. A software package for doing floating-point arithmetic and mathematical functions was available. Scientific calculators and their large scale integrated circuit chips were also available and their advantages were weighed against the software approach. Calculation execution times for multiply, divide, and the various mathematical functions were comparable in both methods and were not a factor in the decision. A software mathematical package for the four-bit microprocessor required about 750 eight-bit bytes or three programmable read-only memory (PROM) chips for program storage. This meant that even the software method would require extra hardware. The scientific calcuator chip required extra hardware, but since it appeared to have more accuracy and range (scientific notation with dynamic range of 10^{99} to 10^{-99}), more mathematical functions, and looked to be generally more flexible, it was the method chosen. In addition, an existing hardware design was found for interfacing a scientific calculator chip to an eight-bit microprocessor that could also be used for a four-bit microprocessor. The software for this design could not be used, however, and new four-bit software had to be written. A four-bit microprocessor was used largely because of past experience with that type. The speed of a newer eight-bit microprocessor could not be used advantageously because of the slowness of scientific calculator chips in general. A four-bit word size was adequate since the task consisted largely of manipulating four-bit hexadecimal characters in and out of the calculator chip or RAM or to the delay generator and display board.

The decision was made to use the four-bit microprocessor and a large scale integration scientific calculator chip. The microprocessor is shown in figures 14 and 15. The system has been in operation at NBS for several months and its performance shows that the decision was more than satisfactory. The system has very powerful, accurate, and flexible computational capability at low cost and with high reliability. Key stroke codes must be entered into the math chip and held for 40 ms with a 40-ms delay between entries of key codes. Some of the mathematical functions such as sin and cos require about 1 1/2 seconds to perform. One complete calculation of the total up and down delay, the execution of about 200 key strokes, requires about 1 minute. Satellite position information is output from the decoder clock twice per minute at 0s and 30s. The delay microprocessor idles, waiting for the satellite position information. When the satellite position is available it is read by the delay microprocessor, stored in RAM, and the delay calculation finished. A complete calculation is performed and the delay generator is reset once per minute.

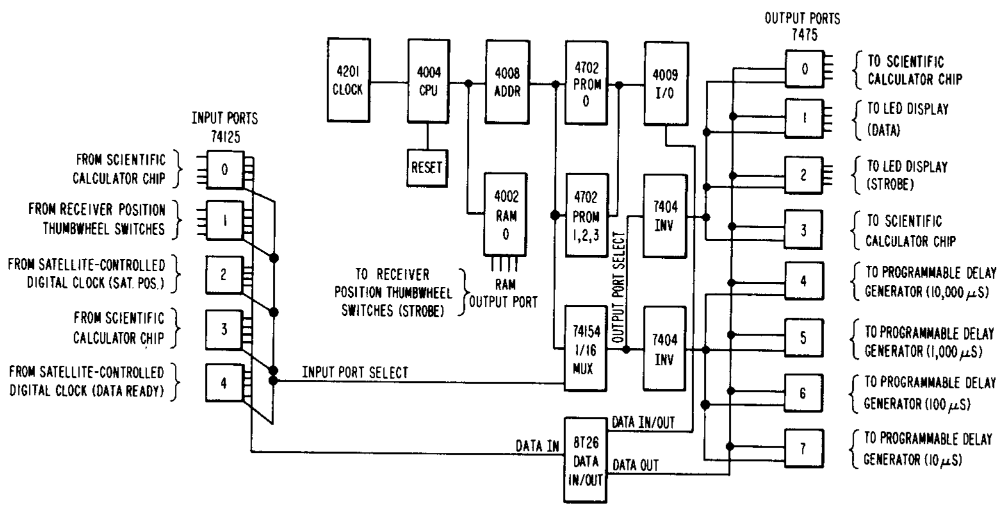

FIGURE 14. MICROPROCESSOR BLOCK DIAGRAM

Since the delay calculations always fall somewhere between 100,000 and 400,000 μs, the decimal point is assumed to be between the seventh and eighth digits of the calculator chip output. The decimal point on the display board can therefore be wired.

Approximately once in every ten different computations, the result will contain one or more trailing zeros. If this happens, since the calculator chip doesn't output trailing zeros for display, the decimal point will be shifted. The software always checks for this condition and adds 0.01 to the result, thus forcing the decimal point back between digits seven and eight. The range of the programmable delay generator setting is always between 10,000 and 90,000, so if a decimal point shift occurs, 0.001 is added to the result to again put the decimal point back between digits seven and eight.

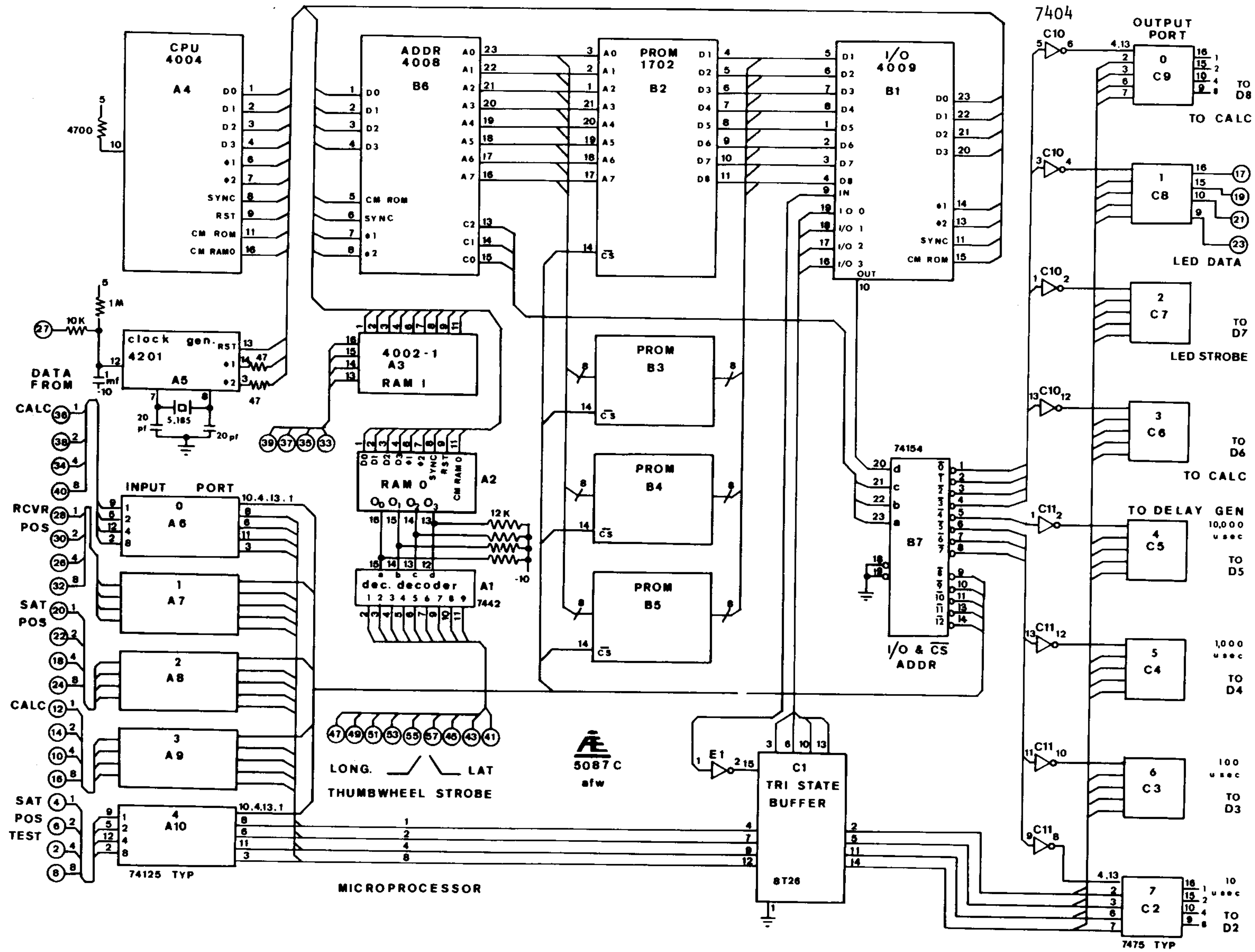

FIGURE 15. MICROPROCESSOR WIRING DIAGRAM

The delay microprocessor has five four-line input ports and nine four-line output ports, including one RAM output port, which are used as follows:

Output Port:

0	to scientific calculator chip	(Least significant part of key code)
1	to LED delay display	(data)
2	to LED delay display	(strobe)
3	to scientific calculator chip	(Most significant part of key code)
4	to programmable delay generator	(10,000 μsec)
5	to programmable delay generator	(1,000 μsec)
6	to programmable delay generator	(100 μsec)
7	to programmable delay generator	(10 μsec)

RAM Output Port:

0	to receiver position thumbwheel switches	(strobe)

Input Port:

0	from scientific calculator chip	(LED code)
1	from thumbwheel switches	(user position)
2	from satellite-controlled digital clock	(satellite position)
3	from scientific calculator chip	(LED code)
4	from satellite-controlled digital clock	(satellite position data ready)

One random access memory (RAM) chip is used for storage of transmitter, receiver, and satellite positions and for storage of math chip results. Figure 16 is the RAM register map showing how the RAM is organized. Total RAM storage available on the chip is 80 four-bit BCD characters.

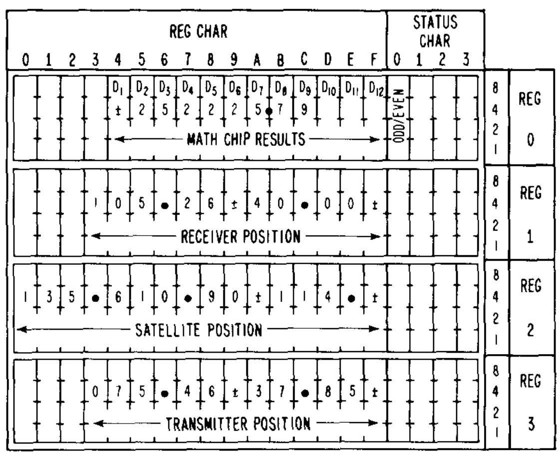

FIGURE 16. RAM REGISTER MAP

Figure 17 shows the scientific calculator chip microprocessor interface. The interface was designed by Dr. Robert Suding of the Digital Group, Denver, Colorado. The design requires two 4-bit input and two 4-bit output ports. The calculator chip is normally connected to a 12 x 4 matrixed keyboard giving a 48 key input capability. Only 41 keys are actually used. Each key can be represented by a 2-digit hexadecimal key code as shown in figure 18. In normal operation with a keyboard,

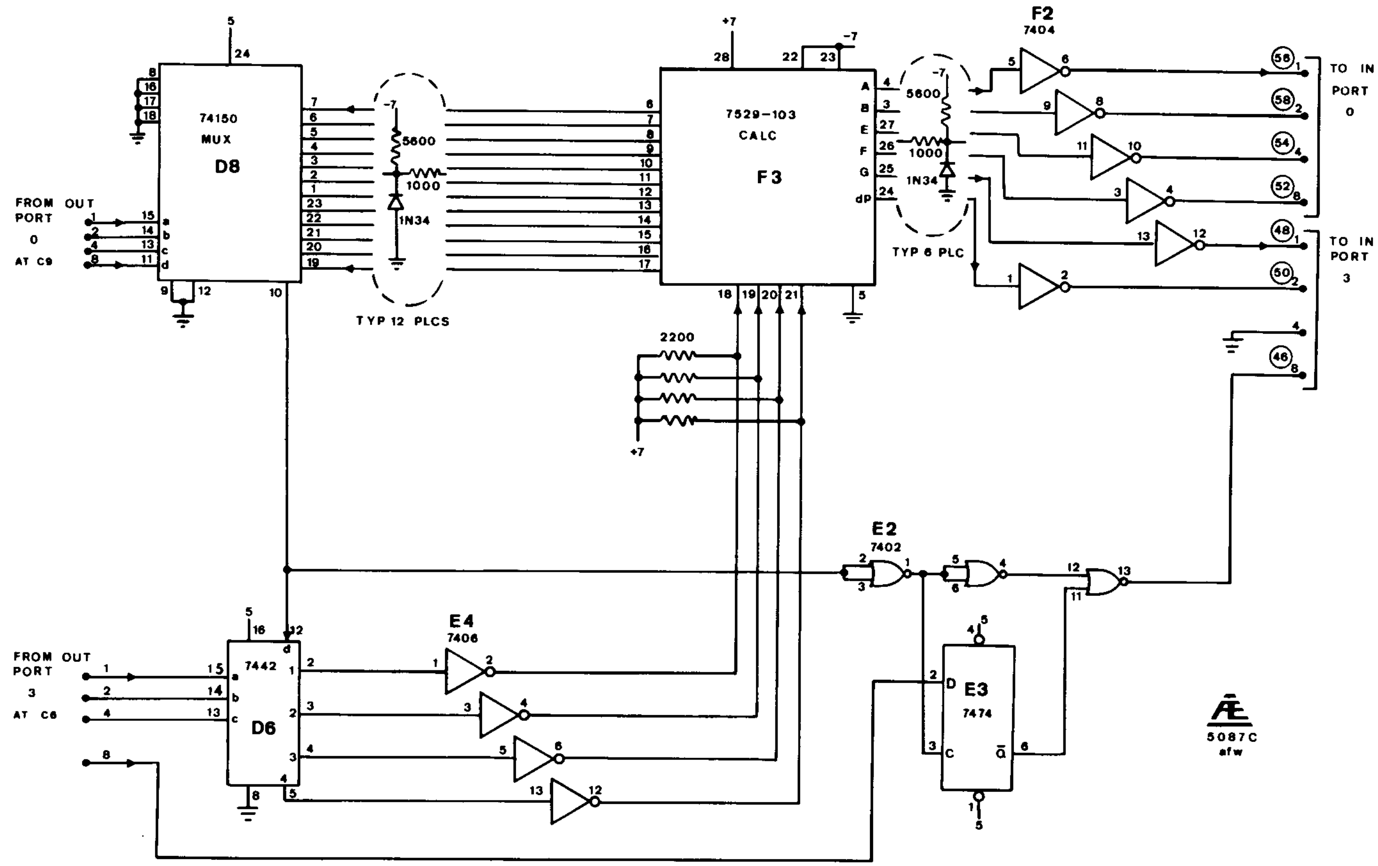

FIGURE 17. SCIENTIFIC CALCULATOR CHIP INTERFACE

the calculator chip outputs a time sequence of pulses on pins 6 through 17, one at a time. Then, depending on which key is depressed, one of the 12 pulses appears on one of the four Y input lines to the chip. The combination of a pulse at 1 of the 12 digit times on one of the four Y input lines provides the calculator chip with information on which one of the 48 possible keys has been depressed.

INPUT CODES FOR FUNCTION ENTRY

FUNCTION	HEX	FUNCTION	HEX	FUNCTION	HEX	FUNCTION	HEX
0	11	ARC	1B	+	22	CA/CE	3C
1	12	SIN	31	-	23	CHS	2B
2	13	COS	32	x	24	EEX	2C
3	14	TAN	33	÷	25	y^x	26
4	15	LN	34	=	27	{	28
5	16	LOG	35	π	2A	}	29
6	17	RCL	37	$\sqrt{\ }$	36	10^x	43
7	18	Σ	38	1/x	41	e^x	44
8	19	x↔y	39	x^2	42	N!	45
9	1A	DGR	3A	No Op	00	Restore-Display	1C
.	21	STO	3B				

INPUT CODES FOR DIGIT DATA REQUEST

DIGIT	HEX	DIGIT	HEX	DIGIT	HEX	DIGIT	HEX
1	81	4	84	7	87	10	8A
2	82	5	85	8	88	11	8B
3	83	6	86	9	89	12	8C

OUTPUT CODES FOR SEGMENT DECODE

DIGIT ALONE	HEX	DIGIT AND DECIMAL PT	HEX	DIGIT ALONE	HEX	DIGIT AND DECIMAL PT	HEX
0	4F	0.	6F	7	43	7.	63
1	42	1.	62	8	5F	8.	7F
2	57	2.	77	9	5B	9.	7B
3	53	3.	73	-	50	-.	70
4	5A	4.	7A	ERROR	4D	ERROR.	6D
5	59	5.	79	ERROR	5D	ERROR.	7D
6	5C	6.	7C	BLANK	40	BLANK.	60

FIGURE 18. SCIENTIFIC CALCULATOR CHIP INPUT, DATA REQUEST AND OUTPUT CODES

The interface was designed to provide the same action as the keyboard but under microprocessor control. The least significant hexadecimal digit of the code is output by the microprocessor into the 1-2-4-8 input lines of the 74150 data selector to select one of 12 lines connected to the calculator chip. At the selected digit time the "8" line (pin 12) of the 7442 BCD-to-decimal converter goes low. At the same time the most significant digit of the hex key code, from output port 3, is going into the 7442 1-2-4 lines. Since the 7442 "8" is now low, one of its 1-2-3-4 decimal output lines, connected to the calculator Y inputs, can be high depending on the digit input. This provides the same effect as depressing a keyboard key, but it is now under microprocessor control. The "8" bit of output port 3 is used for requesting output data for a specific digit. For example, if data for digit 3 are desired, data request code 83 is output, the 8 from output port 3 and the 3 from output port 0. At the 3-digit time, pin 10 of the 74150 data selector goes low and is fed, through an inverter, to the clock input of a 7474 flip-flop. The "8" part of the data request code is connected to the data input of the 7474 and is clocked through at the 3-digit time. The 7474 $\overline{Q}$ output and the 7474 clock input (through an inverter) are connected to a NOR gate which provides a positive pulse that stays high during all of the 3-digit time.

Now the microprocessor only needs to test the "8" bit of its 3 input port for high (negative logic 0) to know when the 7-segment LED data are valid for digit 3. The microprocessor then reads input port 0 and, with the other three bits of input port 3, has all the information necessary to decode the 7-segment LED data into a BCD character. Note that only 5 of the 7 LED segments are required to decode all 10 BCD characters. The decimal point output of the calculator chip is used only for detecting when the calculator chip is "DONE;" that is, when it is providing output. Since the digit 9 decimal point is always used for output, regardless of what the output might be, digit 9 is used for "DONE" testing. To test for "DONE," data request code 89 is output and the decimal point ("2" bit of input 3) is tested for high. When the decimal point is high, the microprocessor knows that the calculator chip is finished and it either reads the 7-segment LED data for all the calculator chip output digits or it knows that entry of a key stroke is complete and enters the next key stroke.

The design of the calculator chip requires a key to be held down for at least 40 ms and when released no other key may be pressed for 40 ms. These delays have been implemented by the microprocessor software to provide the equivalent effect. Figure 18 shows the digit data request codes and the 7-segment LED output codes.

Figure 19 shows details of the programmable delay generator. The delay generator setting for the 10's of μs comes from output port 7 and the settings for 100's of 1000's of μs and 10,000's of μs from output ports 6, 5 and 4 respectively. Half of a 7490 is used to divide the 512 kHz input by five. The 512 kHz comes from the satellite-controlled digital clock which is phase locked to the incoming satellite radio signal derived from the atomic clock standards at Wallops Island. The period of the 102.4 kHz from the divide by five counter is 9.765625 μs instead of exactly 10 μs. This difference is compensated in the microprocessor/calculator chip software by multiplying the delay generator setting by 1.024.

The delay generator uses five 74196 presettable decade up counters. The down-going edge of the 1-Hz pulse from the satellite-controlled digital clock loads four of the counters with the data latched into the four microprocessor output ports and starts the counters counting in the BCD up direction. The fifth counter is preset to "1" and its output (Q1, pin 5) is the 1-Hz output with the proper delay applied. The 1-Hz delayed output is also fed back to the first decade counter (10's of μs) to stop the counting.

A 7474 flip-flop was added to the satellite-controlled digital clock to make its 1-pps output coherent with the received 100 Hz satellite signal. Because the output from the digital clock is under microprocessor control, the exact number of instruction steps between the 1 pps varies. The 7474 allows the 1 pps into the delay generator only at rising edge times of the 100 Hz signal. A 74121 monostable multivibrator is used to give the 1 pps delayed output a constant 10 ms pulse width.

Figure 20 shows the 7-segment LEDS which display the calculation results, the uplink delay and the total uplink plus downlink delays. The display is a convenient monitor of the delays as they are computed. A programmable pocket calculator is used to check the calculations if there is any reason to doubt the displayed results.

The display uses a 7442 BCD-to-decimal converter, connected to output port 2, to strobe the TIL-308 LED display digits one at a time. BCD data from output port 1 are connected to all of the LED digits in parallel. Note that all decimal points are wired "off."

Figure 20 also shows the longitude and latitude thumbwheel switches for input of receiver position. RAM output port 0 is used to strobe the switches one by one and their setting is read into input port 1 and the data are stored in RAM. Five digits of longitude and four of latitude are entered. Figures 21-26 provide board layout and component location.

8. SYSTEM SOFTWARE

The software for the delay microprocessor/scientific calculator chip consists of a main program and 17 subroutines plus an area of PROM for storing the hexadecimal key code equivalents of key strokes. Program storage requires four 256 x 8 PROMs. The program was written to make the package as modular as possible; that is, to keep the main program simple and straightforward, using subroutines wherever practicable. Each program is discussed below in the order it is stored in PROM.

MAIN PROGRAM, 0-00 to 0-DF, uses about 240 bytes and controls the use of the subroutines as shown by the software flowchart, figures 27 and 28. Odd numbered passes through the main program compute the transmitter-to-satellite path delay in microseconds and store it in RAM register 0. Even passes compute the satellite-to-receiver delay. The two delays are then summed, giving the total delay over the path. The computation is identical for all passes through the program, but the up delay uses the transmitter position and the down delay uses the receiver position. RAM register 0 status character counts the number of passes through the program and is tested for odd or even. If odd the up delay is computed and if even the down delay is computed. Total delay is subtracted from the total clock advance of 300,000 μs and a programmable delay generator setting is computed and output.

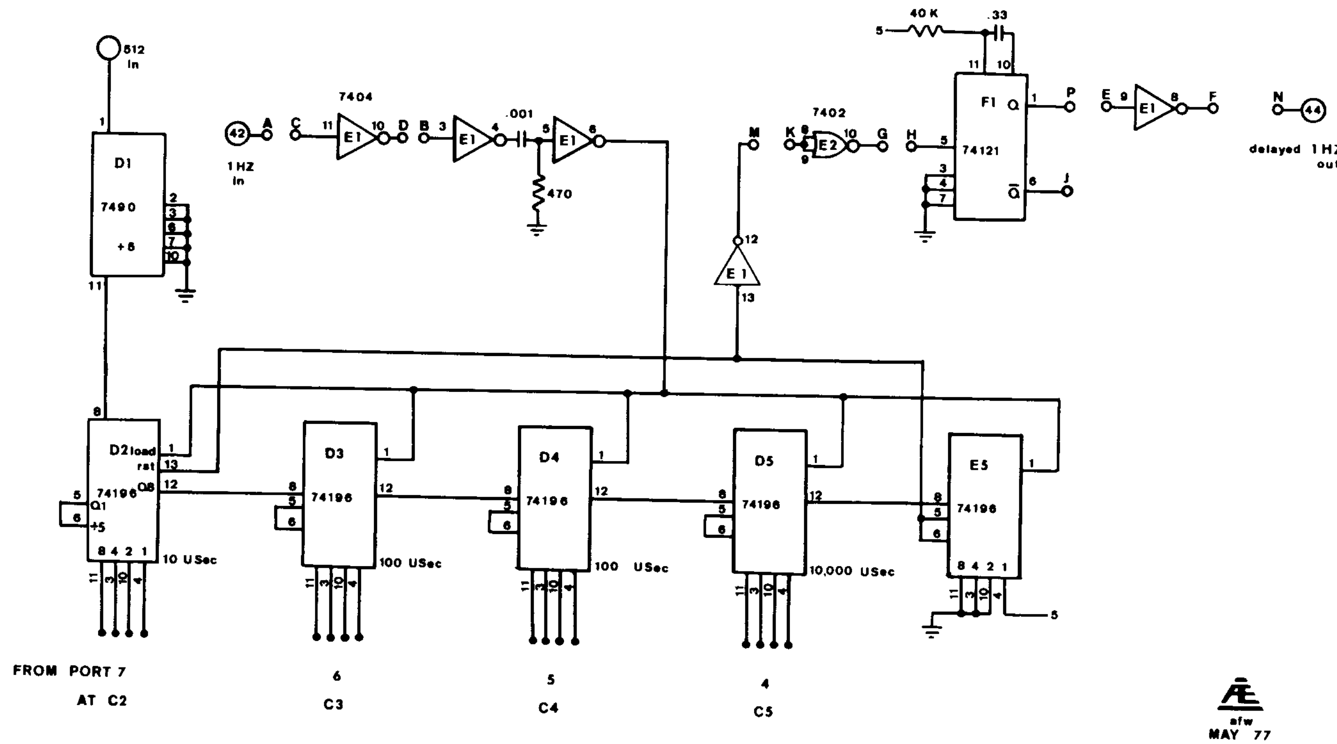

FIGURE 19. PROGRAMMABLE DELAY GENERATOR

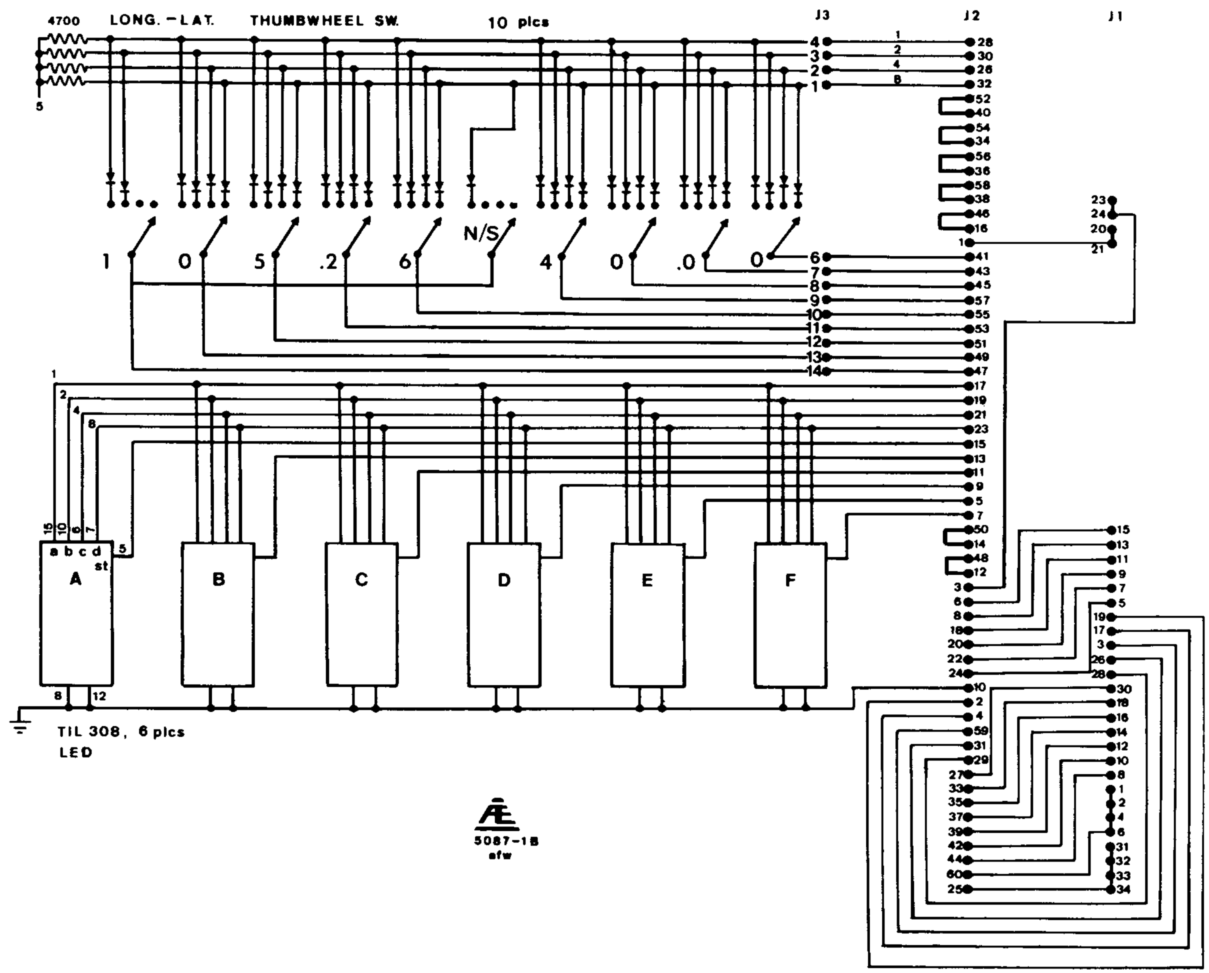

FIGURE 20. DELAY DISPLAY AND INPUT POSITION SWITCHES

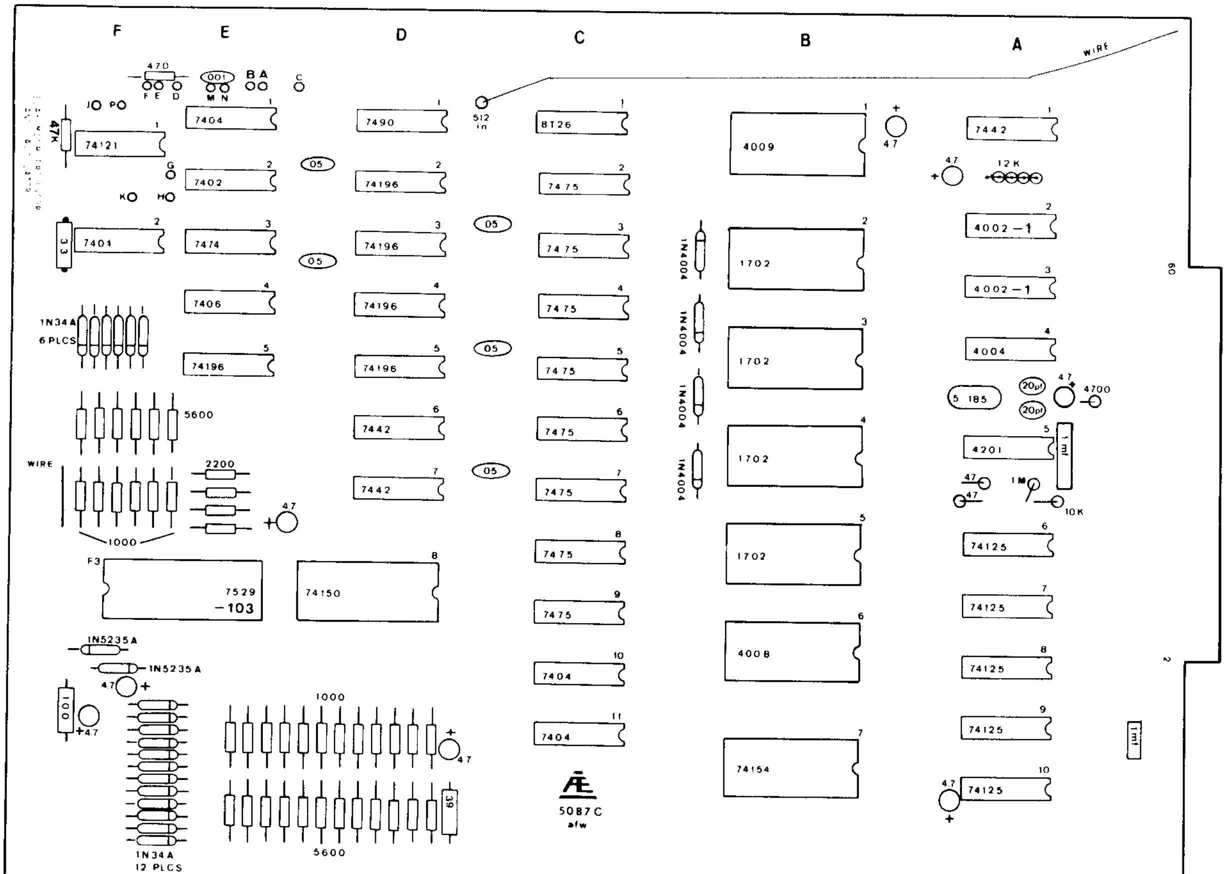

FIGURE 21. MICROPROCESSOR/CALCULATOR COMPONENT LAYOUT.

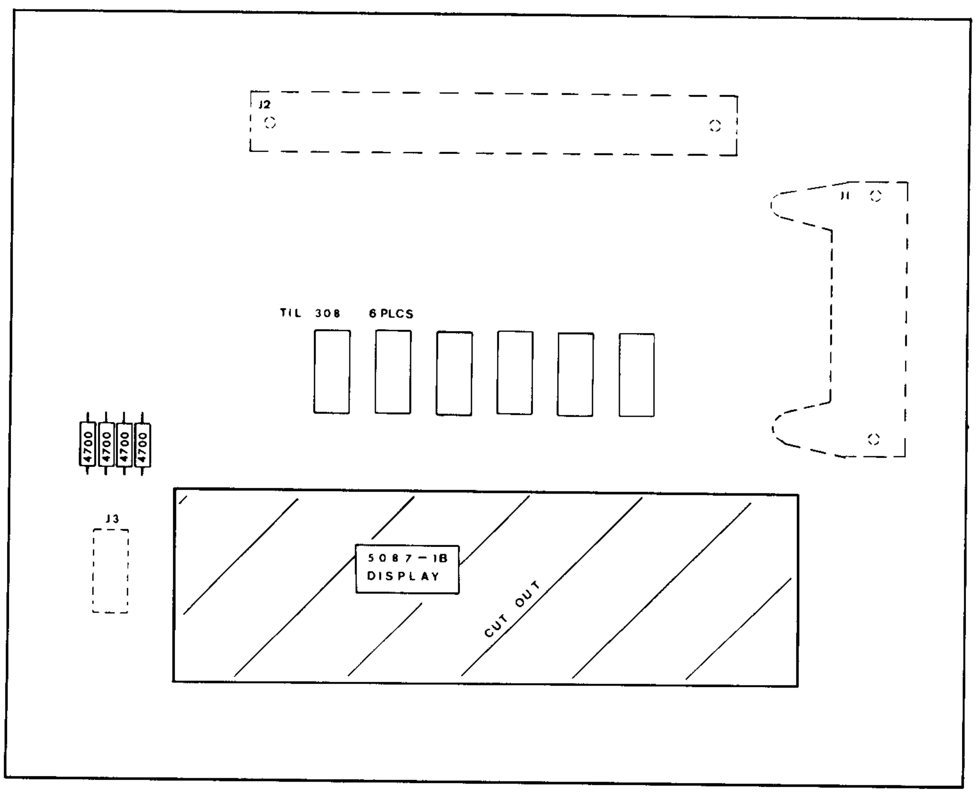

FIGURE 22. DISPLAY BOARD COMPONENT LAYOUT.

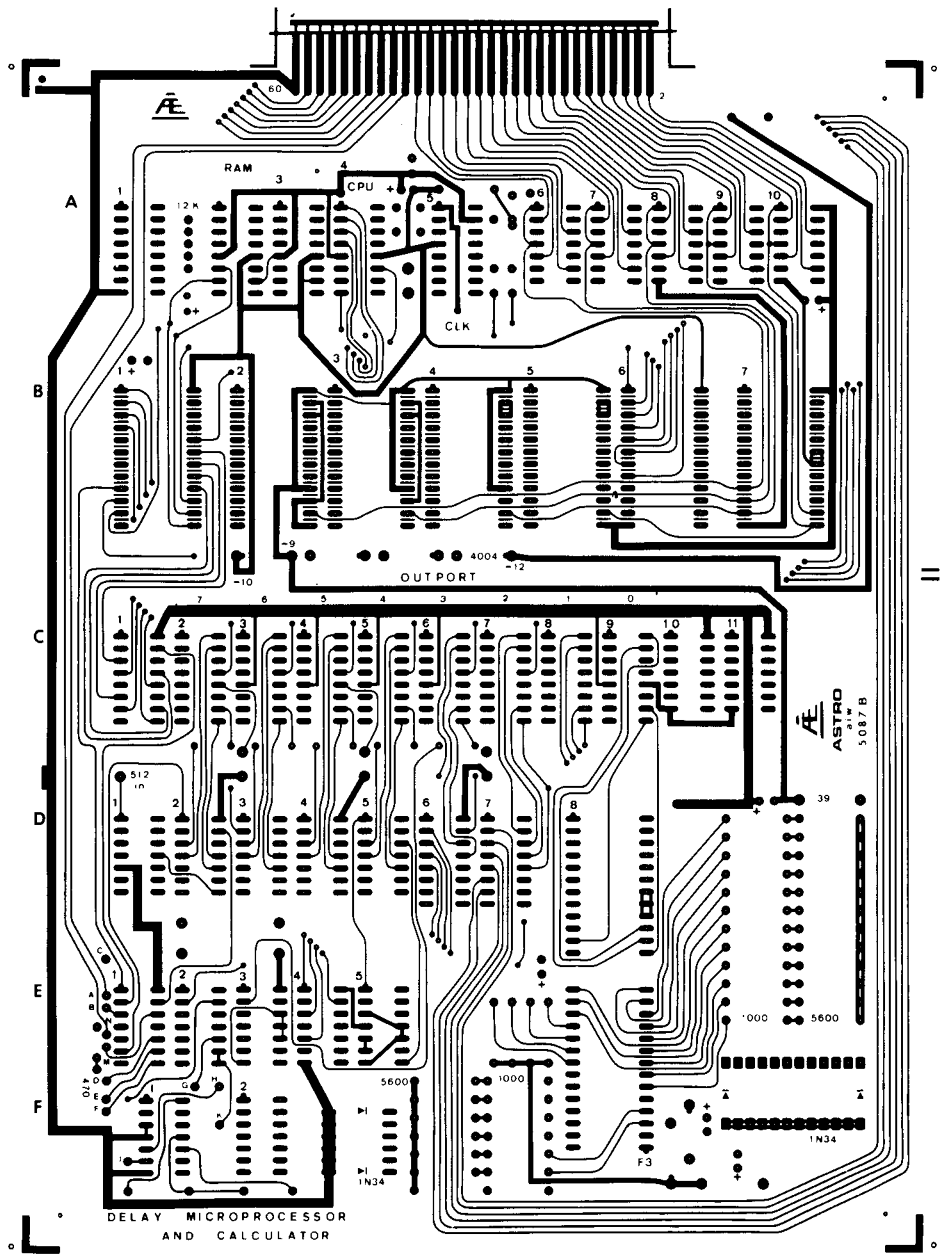

FIGURE 23. MICROPROCESSOR/CALCULATOR BOARD (FRONT).

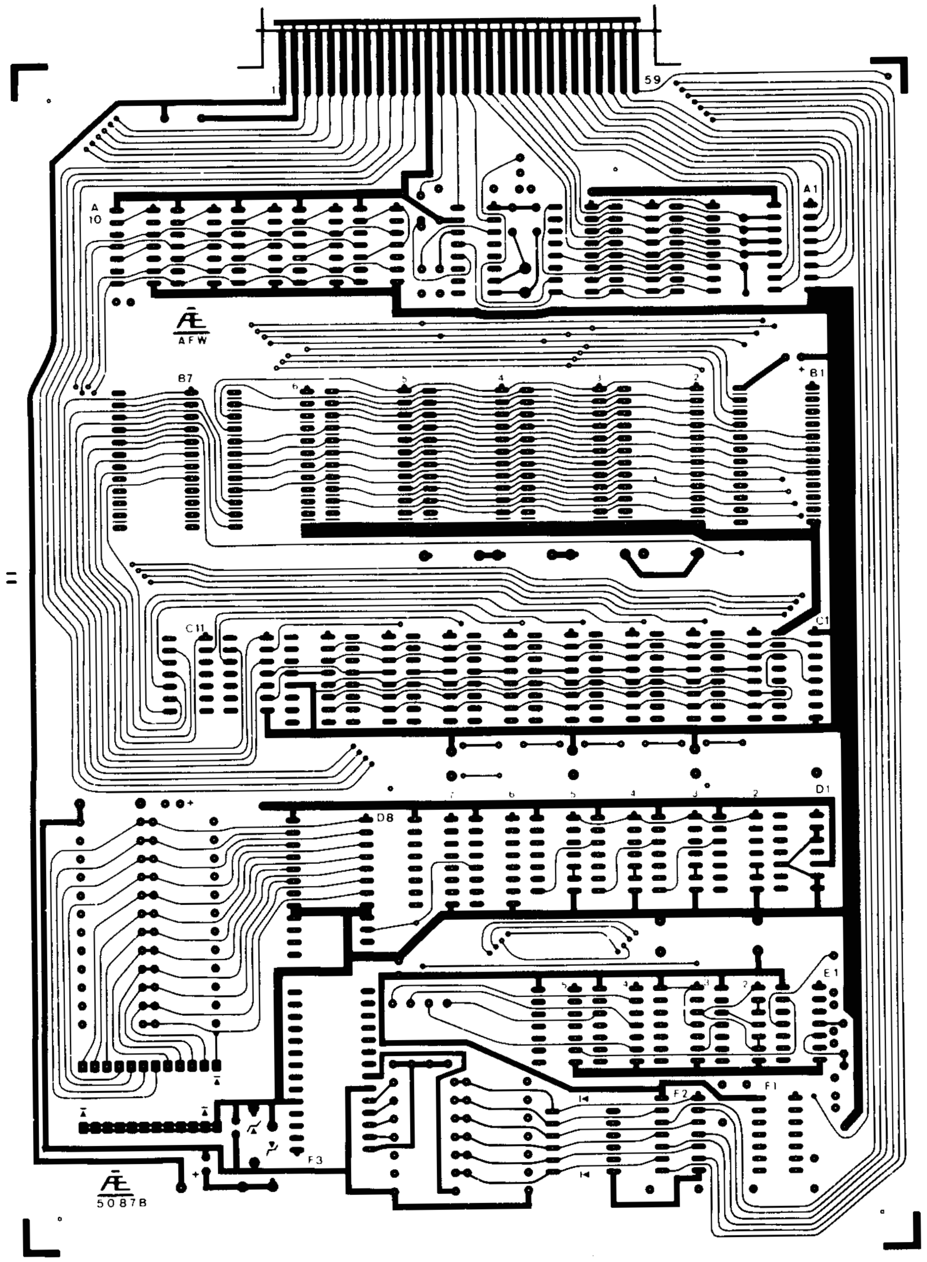

FIGURE 24. MICROPROCESSOR/CALCULATOR BOARD (BACK)

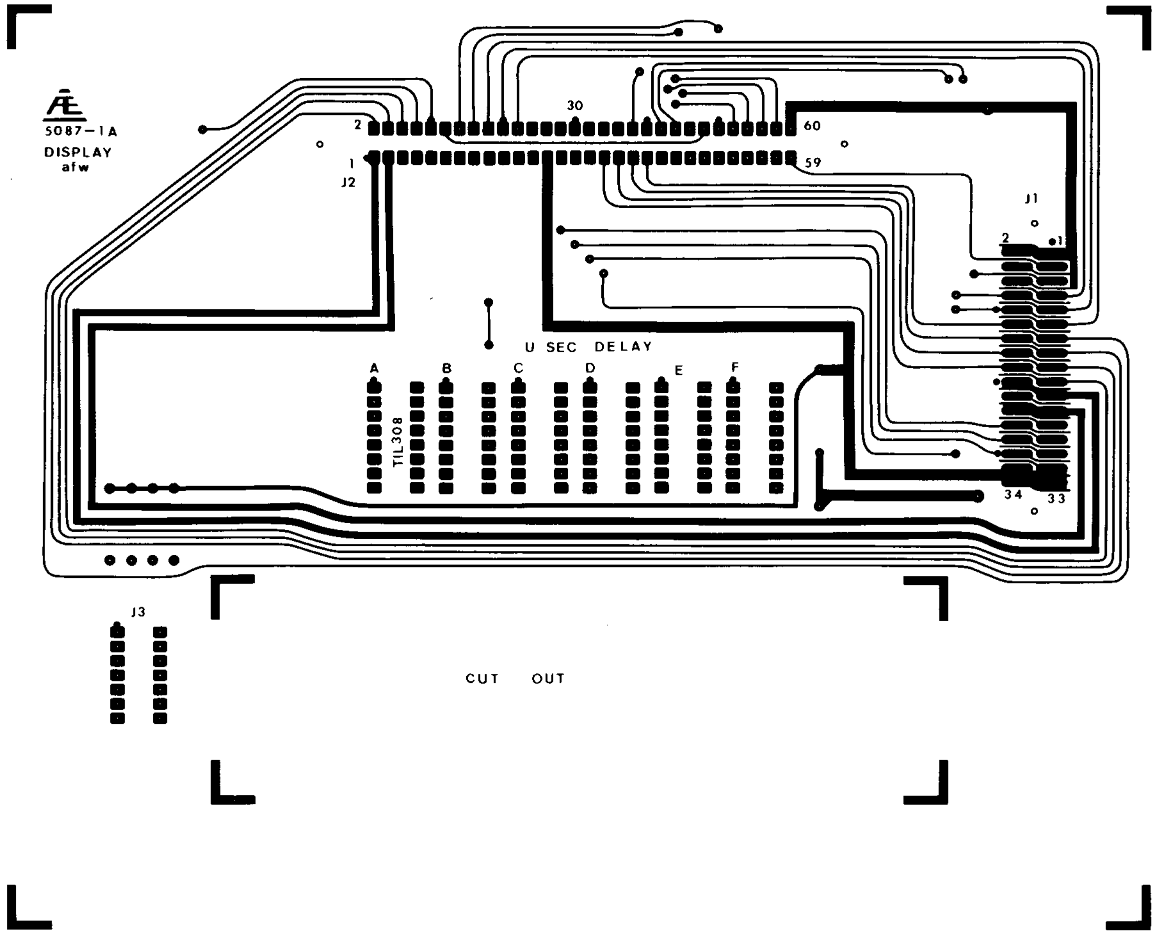

FIGURE 25. DISPLAY BOARD (FRONT)

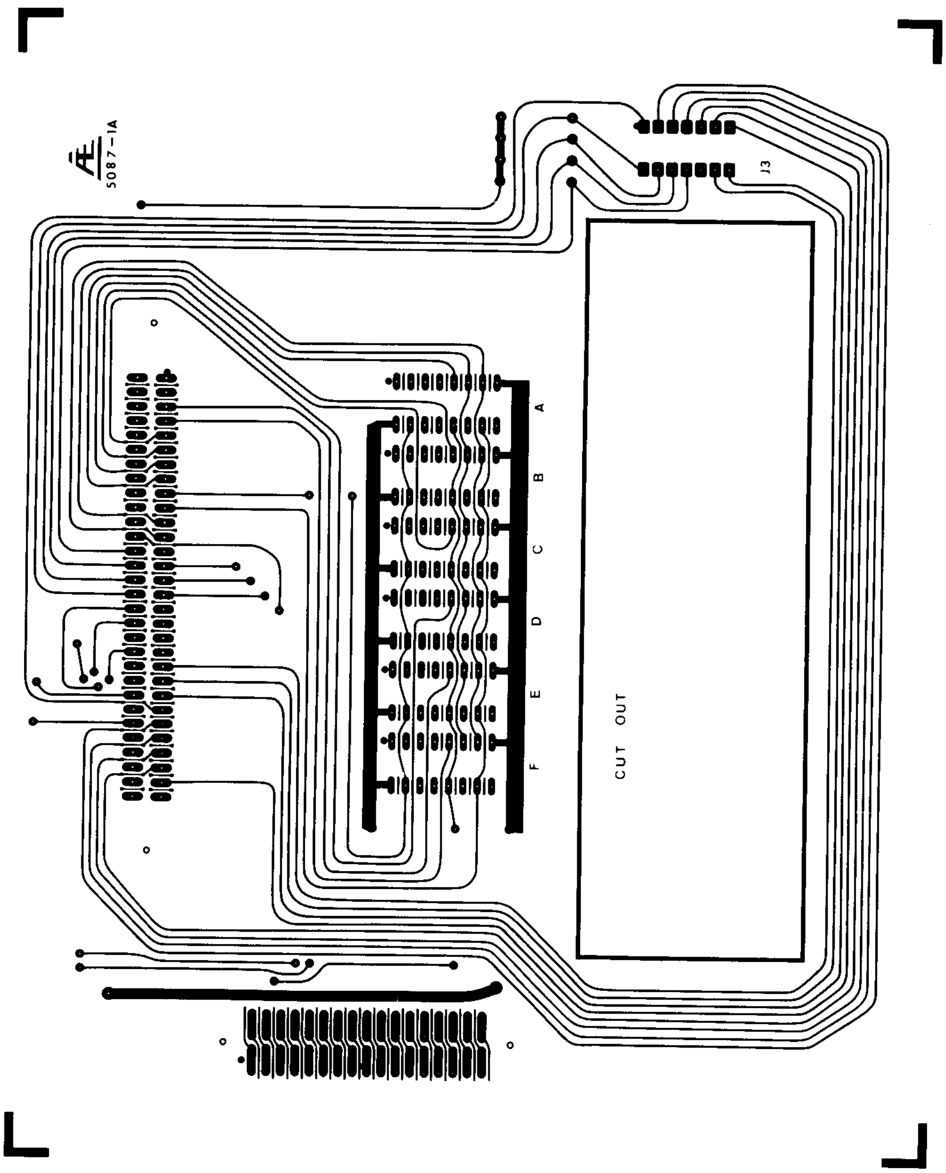

FIGURE 26. DISPLAY BOARD (BACK)

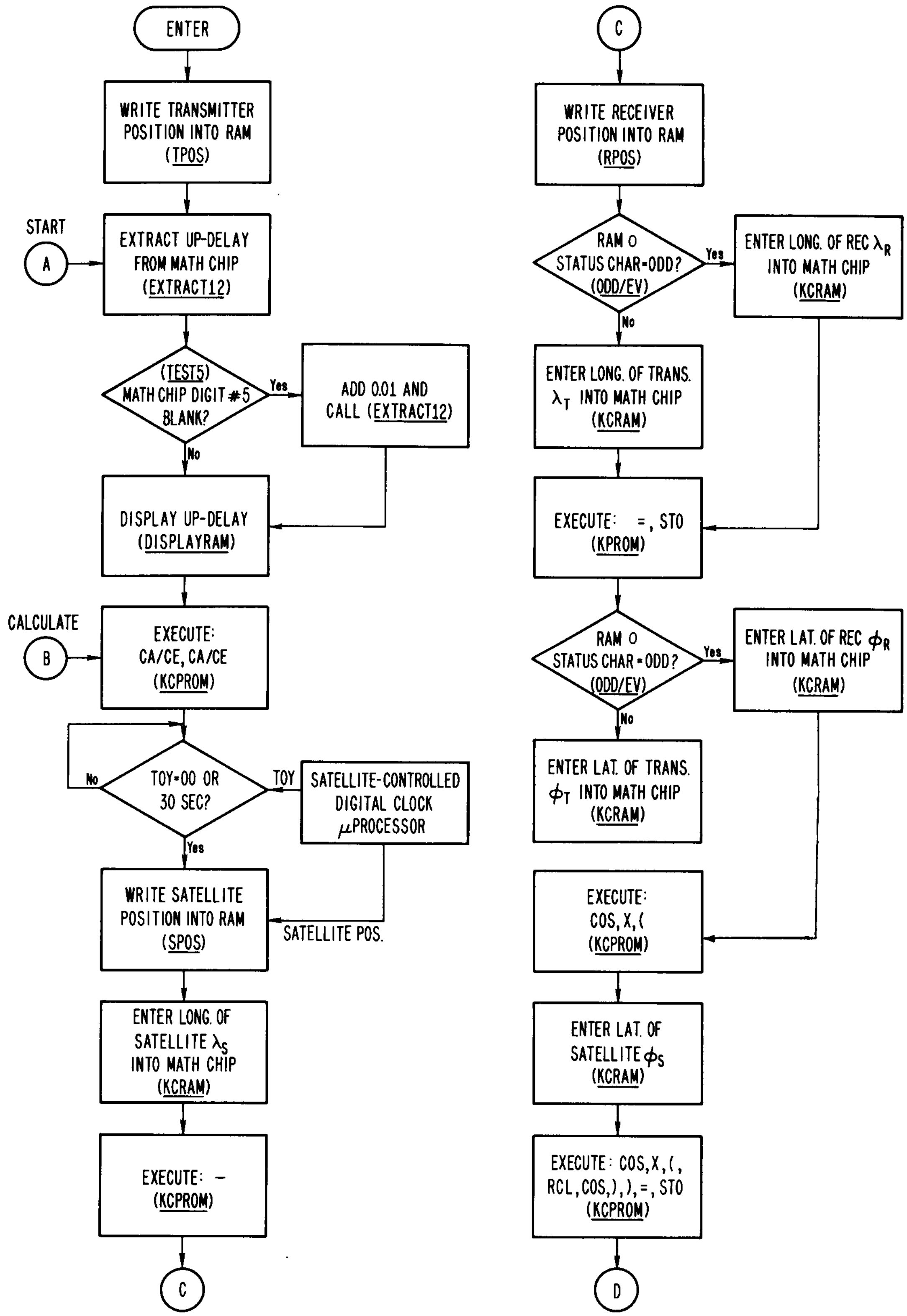

FIGURE 27. SOFTWARE FLOWCHART

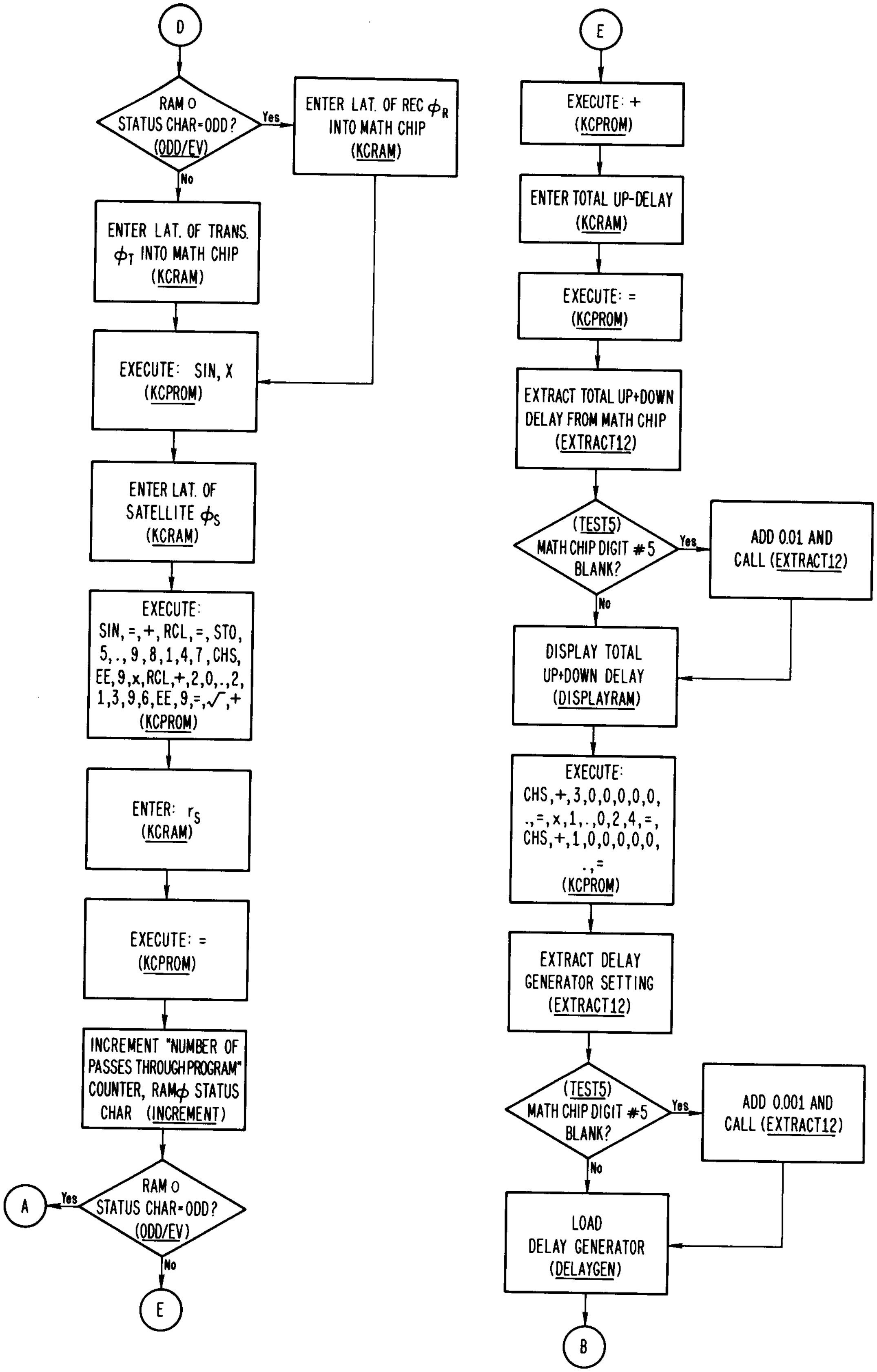

FIGURE 28. SOFTWARE FLOWCHART (CONTINUED)

TEST5, 0-F0 to 0-FF (16 bytes), is used for testing the math chip output 5 digit for blank. If found to be blank, then one or more trailing zeros have occurred in the result and 0.01 is added to the result to move the decimal point back to its assumed position between digits 7 and 8. Index register pair 0 and pair 4 are set up to add the 0.01, but the actual call to KCPROM to do the addition must be made in the main program to avoid exceeding the limit of three levels of subroutines of the 4004.

KCRAM, 1-00 to 1-1B (28 bytes), reads specified BCD characters from RAM, encodes them into key codes, and calls INPUTKC to input the key codes to the math chip. KCRAM expects to find RAM/Reg./ Character address in index register pair 4 and register A of pair 5 to contain the number of characters to be entered. Register A contains F - (number of characters) + 1. For example, if seven characters are to be entered: RA is set to 9 = F - 7 + 1 using hexadecimal arithmetic. After reading the proper hexadecimal character from RAM into index register 1, and using P0 as an address, the FIN instruction puts the encoded equivalent of the hexadecimal character into P3. The key code contained in P3 is then entered into the math chip by subroutine INPUTKC.

INPUTKC, 1-20 to 1-3F (32 bytes), enters key codes into the math chip. First a no operation code (NOP = 00) is entered, and after 40 ms the key code is entered. After another 40 ms delay, the math chip is tested for "DONE" which is indicated by the appearance of a decimal point. The "DONE" indication may occur immediately after the second 40 ms delay if the key code for a single decimal digit is entered or as long as 1.5 s after the entry of a sin or cos function key code. Return to the calling program cannot happen until "DONE" occurs.

DECODE, 1-40 to 1-7F (64 bytes), is called by subroutine EXTRACT12 to convert the math chip 7-segment LED output code to BCD and store it in RAM. DECODE expects to find the most significant part of the segment code in R0 and the least significant part in R1. The FIN instruction using R0 and R1 as an address puts the decoded equivalent, or BCD character, into register pair 5 and it is then stored in RAM.

WRAM, 1-64 to 1-6C (9 bytes) is a subroutine called by TPOS and RPOS to write BCD characters into RAM.

TPOS, 1-80 to 1-9F (32 bytes), writes transmitter position into RAM0, register 3. In this case it is the latitude and longitude of Wallops Island, VA. TPOS calls subroutine WRAM to do the writing in RAM.

EXTRACT12, 1-A0 to 1-C0 (33 bytes), extracts the 12-digit mathematical result from the math chip in the form of 7-segment LED codes. DECODE is then called to convert the 7-segment LED codes to BCD characters and store them in RAM0, register 0. EXTRACT12 requests each of the 12 digits, one at a time, by outputting a digit request code and waiting for the "8" bit of input port 3 to become positive (negative logic "0"). When this happens, the most significant part of the segment code is available at input port 3 and the least significant part is available at input port 0. The digit request codes for digits 0 through 11 are 81 through 8B in hexadecimal notation. With the two-digit segment code contained in register pair 0, DECODE is called to decode and store the equivalent BCD character in RAM.

DISPLAYRAM, 1-C8 to 1-DC (21 bytes), displays the calculation result stored in RAM 0, register 0 on 7-segment LED displays. The display is used as an indication that the system is operating properly.

TESTN/S (1-E0 to 1-EE, 15 bytes), is called by subroutine RPOS to test the receiver position thumbwheel switches for a north or south latitude setting. Since the 8 bit of the longitude 100S position character is never used in a longitude setting is is wired to the north/south switch of the latitude switches. If the 8 bit = 0 north latitude is understood and if the 8 bit = 1 a minus sign (CHS key), indicating south latitude, is attached to the latitude reading.

DELAY40, 1-F2 to 1-FC (11 bytes) is called by INPUTKC to provide the 40 ms delay required by the math chip between the entry of key stroke codes.

INCREMENT, 2-08 to 2-0E (7 bytes), increments the RAM 0, register 0 status character which indicates the odd or even passes through the program; that is, the "up" delay and "down" delay passes.

ODD/EV, 2-0F to 2-1D (15 bytes), tests RAM 0, register 0 status character for odd or even numbered passes through the program and determines whether transmitter position data will be used for the "up" delay or receiver position data will be used for the "down" delay calculation. If odd, R8 is set equal to 1. If even, R8 is set equal to 3. Register pair 4, of which R8 is a part, is used by KCRAM to enter either the transmitter or receiver position into the math chip.

RPOS, 2-20 to 2-64 (69 bytes), reads the thumbwheel switches containing the receiver position and calls WRAM to write the data into RAM 0, register 1. RPOS calls READL/L to strobe the thumbwheel switches via RAM 0 output port and read in their data.

READL/L, 2-67 to 2-6F (9 bytes), is a subroutine called by RPOS to strobe and read receiver position data from thumbwheel switches.

DELAYGEN, 2-70 to 2-7D (14 bytes), reads the programmable delay generator setting from RAM 0, register 0 and outputs it to the delay generator.

SPOS, 2-80 to 2-D8 (89 bytes), waits for and reads satellite position data from the decoder clock. The position data are available only at 0s and 30s when the digital clock is updating its display hardware. Since the data are only present for a few machine cycles, they are read as quickly as possible into RAM 0, register 1 for temporary storage in RAM locations usually reserved for receiver position storage. After all 13 satellite position characters are read and stored in RAM, SPOS transfers them from RAM 0, register 1 to register 2 and inserts decimal point and CHS key codes wherever required. RAM 0, register 1 is then free to be used for its usual receiver position storage.

NCHARS, 2-E0 to 2-E9 (10 bytes) is a subroutine called by SPOS for writing BCD characters into RAM.

KEY CODE STORAGE, 3-00 to 3-DF (224 bytes), is an area used for storage of the key codes corresponding to the key strokes required by the calculation.

KCPROM, 3-E0 to 3-F4 (21 bytes) reads specified hexadecimal characters, representing key codes, that are stored in PROM and calls INPUTKC to enter the key codes into the math chip. When called, KCPROM expects to have the PROM address of the first key code in index register pair 0 and the last key code address + 1 in index register pair 4. The FIN instruction, with the PROM address in register pair 0, puts the key code into register pair 3. Pair 3 then transfers the key code to INPUTKC for entry into the math chip.

The appendix is a listing of the delay microprocessor's software. The program was punched into standard 80 column data processing cards only as a convenient method of documentation. The format of the listing is as follows:

Column	
1	Hexadecimal page or ROM chip number
2	Blank
3-4	Hexadecimal instruction address within ROM chip
5	Blank
6-7	Hexadecimal microprocessor instruction
8	Blank
9-18	1 to 10 character label
19	Blank
20-22	1 to 3 character operation mnemonic
23	Blank
24-33	1 to 10 character operand (data, register, condition, label, etc.)
34-37	Blank
38-80	Comments

Some 4004 instructions require two bytes, in which case the second line of the instructions may contain data or a jump address.

9. PERFORMANCE

The equation relating the time recovered from the satellite to the master clock at Wallops Island is given below.

$$\text{UTC(NBS)} - \text{SAT/NBS} = \overset{1}{(\text{UTC} - \text{CDA})} + \overset{2}{(\text{CDA EQUIP DELAY})} + \begin{pmatrix} 3 \\ \text{FREE SPACE} \\ \text{PROPAGATION} \\ \text{DELAY} \end{pmatrix} + \begin{pmatrix} 4 \\ \text{SATELLITE} \\ \text{TRANSPONDER} \\ \text{DELAY} \end{pmatrix} + \begin{pmatrix} 5 \\ \text{IONOSPHERE \&} \\ \text{TROPOSPHERE} \\ \text{DELAY} \end{pmatrix} + \begin{pmatrix} 6 \\ \text{RECEIVER \&} \\ \text{CLOCK} \\ \text{DELAY} \end{pmatrix}$$

Term 1 in this equation is known to better than 1 μs using the data logger at the CDA which compares the CDA clocks to Loran-C and TV line-10. Using the measurement setups of figure 29, the smart-clock output on the chart recorder will draw a straight line if the orbit predictions are accurate and all equipment delays are constants; i.e., terms 2, 4, 5, and 6. Figure 30 shows raw data for 28 days. Each data point represents an average of measurements taken in one day at one-half hour increments totaling 48 measurements per day. Figure 31 shows the same data after removing the CDA clock drift and the two jumps in delay which have been attributed to equipment changes at the CDA. The orbit predictions used to generate these data were derived from three sets of orbital elements extrapolating as much as 22 days beyond their date.

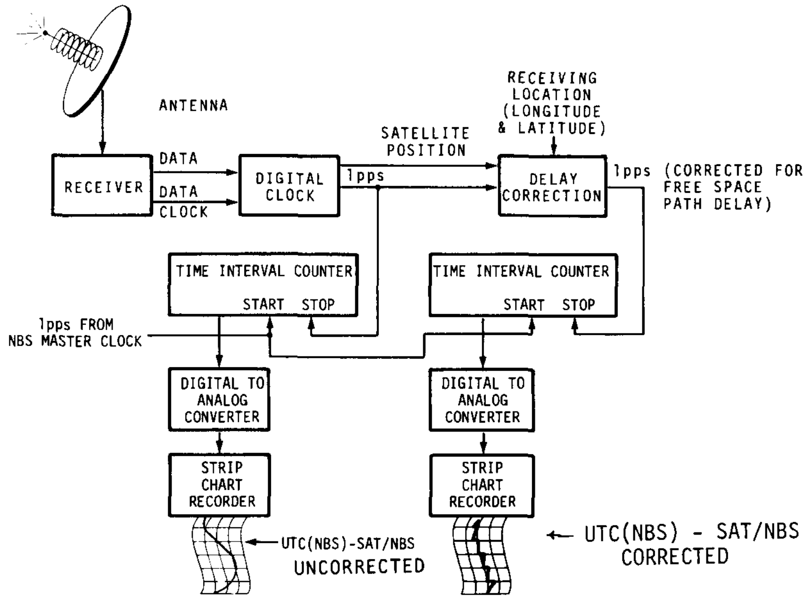

FIGURE 29. MEASUREMENT OF UTC(NBS) - SAT/NBS

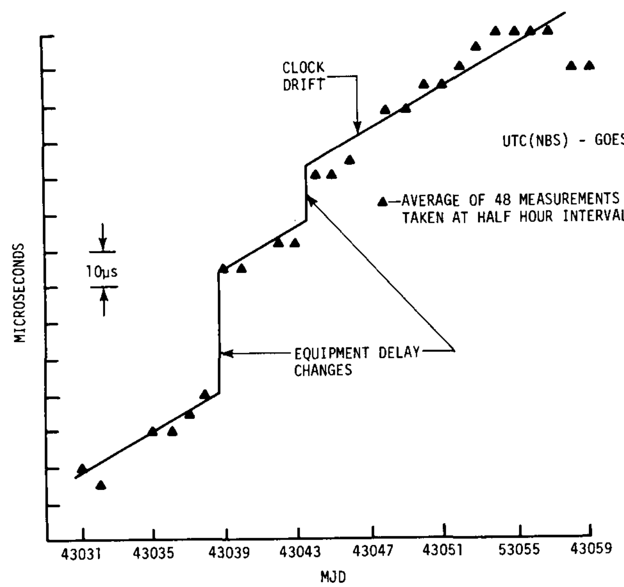

FIGURE 30. UTC(NBS) - GOES1/NBS (UNCORRECTED)

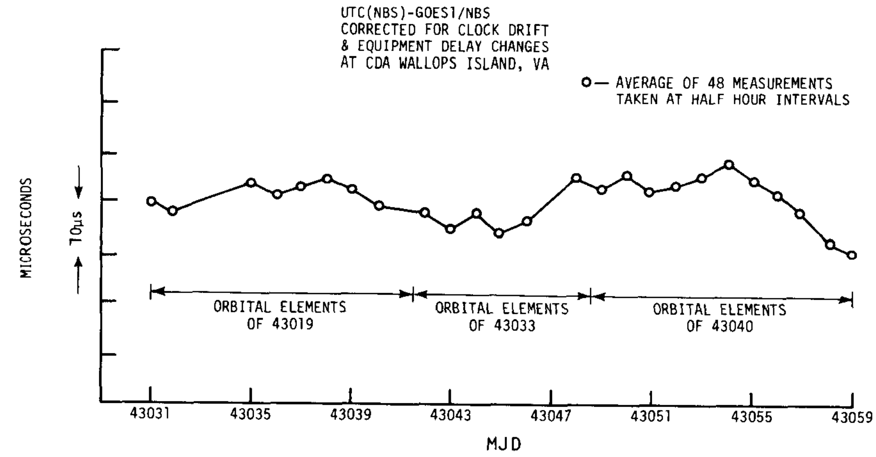

FIGURE 31. UTC(NBS) - GOES1/NBS (CORRECTED)

The results indicate a consistency in orbit determination and in the stability of equipment delays of about 10 μs for the period under study. A claim for accuracy cannot be made, however, until the equipment delays at the CDA and in the receiving equipment have been evaluated and more measurements of this type are taken at points separated by large geographical distances.

Portions of the actual charts producing the data just discussed are illustrated in figure 32. The output, uncorrected for the free-space delay, shows a 24-hour diurnal due to the satellite's orbit inclination and eccentricity. The corrected output, one point every half hour, lies in a straight line at least to a few microseconds on the average. Because the satellite-position data are updated only every half hour, the corrected output deviates from a straight line between the half-hour updates at the same rate shown for the uncorrected output.

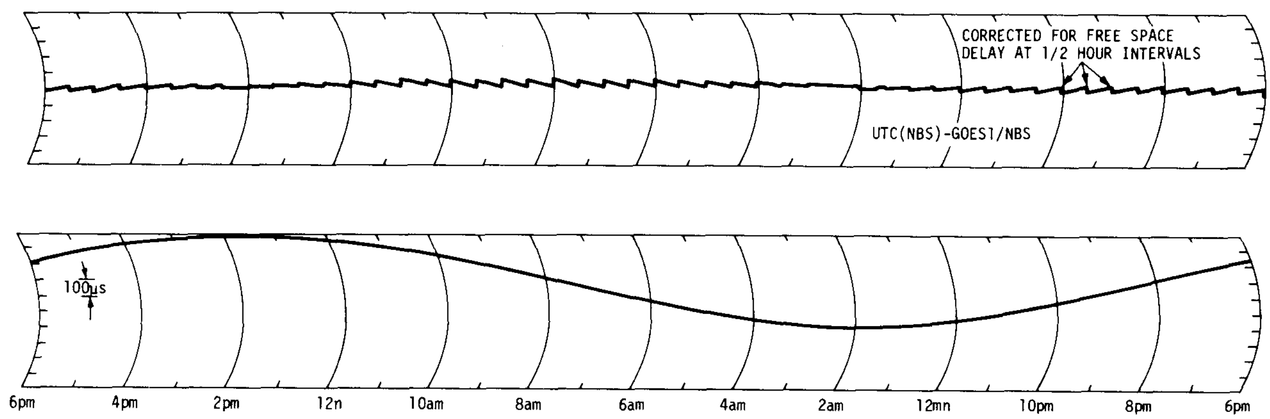

FIGURE 32. SATELLITE OUTPUT: CORRECTED AND UNCORRECTED

10. CONCLUSIONS

The time code has been broadcast from the two GOES satellites for more than one year. It has proven itself to be a reliable, low cost, and extremely simple system for moderately high-accuracy time. The time code is now considered a permanent feature of the GOES satellites and should see an expanding list of users for many purposes within the Western Hemisphere.

The results presented here indicate a potential accuracy of 10 to 20 microseconds. These figures need to be verified, however, by additional observations at widely separated geographical points. Equipment delays need further study. The clock drift and the effect of equipment changes at the CDA need to be offset or eliminated to make the time-code system a true one-way time transfer technique.

NBS plans to continue work toward the development of methods to increase the accuracy of the satellite time dissemination system. A more accurate satellite ephemeris generator has replaced an earlier one. Methods to provide the user with more accurate satellite position information over smaller time increments or on a continuous basis will be investigated.

11. REFERENCES

[1]. Davis, D. D., A microprocessor data logging system for utilizing TV as a time/frequency transfer standard, (Proc. 8th Annual Precise Time and Time Interval (PTTI) Applications and Planning Meeting, Goddard Space Flight Center, Greenbelt, MD., Nov. 30 - Dec. 2, 1976, pp. 167-181).

[2]. Cateora, J. V., Davis, D. D., and Hanson, D. W., A Satellite-Controlled Digital Clock, Nat. Bur. Stand. (U.S.), Tech. Note 681, 41 pages, (June 1976).

[3]. Hamilton, W. F., and Hanson, D. W., A Synchronous Satellite Time Delay Computer, Nat. Bur. Stand. (U.S.), Tech. Note 638, 30 pages, (July 1973).

[4]. Lewis, E. A., Parametric Formulas for Geodesic Curves and Distances on a Slightly Oblate Earth, Air Force Cambridge Research Laboratory Report, pp. 63-495, (April 1963).

[5]. Hanson, D. W. and Hamilton, W. F., Experimental Time and Frequency Broadcasts from the ATS-3 Satellite, Nat. Bur. Stand. (U.S.), Tech. Note 645, 107 pages, (Nov. 1973).

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ROM      INSTRUCTION
ADDRESS
                        MNEMONIC                 COMMENTS

0 00                                    NBS DELAY MICROPROCESSOR/CALCULATOR - THIS
0 01 51             JMS -               4004 PROGRAM COMPUTES THE LINE OF SIGHT
0 02 80             -    TPOS           RADIO PATH DELAY BETWEEN ANY TWO POINTS ON
0 03                                    EARTH VIA A SYNCHRONOUS SATELLITE --- ALL
0 04   MATHEMATICAL FUNCTIONS ARE PERFORMED BY A MOS TECHNOLOGY INC. MPS 7529-
0 05   103 LSI SCIENTIFIC CALCULATOR ARRAY INTERFACED TO THE MICROPROCESSOR.
0 06   THE SATELLITE POSITION DATA IS PROVIDED BY THE SATELLITE CONTROLLED
0 07   DIGITAL CLOCK ALSO INTERFACED TO THE MICROPROCESSOR.  THE RECEIVER
0 08   POSITION IS ENTERED VIA THUMBWHEEL SWITCHES AND THE TRANSMITTER POSITION
0 09   IS WRITTEN INTO THE MICROPROCESSOR PROGRAM.  THE OUTPUT CONTROLS THE
0 0A   DELAY OF A 1 HZ PULSE THROUGH A PROGRAMMABLE DELAY GENERATOR AND IS ALSO
0 0B   DISPLAYED ON LEDS.  THE 1 PPS IS PROVIDED BY THE SATELLITE
0 0C   CONTROLLED DIGITAL CLOCK.                          J.V.CATEORA SEPT. 1976
0 0D
0 0E 51 START       JMS -               EXTRACT 12 DIGIT RESULT FROM MATH CHIP
0 0F A0              -   EXTRACT12
0 10 50             JMS -               TEST RESULT FROM MATH CHIP FOR
0 11 F0              -   TEST5          TRAILING ZEROS WHICH WILL CAUSE A DISPLACE-
0 12 14             JCN A0              MENT OF THE DECIMAL POINT
0 13 1A              -   SKIP.01
0 14 53             JMS -               IF DISPLACEMENT IS DETECTED ADD .01 AND
0 15 E0              -   KCPROM         EXTRACT NEW RESULT --- ELSE SKIP AND LEAVE
0 16 51             JMS -               THE RESULT ALONE
0 17 A0              -   EXTRACT12
0 18
0 19
0 1A 51 SKIP.01     JMS -               DISPLAY RESULTS STORED IN RAM
0 1B C8             -    DISPLAYRAM
0 1C 20 CALCULATE   FIM P0              ADDRESS OF FIRST KEY CODE TO BE EXECUTED
0 1D                0    0
0 1E 28             FIM P4              ADDRESS OF  LAST KEY CODE TO BE EXECUTED +1
0 1F 02             0    2
0 20 53             JMS -                                              EXECUTE CA/CE
0 21 E0             -    KCPROM                                                CA/CE
0 22 52             JMS -               WRITE SATELLITE POSITION IN RAM
0 23 80             -    SPOS
0 24 28             FIM P4              FIRST CHARACTER IN RAM TO BE EXECUTED
0 25 20             2    0
0 26 2A             FIM P4              F-NUMBER OF RAM CHARS+1 TO BE ENTERED INTO
0 27 A0             A    0              MATH CHIP, THAT IS F-6+1=A
0 28 51             JMS -
0 29 00             -    KCRAM          ENTER LONGITUDE OF SAT. INTO MATH CHIP
0 2A 20             FIM P0
0 2B 02             0    2
0 2C 28             FIM P4
0 2D 03             0    3
0 2E 53             JMS -                                              EXECUTE -
0 2F E0             -    KCPROM
0 30
0 31
0 32 52             JMS -               WRITE RECEIVER POSITION INTO RAM
0 33 20             -    RPOS
0 34
0 35
0 36 52             JMS -
0 37 0F             -    ODD/EV         TEST NUMBER OF PASSES THRU PROGRAM (STATUS
0 38 D3             LDM 3               CHARACTER) FOR ODD OR EVEN ---
0 39 B9             XCH R9              IF  ODD ENTER LONGITUDE OF RECEIVER
0 3A 2A             FIM P5              IF EVEN ENTER LONGITUDE OF TRANSMITTER
0 3B 90             9    0              INTO MATH CHIP
0 3C 51             JMS -
0 3D                -    KCRAM          ENTER LONGITUDE OF TRANSMITTER OR RECEIVER
0 3E                                    INTO MATH CHIP
0 3F
```

```
0 40 20          FIM P0
0 41 03          0   3
0 42 28          FIM P4
0 43 05          0   5
0 44 53          JMS -                                                     EXECUTE =
0 45 E0          -   KCPROM                                                        STO
0 46
0 47
0 48 52          JMS -          TEST NUMBER OF PASSES THRU PROGRAM (STATUS
0 49 0F          -   ODD/EV     CHARACTER) FOR ODD OR EVEN ---
0 4A 0A          LD  RA
0 4B B9          XCH R9         IF EVEN ENTER TRANSMITTER LATITUDE
0 4C 2A          FIM P5
0 4D A0          A   0
0 4E 51          JMS -          ENTER  LATITUDE OF TRANSMITTER OR RECEIVER
0 4F             -   KCRAM      INTO MATH CHIP
0 50
0 51
0 52 20          FIM P0
0 53 05          0   5
0 54 28          FIM P4                                                    EXECUTE COS
0 55 08          0   8                                                             X
0 56 53          JMS -                                                             (
0 57 E0          -   KCPROM
0 58 28          FIM P4
0 59 26          2   6
0 5A 2A          FIM P5
0 5B B0          B   0
0 5C 51          JMS -          ENTER LATITUDE OF SATELLITE INTO MATH CHIP
0 5D             -   KCRAM
0 5E
0 5F
0 60 20          FIM P0                                             EXECUTE COS )
0 61 08          0   8                                                      X    =
0 62 28          FIM P4                                                     (    STO
0 63 11          1   1                                                      RCL
0 64 53          JMS -                                                      COS
0 65 E0          -   KCPROM                                                 )
0 66
0 67
0 68 52          JMS -          TEST NUMBER OF PASSES THRU PROGRAM (STATUS
0 69 0F          -   ODD/EV     CHARACTER) FOR ODD OR EVEN ---
0 6A 0A          LDM A          IF  ODD ENTER RECEIVER    LATITUDE
0 6B B9          XCH R9         IF EVEN ENTER TRANSMITTER LATITUDE
0 6C 2A          FIM P5
0 6D A0          A   0
0 6E 51          JMS -          ENTER  LATITUDE OF TRANSMITTER OR RECEIVER
0 6F             -   KCRAM      INTO MATH CHIP
0 70
0 71
0 72 20          FIM P0
0 73 11          1   1
0 74 28          FIM P4
0 75 13          1   3
0 76 53          JMS -                                                     EXECUTE SIN
0 77 E0          -   KCPROM                                                        X
0 78 28          FIM P4
0 79 26          2   6
0 7A 2A          FIM P5
0 7B B0          B   0
0 7C 51          JMS -          ENTER LATITUDE OF SATELLITE INTO MATH CHIP
0 7D             -   KCRAM
0 7E
0 7F
```

```
0 80 20          FIM P0                          EXECUTE SIN 5    7   +    3   SQRT
0 81 13          1   3                                   =   .    CHS 2    9   +
0 82 28          FIM P4                                  +   9    EE  0    6
0 83 33          3   3                                   RCL 8    9   .    EE
0 84 53          JMS -                                   =   1    X   2    9
0 85 E0          -   KCPROM                              STO 4    RCL 1    =
0 86 28          FIM P4                                           (32 KEY CODES)
0 87 2B          2   B
0 88 2A          FIM P5
0 89 B0          B   0
0 8A 51          JMS -
0 8B             -   KCRAM        ENTER NORMALIZED RANGE OF SATELLITE INTO
0 8C 20          FIM P0           MATH CHIP
0 8D 33          3   3
0 8E 28          FIM P4
0 8F 34          3   4
0 90 53          JMS -                                            EXECUTE =
0 91 E0          -   KCPROM
0 92 52          JMS -            INCREMENT RAM0/REG0 STATUS CHARACTER EACH
0 93 08          -   INCREMENT    PASS THROUGH PROGRAM
0 94 52          JMS -
0 95 0F          -   ODD/EV       TEST NUMBER OF PASSES THRU PROGRAM (STATUS
0 96 F0          CLB              CHARACTER) FOR ODD OR EVEN ---
0 97 D1          LDM 1            IF  ODD, R8 = 1  UP DELAY COMPUTED GO BACK
0 98 98          SUB R8           TO START AND COMPUTE DOWN DELAY
0 99 14          JCN A0           IF EVEN, R8 = 3 BOTH DELAYS HAVE BEEN
0 9A 0E          -   START        COMPUTED --- CONTINUE ON
0 9B 20          FIM P0
0 9C 34          3   4
0 9D 28          FIM P4
0 9E 35          3   5
0 9F 53          JMS -                                            EXECUTE +
0 A0 E0          -   KCPROM
0 A1 28          FIM P4
0 A2 04          0   4
0 A3 2A          FIM P5
0 A4 90          9   0
0 A5 51          JMS -            ENTER TOTAL UP DELAY INTO MATH CHIP
0 A6             -   KCRAM
0 A7 20          FIM P0
0 A8 35          3   5
0 A9 28          FIM P4
0 AA 36          3   6
0 AB 53          JMS -                                            EXECUTE =
0 AC E0          -   KCPROM
0 AD 51          JMS -            EXTRACT TOTAL UP DELAY + TOTAL DOWN DELAY
0 AE A0          -   EXTRACT12    FROM MATH CHIP
0 AF
0 B0 50          JMS -
0 B1 F0          -   TEST5
0 B2 14          JCN A0
0 B3 C0          -   SKIP.01      TEST FOR TRAILING ZEROS AND ADJUST IF
0 B4 53          JMS -            NECESSARY
0 B5 E0          -   KCPROM
0 B6 51          JMS -
0 B7 A0          -   EXTRACT12
0 B8
0 B9
0 BA
0 BB
0 BC
0 BD
0 BE
0 BF
```

```
0 C0 51 SKIP.01     JMS -               DISPLAY TOTAL UP + DOWN DELAY
0 C1 C8             -   DISPLAYRAM
0 C2 20             FIM P0                        EXECUTE CHS 0    .    +    0
0 C3 38             3   8               DELAY               +    0    0    1    .
0 C4 28             FIM P4              GENERATOR           3    .    2    0    =
0 C5 56             5   6               SETTING             0    =    4    0
0 C6 53             JMS -                                   0    X    =    0
0 C7 E0             -   KCPROM                              0    1    CHS  0
0 C8 51             JMS -
0 C9 A0             -   EXTRACT12       EXTRACT DELAY GENERATOR SETTING
0 CA 22             FIM P1
0 CB 05             0   5               READ RAM0/REG0/CHARACTER 5 INTO R2 TO TEST
0 CC 23             SRC P1              FOR BLANK
0 CD E9             RDM
0 CE B2             XCH R2
0 CF D0             LDM 0
0 D0 F1             CLC                 IF RAM CHAR IS NOT = 0 (BLANK) SKIP
0 D1 92             SUB R2
0 D2 1C             JCN A1
0 D3 DC             -   SKIP.001
0 D4 20             FIM P0
0 D5 56             5   6               IF RAM CHARACTER = 0 ADD .001 TO PREVENT
0 D6 28             FIM P4              TRAILING ZEROS FROM CAUSING A DECIMAL POINT
0 D7 5C             5   C               SHIFT
0 D8 53             JMS -
0 D9 E0             -   KCPROM
0 DA 51             JMS -               EXTRACT NEW RESULT
0 DB A0             -   EXTRACT12
0 DC 52 SKIP.001    JMS -               OUTPUT DELAY GENERATOR SETTING
0 DD 70             -   DELAYGEN
0 DE 40             JUN -
0 DF 1C             -   CALCULATE
0 E0
0 E1
0 E2
0 E3
0 E4
0 E5
0 E6
0 E7
0 E8
0 E9
0 EA
0 EB
0 EC
0 ED
0 EE
0 EF
0 F0 22 TEST5       FIM P1              TEST5 TESTS FOR MATH CHIP OUTPUT DIGIT
0 F1 05             0   5               NUMBER 5 BLANK
0 F2 23             SRC P1
0 F3 E9             RDM                 READ RAM0/REG0/CHARACTER 5 INTO R2 TO TEST
0 F4 B2             XCH R2              FOR BLANK
0 F5 D0             LDM 0
0 F6 F1             CLC
0 F7 92             SUB R2              IF RAM CHARACTER IS NOT = 0 (BLANK) SKIP
0 F8 1C             JCN A1
0 F9 FF             -   SKIP.01
0 FA 20             FIM P0              SET UP TO CALL KCPROM TO ADD .01 ---
0 FB 36             3   6               HOWEVER MAIN PROGRAM MUST MAKE THE CALL OR
0 FC 28             FIM P4              ELSE THE LIMIT OF 3 LEVELS OF SUBROUTINES
0 FD 38             3   8               WOULD BE EXCEEDED IF KCPROM WERE CALLED
0 FE C1             BBL                 FROM HERE. IF RAM CHAR     = BLANK RETURN 1
0 FF C0 SKIP.01     BBL                            IF RAM CHAR NOT = BLANK RETURN 0
```

```
1 00 20 KCRAM       FIM P0          FIRST KEY CODE ADDRESS FOR FIN INSTRUCTION
1 01 10             1   0
1 02 22             FIM P1          TO SELECT I/O PORTS NUMBER 0
1 03                0   0
1 04 24             FIM P2          TO SELECT I/O PORTS NUMBER 3
1 05 30             3   0
1 06 29 ENCODE      SRC P4          P0 CONTAINS ADDRESS OF KEY CODE
1 07 E9             RDM
1 08 B1             XCH R1
1 09 36             FIN P3          PUT KEY CODE INTO P3
1 0A 51             JMS -           WRITE NOP AND KEY CODE TO MATH CHIP, WAIT
1 0B 20             -   INPUTKC     FOR DONE
1 0C 69             INC R9          INCREMENT RAM CHARACTER ADDRESS IN R9
1 0D 7A             ISZ RA          INCREMENT NUMBER OF RAM CHARS COUNTER RA
1 0E 06             -   ENCODE
1 0F C0             BBL             RETURN TO MAIN PROGRAM
1 10 11 ZERO
1 11 12 ONE                         KCRAM READS SPECIFIED BCD CHARACTERS FROM
1 12 13 TWO                         RAM AND ENCODES THEM INTO KEY CODES ---
1 13 14 THREE                       THEN CALLS INPUTKC TO INPUT THEM TO MATH
1 14 15 FOUR                        CHIP
1 15 16 FIVE
1 16 17 SIX
1 17 18 SEVEN
1 18 19 EIGHT
1 19 1A NINE
1 1A 21 DEC.PT.                     BCD CHARACTER A INTERPRETED AS DECIMAL PT.
1 1B 2B CHS                         BCD CHARACTER B INTERPRETED AS CHS KEY
1 1C
1 1D
1 1E
1 1F
1 20 00 INPUTKC     LDM 0           INPUTKC INPUTS KEY STROKE CODES AND DATA
1 21 23             SRC P1          TO MATH CHIP ALONG WITH NOP AND WAITS FOR
1 22 F4             CMA             DONE  --- NOP KEY CODE = 00
1 23 E2             WRR
1 24 25             SRC P2
1 25 F4             CMA
1 26 E2             WRR
1 27 51             JMS -           WAIT 40 MILLISECONDS
1 28 F2             -   DELAY40
1 29 A7             LD  R7          R7 CONTAINS LEAST SIGNIFIGANT PART OF KEY
1 2A 23             SRC P1          CODE --- OUTPUT IT TO OUTPORT NUMBER 0
1 2B F4             CMA
1 2C E2             WRR
1 2D A6             LD  R6          R6 CONTAINS MOST  SIGNIFIGANT PART OF KEY
1 2E 25             SRC P2          CODE --- OUTPUT IT TO OUTPORT NUMBER 3
1 2F F4             CMA
1 30 E2             WRR
1 31 51             JMS -           WAIT 40 MILLISECONDS
1 32 F2             -   DELAY40
1 33 D6             LDM 6           WRITE OUT 89 FOR DONE TEST  (NEG. LOGIC 76)
1 34 23             SRC P1
1 35 E2             WRR             WRITE 9 TO OUTPORT NUMBER 0 (NEG. LOGIC 6)
1 36 D7             LDM 7
1 37 25             SRC P2          WRITE 8 TO OUTPORT NUMBER 3 (NEG. LOGIC 7)
1 38 E2             WRR
1 39 F0 DONETEST    CLB
1 3A EA             RDR             INPORT NUMBER 3 STILL SELECTED --- READ IT
1 3B F6             RAR
1 3C F6             RAR             ROTATE DECIMAL POINT LED SEGMENT INTO CARRY
1 3D 1A             JCN C0          POSITION TO TEST FOR DONE
1 3E 39             -   DONETEST
1 3F C0 DONE        BBL             IF DONE RETURN TO KCPROM OR KCRAM
```

```
1 40 00 BLANK                      DECODE CONVERTS FROM 7 SEGMENT LED CODE TO
1 41                               BCD AND WRITES BCD INTO RAM0/REG0/CHARS 4
1 42 10 ONE                        THRU F (THIS ROUTINE MUST BE LOCATED AT
1 43 70 SEVEN                      ADDRESSES 40 THRU 7F IN A PROM -- BECAUSE
1 44                               THE SEGMENT CODES ARE THE ADDRESSES)
1 45 3A DECODE       FIN P5
1 46 29              SRC P4        USING SEGMENT CODE IN P0 AS ADDRESS FETCH
1 47 AA              LD  RA        INDIRECT BCD CHARACTER INTO RA OF P5
1 48 E0              WRM           WRITE BCD CHARACTER INTO RAM
1 49 69              INC R9        INCREMENT RAM CHARACTER ADDRESS
1 4A C5              BBL           RETURN TO EXTRACT12
1 4B
1 4C
1 4D E0 +OVERFLOW
1 4E
1 4F    ZERO
1 50 80 MINUS                      NOTE THAT IT IS ONLY NECESSARY TO USE 5 OF
1 51                               THE 7 SEGMENTS TO DECODE INTO BCD
1 52
1 53 30 THREE
1 54
1 55
1 56
1 57 20 TWO
1 58
1 59 50 FIVE
1 5A 40 FOUR
1 5B 90 NINE
1 5C 60 SIX
1 5D F0 -OVERFLOW
1 5E
1 5F 80 EIGHT
1 60 00 BLANK.
1 61
1 62 10 ONE.
1 63 70 SEVEN.
1 64 A4 WRAM         LD  R4        WRAM IS CALLED BY SUBROUTINES TPOS AND RPOS
1 65 23              SRC P1        TO WRITE TWO BCD CHARACTERS CONTAINED IN R4
1 66 E0              WRM           AND R5 INTO RAM AND IS IMBEDDED INTO
1 67 63              INC R3        SUBROUTINE DECODE ONLY TO MAKE USE OF BLANK
1 68 A5              LD  R5        SPACES THAT ARE IN DECODE BY NECESSITY
1 69 23              SRC P1
1 6A E0              WRM
1 6B 63              INC R3
1 6C C0              BBL           RETURN TO TPOS OR RPOS
1 6D E0 +OVERFLOW.
1 6E
1 6F    ZERO.
1 70 80 MINUS.
1 71
1 72
1 73 30 THREE.
1 74
1 75
1 76
1 77 20 TWO.
1 78
1 79 50 FIVE.
1 7A 40 FOUR.
1 7B 90 NINE.
1 7C 60 SIX.
1 7D F0 -OVERFLOW.
1 7E
1 7F 80 EIGHT.
```

```
1 80 22 TPOS      FIM P1        TPOS WRITES POSITION OF TRANSMITTER INTO
1 81 33           3   3         RAM --- IN THIS CASE WALLOPS ISLAND, VA.
1 82                            LONGITUDE = 75.46, LATITUDE = 37.85
1 83 24           FIM P2
1 84 07           0   7
1 85 51           JMS -
1 86 64           -   WRAM      WRITE 07 INTO RAM
1 87 24           FIM P2
1 88 5A           5   A
1 89 51           JMS -
1 8A 64           -   WRAM      WRITE 5. INTO RAM
1 8B 24           FIM P2
1 8C 46           4   6
1 8D 51           JMS -
1 8E 64           -   WRAM      WRITE 46 INTO RAM
1 8F 24           FIM P2
1 90 03           0   3
1 91 51           JMS -
1 92 64           -   WRAM      WRITE 03 INTO RAM
1 93 24           FIM P2
1 94 7A           7   A
1 95 51           JMS -
1 96 64           -   WRAM      WRITE 7. INTO RAM
1 97 24           FIM P2
1 98 85           8   5
1 99 51           JMS -
1 9A 64           -   WRAM      WRITE 85 INTO RAM
1 9B 24           FIM P2
1 9C              0   0
1 9D 51           JMS -
1 9E 64           -   WRAM      WRITE 00 INTO RAM
1 9F C0           BBL           RETURN TO MAIN PROGRAM
1 A0 22 EXTRACT12 FIM P1        EXTRACT12 EXTRACTS THE 12 DIGIT RESULT FROM
1 A1 04           0   4         THE MATH CHIP, DECODES IT AND STORES BCD
1 A2 24           FIM P2        CHARACTER IN RAM0/REG0
1 A3 30           3   0
1 A4 26           FIM P3        DIGIT DATA REQUEST CODES 81, 82, 83, ETC.
1 A5 81           8   1
1 A6 28           FIM P4        TO SELECT RAM0/REG0/CHARS4 THRU F FOR BCD
1 A7 04           0   4         STORAGE
1 A8 23 NEXTDIGIT SRC P1
1 A9 A7           LD  R7        WRITE OUT DIGIT REQUEST CODES
1 AA F4           CMA
1 AB E2           WRR
1 AC 25           SRC P2        L.S.P. OF DIGIT REQUEST CODE TO OUTPORT 0
1 AD A6           LD  R6        M.S.P. OF DIGIT REQUEST CODE TO OUTPORT 3
1 AE F4           CMA
1 AF E2           WRR
1 B0 F0 TESTDIGIT CLB
1 B1 EA           RDR           I/O PORTS 3 STILL SELECTED --- READ INPORT
1 B2 F4           CMA           NUMBER 3
1 B3 F5           RAL           IF 8 BIT IS POSITIVE (NEG. LOGIC 0) DIGIT
1 B4 1A           JCN C0        IS AVAILABLE --- IF NOT CONTINUE TESTING
1 B5 B0           -   TESTDIGIT
1 B6 EA           RDR           I/O PORTS 3 STILL SELECTED --- READ M.S.P.
1 B7 B0           XCH R0        OF SEGMENT CODE FROM INPORT 3 AND STORE IT
1 B8 23           SRC P1        IN R0
1 B9 EA           RDR           READ L.S.P. OF SEGMENT CODE FROM INPORT 0
1 BA B1           XCH R1        AND STORE IT IN R1
1 BB 51           JMS -         DECODE SEGMENT CODE AND STORE BCD CHARACTER
1 BC 45           -   DECODE    IN RAM
1 BD 67           INC R7        INCREMENT L.S.P. OF DIGIT REQUEST CODE
1 BE 73           ISZ R3
1 BF A8           -   NEXTDIGIT IF ALL 12 CODES HAVE BEEN SENT
```

```
1 C0 C0              BBL                    RETURN TO MAIN PROGRAM
1 C1
1 C2
1 C3
1 C4
1 C5
1 C6
1 C7
1 C8 22 DISPLAYRAM FIM P1                   DISPLAYRAM DISPLAYS MATH CHIP OUTPUT ON
1 C9 10              1   0                  LEDS. OUTPUT IS STORED IN RAM0/REG0/CHARS
1 CA 24              FIM P2                 4 THROUGH F
1 CB 20              2   0                  TO SELECT OUTPORT NO. 2 FOR STROBE OUTPUT
1 CC 26              FIM P3                 INITIALIZE STROBE TO ZERO
1 CD                 0   0
1 CE 28              FIM P4                 TO SELECT RAM0/REG0/CHARACTERS 4 THRU F
1 CF 04              0   4
1 D0 25 RRAM         SRC P2                 WRITE STROBE TO OUTPORT 2 --- STROBE IS
1 D1 A7              LD  R7                 OUTPUT BEFORE DATA BECAUSE OF LATCHED
1 D2 F4              CMA                    MICROPROCESSOR OUTPUT PORTS --- PREVENTS
1 D3 E2              WRR                    CHARACTERS FROM BEING SHIFTED ON DISPLAY
1 D4 29              SRC P4                 LEDS
1 D5 E9              RDM
1 D6 23              SRC P1
1 D7 F4              CMA
1 D8 E2              WRR                    SELECT, READ, WRITE RAM CHAR TO OUTPORT 1
1 D9 67              INC R7                 INCREMENT STROBE
1 DA 79              ISZ R9
1 DB D0              -   RRAM               INCREMENT RAM CHARACTER ADDRESS
1 DC C0              BBL                    RETURN TO MAIN PROGRAM
1 DD
1 DE
1 DF
1 E0 AA TESTN/S      LD  RA                 TESTN/S TESTS NORTH/SOUTH LATITUDE SWITCH
1 E1 F5              RAL                    WHICH IS CONNECTED TO LONGITUDE 100S
1 E2 12              JCN C1                 POSITION 8 BIT.  IF = 0 LATITUDE IS NORTH
1 E3 E9              -   SOUTH                               IF = 1 LATITUDE IS SOUTH
1 E4 2A NORTH        FIM P5                 SET RB, LATITUDE CHS CHAR. = 0 FOR NORTH
1 E5                 0   0
1 E6 F6              RAR                    SHIFT LONG. 100S CHAR. BACK TO NORMAL AND
1 E7 BA              XCH RA                 STORE BACK INTO RA
1 E8 C0              BBL                    RETURN TO RPOS
1 E9 2A SOUTH        FIM P5                 SET RB, LATITUDE CHS CHAR. = B FOR SOUTH
1 EA 0B              0   B
1 EB F1              CLC                    CLEAR SOUTH LATITUDE INDICATION
1 EC F6              RAR                    SHIFT LONG. 100S CHAR. BACK TO NORMAL AND
1 ED BA              XCH RA                 STORE BACK INTO RA
1 EE C0              BBL                    RETURN TO RPOS
1 EF
1 F0
1 F1
1 F2 2C DELAY40      FIM P6                 DELAY40 PROVIDES THE 40 MILLISECONDS
1 F3                 0   0                  DELAY REQUIRED BETWEEN ENTRIES OF KEY
1 F4 2E              FIM P7                 STROKE CODES INTO MATH CHIP
1 F5 A0              A   0
1 F6 7C FIRST        ISZ RC
1 F7 F6              -   FIRST
1 F8 7D              ISZ RD
1 F9 F6              -   FIRST
1 FA 7E              ISZ RE
1 FB F6              -   FIRST
1 FC C4              BBL                    RETURN TO INPUTKC
1 FD
1 FE
1 FF
```

```
2 00                                  INCREMENT INCREMENTS THE NUMBER STORED IN
2 01                                  RAM0/REG0 STATUS CHARACTER WHICH RECORDS
2 02                                  NUMBER OF PASSES THRU PROGRAM --- ODD OR
2 03                                  EVEN PASSES DETERMINE WHETHER TRANSMITTER
2 04                                  OR RECEIVER POSITION WILL BE USED IN THE
2 05                                  DELAY CALCULATION
2 06
2 07
2 08 28 INCREMENT   FIM P4
2 09                0   0             READ STATUS CHARACTER INTO ACCUMULATOR
2 0A 29             SRC P4
2 0B EC             RD0
2 0C F2             IAC               INCREMENT ACCUMULATOR
2 0D E4             WR0               WRITE ACCUMULATOR BACK INTO STATUS CHAR
2 0E C0             BBL               RETURN TO MAIN PROGRAM
2 0F 28 ODD/EV      FIM P4
2 10                0   0             READ STATUS CHARACTER INTO ACCUMULATOR
2 11 29             SRC P4
2 12 EC             RD0
2 13 F6             RAR
2 14 1A             JCN C0            TEST IF NUMBER IN STATUS CHARACTER IS ODD
2 15 1A             -   EVEN          OR EVEN
2 16 F5 ODD         RAL
2 17 D1             LDM 1             IF  ODD SET R8 =1 CAUSES USE OF RECEIVER
2 18 B8             XCH R8            POSITION DATA STORED IN RAM
2 19 C0             BBL               RETURN TO MAIN PROGRAM
2 1A F5 EVEN        RAL
2 1B D3             LDM 3             IF EVEN SET R8 =3 CAUSES USE OF TRANSMITTER
2 1C B8             XCH R8            POSITION DATA STORED IN RAM
2 1D C0             BBL               RETURN TO MAIN PROGRAM
2 1E
2 1F
2 20 22 RPOS        FIM P1            RPOS WRITES RECEIVER POSITION INTO RAM0/
2 21 13             1   3             REG1/CHARACTERS 3 THRU F AFTER READING IT
2 22 26             FIM P3            FROM THUMBWHEEL SWITCHES
2 23 01             0   1             TO SELECT RAM0 OUTPUT PORT --- R7 = STROBE
2 24 28             FIM P4
2 25 10             1   0             TO SELECT INPORT 1 (LONG/LAT DATA)
2 26 52             JMS -
2 27 67             -   READL/L
0 28 51             JMS -             TEST LONGITUDE 100S CHARACTER 8 BIT FOR 0
0 29 E0             -   TESTN/S       OR 1 FOR NORTH OR SOUTH LATITUDE
2 2A AA             LD  RA
2 2B B4             XCH R4            READ 2 RECEIVER LONG/LAT SWITCHES AND STORE
2 2C 52             JMS -             2 POSITION CHARACTERS IN RAM
2 2D 67             -   READL/L
2 2E AA             LD  RA
2 2F B5             XCH R5
2 30 51             JMS -
2 31 64             -   WRAM
2 32 52             JMS -
2 33 67             -   READL/L
2 34 AA             LD  RA            STORE 1 POSITION CHARACTER + DECIMAL POINT
2 35 B4             XCH R4            IN RAM
2 36 DA             LDM A
2 37 B5             XCH R5
2 38 51             JMS -
2 39 64             -   WRAM
2 3A 52             JMS -
2 3B 67             -   READL/L
2 3C AA             LD  RA            STORE 2 POSITION CHARACTERS IN RAM
2 3D B4             XCH R4
2 3E 52             JMS -
2 3F 67             -   READL/L
```

```
2 40 AA             LD   RA
2 41 B5             XCH  R5
2 42 51             JMS  -
2 43 64             -    WRAM
2 44 D0             LDM  0
2 45 B4             XCH  R4
2 46 52             JMS  -
2 47 67             -    READL/L       STORE CHS + 1 POSITION CHARACTER IN RAM
2 48 AA             LD   RA
2 49 B5             XCH  R5
2 4A 51             JMS  -
2 4B 64             -    WRAM
2 4C 52             JMS  -
2 4D 67             -    READL/L
2 4E AA             LD   RA            STORE 1 POSITION CHARACTER + DECIMAL POINT
2 4F B4             XCH  R4            IN RAM
2 50 DA             LDM  A
2 51 B5             XCH  R5
2 52 51             JMS  -
2 53 64             -    WRAM
2 54 52             JMS  -
2 55 67             -    READL/L
2 56 AA             LD   RA
2 57 B4             XCH  R4            STORE 2 POSITION CHARACTERS IN RAM
2 58 52             JMS  -
2 59 67             -    READL/L
2 5A AA             LD   RA
2 5B B5             XCH  R5
2 5C 51             JMS  -
2 5D 64             -    WRAM
2 5E AB             LD   RB            STORE LATITUDE CHS CHARACTER, WHICH WAS
2 5F B4             XCH  R4            SAVED IN RB BY ROUTINE TESTN/S, IN RAM
2 60 D0             LDM  0
2 61 B5             XCH  R5
2 62 51             JMS  -
2 63 64             -    WRAM
2 64 C0             BBL                RETURN TO MAIN PROGRAM
2 65
2 66
2 67 27 READL/L     SRC  P3            READL/L WRITES STROBE TO RECEIVER LONGITUDE
2 68 A7             LD   R7            LATITUDE THUMBWHEEL SWITCHES VIA RAM0
2 69 F4             CMA                OUTPORT AND READS IN POSITION
2 6A E1             WMP
2 6B 29             SRC  P4            READ LONG/LAT CHARACTER FROM INPORT 1
2 6C EA             RDR
2 6D BA             XCH  RA            TRANSFER LONG/LAT CHAR TO RPOS VIA RA
2 6E 67             INC  R7            INCREMENT STROBE
2 6F C0             BBL                RETURN TO RPOS
2 70 22 DELAYGEN    FIM  P1            DELAYGEN OUTPUTS 4 CHARACTER DELAY
2 71 05             0    5             GENERATOR SETTING TO DELAY GENERATOR
2 72 24             FIM  P2            TO SELECT OUTPORT 4 AND SET UP 4 CHARACTER
2 73 4C             4    C             COUNTER
2 74 23 NEXTCHAR    SRC  P1            READ RAM CHARACTER
2 75 E9             RDM
2 76 25             SRC  P2
2 77 F4             CMA                WRITE CHARACTER TO OUTPORT 4
2 78 E2             WRR
2 79 63             INC  R3            INCREMENT RAM CHARACTER ADDRESS
2 7A 64             INC  R4            INCREMENT NUMBER OF OUTPORT
2 7B 75             ISZ  R5            INCREMENT RAM CHARACTER COUNTER
2 7C 74             -    NEXTCHAR
2 7D C0             BBL                RETURN TO RPOS
2 7E
2 7F
```

```
2 80 22 SPOS         FIM P1           SPOS READS SATELLITE POSITION INFORMATION
2 81 20              2   0            FROM DECODER MICROPROCESSOR AND STORES IT
2 82 24              FIM P2           IN RAM0/REG1 TEMPORARILY THEN LATER
2 83 43              4   3            TRANSFERS IT TO REG2
2 84 26              FIM P3
2 85 13              1   3            TO SELECT RAM0/REG1/CHARACTERS 3 THRU F
2 86 25 READS        SRC P2
2 87 EA READS+1      RDR              TEST DECODER MICROPROCESSOR RAM OUTPUT PORT
2 88 F1              CLC              FOR 3 --- IF NOT FOUND KEEP TESTING --- IF
2 89 95              SUB R5           FOUND READ DECODER OUTPORT 1 CONNECTED TO
2 8A 1C              JCN A1           DELAY MICROPROCESSOR INPORT 2
2 8B 87              -   READS+1
2 8C 23              SRC P1           READ SATELLITE POSITION DATA FROM INPORT 2
2 8D EA              RDR
2 8E 27              SRC P3           WRITE SATELLITE POSITION DATA INTO RAM0/
2 8F E0              WRM              REG1
2 90 77              ISZ R7           IF 13 SATELLITE POSITION CHARACTERS HAVE
2 91 86              -   READS        BEEN WRITTEN INTO RAM GO ON TO TRANSFER
2 92 22              FIM P1           THEM FROM REG1 TO REG2 AND INSERT DECIMAL
2 93 13              1   3            POINTS AND CHS WHERE NECESSARY
2 94 24              FIM P2
2 95 20              2   0            TO SELECT RAM0/REG2/CHARACTERS 0 THRU F
2 96 D0              LDM 0
2 97 B6              XCH R6           TRANSFER 3 CHARACTERS FROM RAM REG1 TO REG2
2 98 52              JMS -
2 99 E0              -   NCHARS
2 9A DA              LDM A
2 9B 25              SRC P2           WRITE DECIMAL POINT (A) INTO REG2
2 9C E0              WRM
2 9D 65              INC R5
2 9E DE              LDM E
2 9F B6              XCH R6
2 A0 52              JMS -            TRANSFER 2 CHARACTERS FROM RAM REG1 TO REG2
2 A1 E0              -   NCHARS
2 A2 23              SRC P1
2 A3 F0              CLB
2 A4 E9              RDM              IF 6TH CHARACTER IN RAM REG1 1 BIT = 0 THEN
2 A5 63              INC R3           SIGN IS -
2 A6 F6              RAR
2 A7 1A              JCN C0
2 A8 AD              -   MINUS
2 A9 D0 POSITIVE     LDM 0            IF 6TH CHARACTER IN RAM REG1 1 BIT NOT = 0
2 AA B8              XCH R8           SAVE R8 = 0 FOR + SIGN
2 AB 42              JUN -
2 AC AF              -   NEXT
2 AD DB MINUS        LDM B            IF 6TH CHARACTER IN RAM REG1 1 BIT = 0
2 AE B8              XCH R8           SAVE R8 = B FOR - SIGN
2 AF DF NEXT         LDM F
2 B0 B6              XCH R6           TRANSFER 1 CHARACTER FROM RAM REG1 TO REG2
2 B1 52              JMS -
2 B2 E0              -   NCHARS
2 B3 DA              LDM A
2 B4 25              SRC P2           WRITE DECIMAL POINT (A) INTO RAM REG2
2 B5 E0              WRM
2 B6 65              INC R5
2 B7
2 B8 DE              LDM E            TRANSFER 2 CHARACTERS FROM RAM REG1 TO REG2
2 B9 B6              XCH R6
2 BA 52              JMS -
2 BB E0              -   NCHARS
2 BC A8              LD  R8
2 BD 25              SRC P2           WRITE 0 OR B SAVED IN R8 INTO REG2 FOR + OR
2 BE E0              WRM              CHS
2 BF 65              INC R5
```

```
2 C0 23                 SRC P1
2 C1 F0                 CLB
2 C2 E9                 RDM                          IF 10TH CHARACTER IN RAM REG1 1 BIT =0 THEN
2 C3 63                 INC R3                       SIGN IS -
2 C4 F6                 RAR
2 C5 1A                 JCN C0
2 C6 CB                 -    MINUS
2 C7 D0 POSITIVE        LDM 0                        IF 10TH CHARACTER IN RAM REG1 1 BIT NOT = 0
2 C8 B8                 XCH R8                       SAVE R8 = 0 FOR + SIGN
2 C9 42                 JUN -
2 CA CD                 -    NEXT
2 CB D8 MINUS           LDM 8                        IF 10TH CHARACTER IN RAM REG1 1 BIT = 0
2 CC B8                 XCH R8                       SAVE R8 = 8 FOR - SIGN
2 CD D0 NEXT            LDM 0
2 CE B6                 XCH R6                       TRANSFER 3 CHARACTERS FROM RAM REG1 TO REG2
2 CF 52                 JMS -
2 D0 E0                 -    NCHARS
2 D1 DA                 LDM A
2 D2 25                 SRC P2                       WRITE DECIMAL POINT (A) INTO RAM REG2
2 D3 E0                 WRM
2 D4 65                 INC R5
2 D5 A8                 LD   R8
2 D6 25                 SRC P2                       WRITE 0 OR 8 SAVED IN R8 INTO REG2 FOR + OR
2 D7 E0                 WRM                          CHS
2 D8 C0                 BBL                          RETURN TO MAIN PROGRAM
2 D9
2 DA
2 DB
2 DC
2 DD
2 DE
2 DF
2 E0 23 NCHARS          SRC P1                       NCHARS TRANSFERS A SPECIFIED NUMBER OF
2 E1 E9                 RDM                          SATELLITE POSITION CHARACTERS FROM RAM0/
2 E2 F4                 CMA                          REG1 TO REG2
2 E3 25                 SRC P2
2 E4 E0                 WRM
2 E5 63                 INC R3                       INCREMENT RAM REG1 CHARACTER ADDRESS
2 E6 65                 INC R5                       INCREMENT RAM REG2 CHARACTER ADDRESS
2 E7 76                 ISZ R6
2 E8 E0                 -    NCHARS                  INCREMENT NUMBER OF CHARACTERS COUNTER
2 E9 C0                 BBL                          RETURN TO SPOS
2 EA
2 EB
2 EC
2 ED
2 EE
2 EF
2 F0
2 F1
2 F2
2 F3
2 F4
2 F5
2 F6
2 F7
2 F8
2 F9
2 FA
2 FB
2 FC
2 FD
2 FE
2 FF
```

3	00	3C	CA/CE	PROM 3 IS USED FOR KEY STROKE CODE STORAGE
3	01	3C	CA/CE	ENTER LONGITUDE OF SATELLITE
3	02	23	-	ENTER LONGITUDE OF TRANSMITTER OR RECEIVER
3	03	27	=	
3	04	3B	STO	ENTER LATITUDE OF TRANSMITTER OR RECEIVER
3	05	32	COS	
3	06	24	X	
3	07	28	(	ENTER LATITUDE OF SATELLITE
3	08	32	COS	
3	09	24	X	
3	0A	28	(	
3	0B	37	RCL	
3	0C	32	COS	
3	0D	29	)	
3	0E	29	)	
3	0F	27	=	
3	10	3B	STO	ENTER LATITUDE OF TRANSMITTER OR RECEIVER
3	11	31	SIN	
3	12	24	X	ENTER LATITUDE OF SATELLITE
3	13	31	SIN	
3	14	27	=	
3	15	22	+	
3	16	37	RCL	
3	17	27	=	
3	18	3B	STO	
3	19	16	5	
3	1A	21	.	
3	1B	1A	9	
3	1C	19	8	-2RH = -5.98147 X 10**9
3	1D	12	1	
3	1E	15	4	
3	1F	18	7	
3	20	2B	CHS	
3	21	2C	EE	
3	22	1A	9	
3	23	24	X	
3	24	37	RCL	
3	25	22	+	
3	26	13	2	
3	27	11	0	
3	28	21	.	
3	29	13	2	
3	2A	12	1	R**2 + H**2 = 20.21396 X 10**9
3	2B	14	3	
3	2C	1A	9	
3	2D	17	6	
3	2E	2C	EE	
3	2F	1A	9	
3	30	27	=	
3	31	36	SQRT	
3	32	22	+	ENTER NORMALIZED RANGE OF SATELLITE
3	33	27	=	
3	34	22	+	ENTER TOTAL UP DELAY FROM RAM
3	35	27	=	
3	36	22	+	
3	37	21	.	
3	38	11	0	
3	39	12	1	
3	3A	27	=	
3	3B	2B	CHS	
3	3C	22	+	SUBTRACT TOTAL COMPUTED DELAY FROM 300000.
3	3D	14	3	MICROSECONDS
3	3E	11	0	
3	3F	11	0	

```
3 40 11        0
3 41 11        0
3 42 11        0
3 43 21        .
3 44 27        =
3 45 24        X
3 46 12        1
3 47 21        .          X 1.024 = RATIO BETWEEN DECODER
3 48 11        0          MICROPROCESSOR CLOCK AND DELAY
3 49 13        2          MICROPROCESSOR CLOCK FREQUENCIES, THAT IS
3 4A 15        4          THE MINIMUM DELAY GENERATOR STEP IS
3 4B 27        =          9.765625 MICROSECONDS AND NOT 10.
3 4C 2B        CHS        MICROSECONDS
3 4D 22        +
3 4E 12        1
3 4F 11        0
3 50 11        0          10S COMPLEMENT DELAY GENERATOR SETTING
3 51 11        0          BECAUSE OF UP COUNTERS USED IN DELAY
3 52 11        0          GENERATOR
3 53 11        0
3 54 21        .
3 55 27        =
3 56 22        +
3 57 21        .
3 58 11        0          THESE STROKES ARE USED FOR DECIMAL POINT
3 59 11        0          ADJUSTMENT OF DELAY GENERATOR SETTING
3 5A 12        1          CALCULATION
3 5B 27        =
3 5C
3 5D
3 5E
3 5F
3 60
3 61
3 62
3 63
3 64
3 65
3 66
3 67
3 68
3 69
3 6A
3 6B
3 6C
3 6D
3 6E
3 6F
3 70
3 71
3 72
3 73
3 74
3 75
3 76
3 77
3 78
3 79
3 7A
3 7B
3 7C
3 7D
3 7E
3 7F
```

```
3 C0                    LOCATIONS 80 THRU BF ARE BLANK AND HAVE BEEN OMITTED
3 C1                    FROM THIS LISTING
3 C2
3 C3
3 C4
3 C5
3 C6
3 C7
3 C8
3 C9
3 CA
3 CB
3 CC
3 CD
3 CE
3 CF
3 D0
3 D1
3 D2
3 D3
3 D4
3 D5
3 D6
3 D7
3 D8
3 D9
3 DA
3 DB
3 DC
3 DD
3 DE
3 DF
3 E0 22 KCPROM      FIM P1          KCPROM ENTERS SPECIFIED KEY CODES STORED IN
3 E1                0   0           PROM
3 E2 24             FIM P2          TO SELECT I/O PORTS 3
3 E3 30             3   0
3 E4 36 NOP         FIN P3          KEY CODE ADDRESS IS IN P0, KEY CODE WILL BE
3 E5 51             JMS -           STORED IN P3
3 E6 20             -   INPUTKC     WRITE NOP, WRITE KEY CODE, WAIT FOR DONE
3 E7 71             ISZ R1
3 E8 EA             -   TESTADD     INCREMENT KEY CODE ADDRESS A2A1 FOR FIN
3 E9 60             INC R0
3 EA F0 TESTADD     CLB
3 EB A8             LD  R8
3 EC 90             SUB R0
3 ED 1C             JCN A1          TEST KEY CODE ADDRESS IN P0 TO SEE IF LAST
3 EE E4             -   NOP         KEY CODE HAS BEEN EXECUTED --- IF NOT
3 EF F0             CLB             EXECUTE NEXT ONE.
3 F0 A9             LD  R9
3 F1 91             SUB R1
3 F2 1C             JCN A1
3 F3 E4             -   NOP
3 F4 C0             BBL             RETURN TO MAIN PROGRAM
3 F5
3 F6
3 F7
3 F8
3 F9
3 FA
3 FB
3 FC
3 FD
3 FE
3 FF
```

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