SYSTEM-LEVEL INTEGRATION OF A CHIP-SCALE ATOMIC CLOCK: MICROWAVE OSCILLATOR AND PHYSICS PACKAGE

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Abstract-We report on our progress in developing a prototype chip-scale atomic clock and describe the integration of the local oscillator and the physics package. A discussion of the design and results is given with a focus on frequency stability, size, and power consumption. Finally, we suggest methods to improve reliability.
***Keywords*:** atomic clocks, CSAC, CPT, microfabrication, VCO.

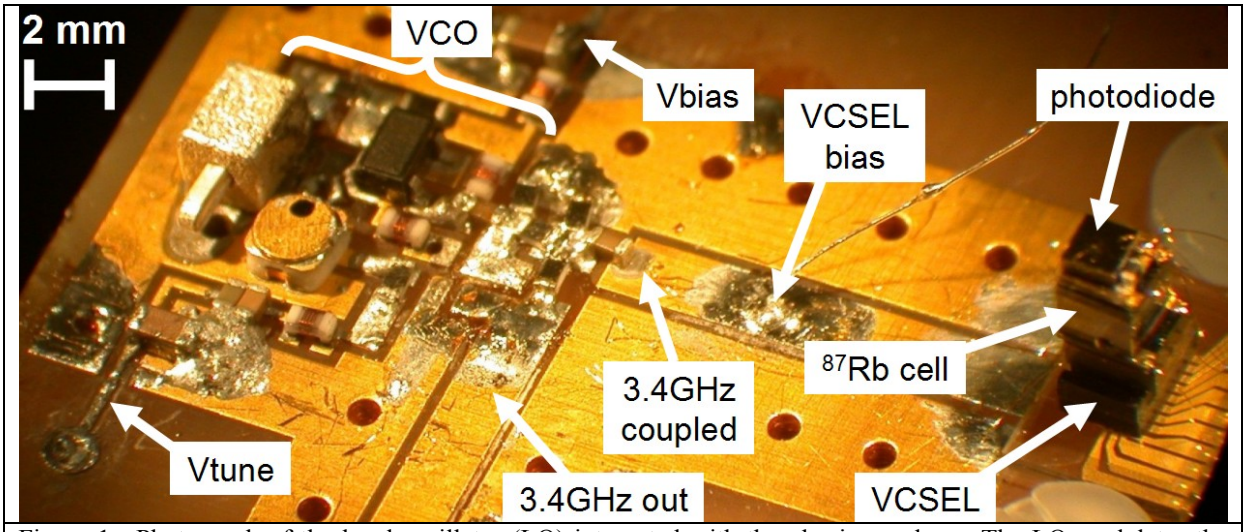

Figure 1. Photograph of the local oscillator (LO) integrated with the physics package. The LO modulates the vertical-cavity surface-emitting laser (VCSEL) at 3.4173 GHz, exciting the coherent-population-trapping (CPT) resonance of gaseous ^{87}Rb atoms contained in a glass and silicon cell. The photodetector at the top of the physics package receives the laser light and control electronics (not shown) tune the LO to a lock on the CPT resonance.

INTEGRATED LO AND PHYSICS

The goal of the chip-scale atomic clock (CSAC) project has been to design a frequency reference with instability better than 10^{-11} at one hour (extrapolated to a short-term instability below $6\times10^{-10}/\tau^{1/2}$ at short times) with power consumption less than 30 mW and in a package smaller than 1 cm^3. At one hour integration, this is comparable to the stability of commercially available compact atomic frequency references but with two orders of magnitude reduction in size and power consumption. We report our progress in this direction with the successful integration of the local oscillator (LO) [1, 2] and the physics package [3] on a single circuit board, forming a system that meets the stability specification with an Allan

1-4244-0628-5/06/$20.00 ©2006 IEEE

deviation of $2.5 \times 10^{-10}/\tau^{1/2}$ for short integration times. The occupied volume of the components is less than 0.5 cm^3 and they are integrated as shown in Figs 1-3. Inputs to the board are DC bias and tune voltages for the LO, DC current bias for the vertical-cavity surface-emitting laser (VCSEL), and currents to resistive heaters on the physics package. The outputs are a stabilized 3.4173 GHz reference frequency, photodetector signal for locking to the atomic resonance, and voltages for temperature stabilization of the rubidium vapor cell and the VCSEL. Electronics for temperature control and for locking the VCO to the atomic resonance are external but could in principle be integrated on the remaining board space. The total power consumption is 147 mW and 137 mW of this is for heating the laser and the ^{87}Rb atoms. In principle, a package can be designed as in [4] that consumes much less power for heating. In our case, the local oscillator consumes only 8.4 mW from a 3.3 V power supply and fills the majority of the volume at 0.4 cm^3. The physics package fills approximately 0.1 cm^3 and, apart from thermal power consumption, consumes only 2 mW. The FR-4 substrate shown in Fig. 1 is larger than would be necessary for a finalized design but allows access to test points and to LO components for frequency tuning and modifications.

SYSTEM DESIGN

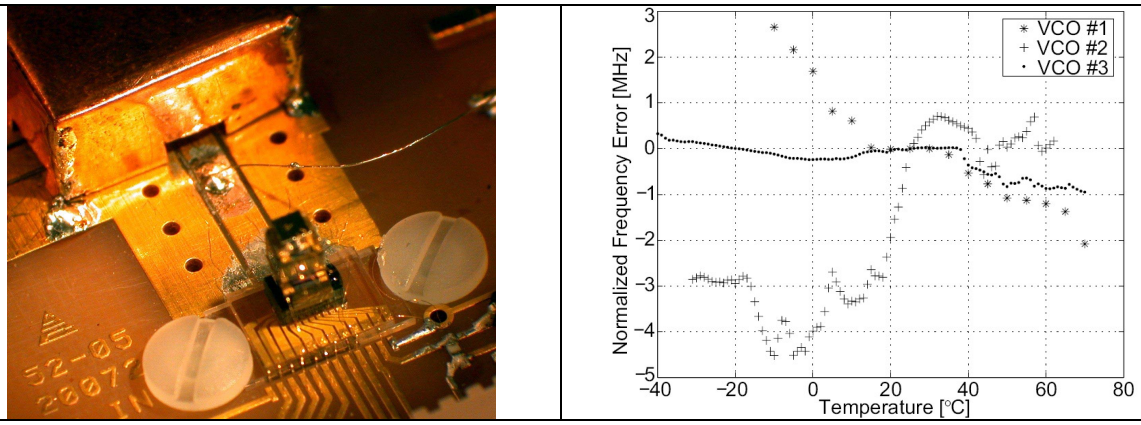

Figure 2. Photograph of integrated LO and physics (left) showing the electric shield placed around the LO and (right) thermal frequency drift of three LO's of similar design when not locked to the physics package.

The design for this type of oscillator in terms of DC consumption, RF power output, thermal stability, and low phase noise has been discussed in [2]. The design of the physics package has been discussed in [3]. Integrating these components can be challenging considering the experimentally-determined requirements that: 1.) The 3.4173 GHz frequency should be maintained with a precision better than 340 mHz for one-hour integration times using feedback from control electronics. 2.) The VCSEL must be modulated with between -6 dBm and -9 dBm of RF power, 3.) More than -20 dBm of useful RF power should be coupled out of the circuit, and 4.) Low thermal losses are desired. The precision of the voltage tunability of the LO frequency is limited by the number of bits of the DAC that controls it. For a 12-bit DAC and a locking time of 1 ms, the tunability must be less than 266 kHz/V to achieve required stability. The right half of Fig. 2 shows that the free-running LO frequency typically varies more than this for temperatures away from room temperature. Additionally, part tolerances require approximately 3 MHz/V tunability for a reliable design [1]. Therefore, future designs will minimally require a 16-bit DAC and separate methods for coarse tuning

and fine tuning are desired. To reduce the effects of frequency variations due to external coupled and radiated fields, a copper shield, shown in Fig 2, was placed around the LO. To provide proper power levels and impedance matching to the VCSEL, a lumped-element coupling circuit was designed and then was replaced by a 6 dB lumped-element attenuator because unpredictable transmission line and bondwire lengths led to an uncertain RF impedance of the VCSEL. To overcome the attenuation losses, the LO power consumption was increased from the design in [2] to 8.4 mW. Finally, we modified the substrate for the second integrated system (shown in Fig. 3) resulting in a 20% reduction of heat losses through the conductors and the bulk FR-4 substrate. Holes were drilled in the substrate, the transmission line was made less wide, and a thinly-milled ledge was provided to support the physics package. Other improvements were adding a high-impedance laser bias line, reducing the size of the components on the LO, and adding AC coupling of the LO ground and the VCSEL ground to protect the laser and to eliminate a ground loop.

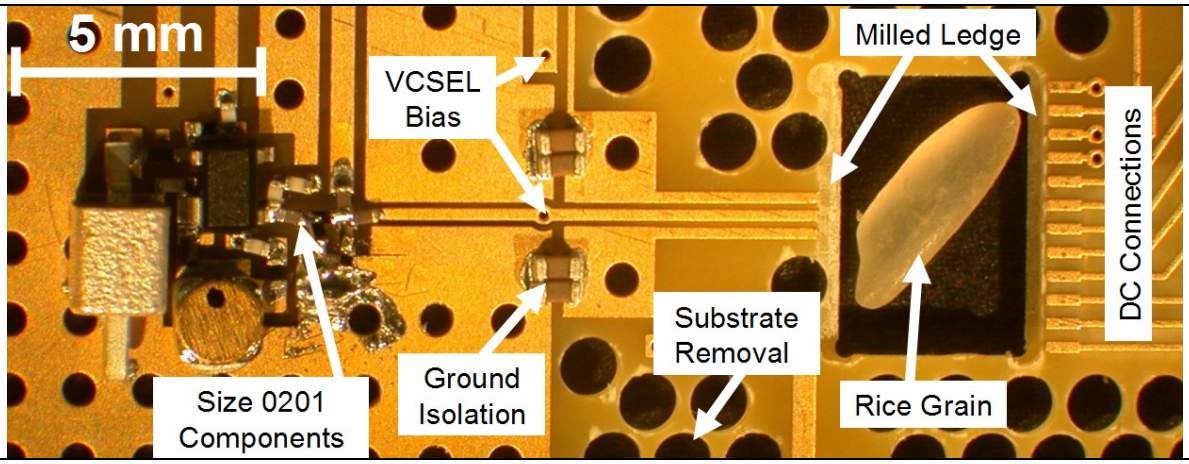

Figure 3. Photograph of an improved integrated system. The physics package is not shown, giving a better view of the board layout. Thermal power losses were reduced by the removal of unnecessary substrate material and by the thinning of circuit traces near the physics package.

CONCLUSION

Though this system has met the size and short-term stability requirements, the thermal power losses should be reduced with a better thermal design. The system remains susceptible to external radiated and coupled fields. Significant reduction in this sensitivity can be achieved at a cost of a few milliwatts of DC power consumption with the introduction of a buffer amplifier after the LO. This would also reduce undesirable frequency shifts caused by strong RF reflections from the VCSEL and coupled output. Further shielding can be obtained using stripline in a multilayer circuit board and by shielding the entire package.

ACKNOWLEDGMENT

This work was supported by the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA). The first author was supported by fellowships from the National Science Foundation and NIST. This work is in part a contribution of NIST, an agency of the US government, and is not subject to copyright.

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