Proceedings ICTF
NPL, New Delhi, 6-7 February 2001

Microwave Synthesisers for Atomic Frequency Standards

A. Sen Gupta*, F. L. Walls, J. F. Garcia Nava and C. Nelson

**National Physical Laboratory,*
New Delhi, India
National Institute of Standards & Technology,
Boulder, Co, USA

Abstract

Following our earlier work, on a new approach to synthesising the Cs hyperfine frequency of 9.192 GHz, we describe developments on its further refinements. The new design has the flexibility to generate not only the Cs hyperfine clock transition frequency but also frequencies corresponding to the Rb, 6.834GHz; Hydrogen, 1.414GHz; Mercury, 40.5GHz etc with a resolution of ~0.2 μ Hz and a range of several MHz. The salient feature of our design is that it is mainly based on frequency division and requires no narrow band filter stages. Tests indicate an internal fractional frequency stability of 1.5 x 10^{-15} at 10 s and 1 x 10^{-18} at 1 day. The temperature coefficient is approximately 0.1 ps to 0.5 ps/ ^{o}K, depending on which output frequency is chosen. We have added digital control of the oscillators so that no mechanical intervention in needed to tune the oscillators over a 25-year lifetime. The units now accept a single input voltage of 24 ±4 V and uses RS 432 for all control and monitoring functions.

1. Introduction

The advent of newer generations of ultra high stability frequency standards based on laser cooled atoms and ions [1-3] has created a situation where the performance of the local oscillator and the microwave synthesis chain appear to be limiting factor. In an earlier work [4] we had described a new approach to design a microwave synthesiser for Cs hyperfine clock transition, having high resolution, low phase modulation (PM) and amplitude modulation (AM) noise, low spurs near the carrier, and very high phase stability with respect to environmental effects. Since this synthesiser was originally intended to be for a slow beam Cs primary atomic reference clock in space (PARCS) scheduled for flight aboard the international space station [5], it required the use of components that are or can be space-qualified. Other major features of the synthesiser were its compactness, robustness and low power consumption, and that all dissipated heat to be removed by conduction and radiation, as there is minimal convection in space. A fractional frequency step of 2 x 10^{-17} was achieved by mixing the output of a 48 bit numerically controlled oscillator with the microwave signal. Preliminary tests on the new synthesiser design indicated an internal fractional frequency stability of 1.5 x 10^{-15} at 10 s and 1 x 10^{-18} at 1 d, dominated by the daily room temperature variations. The PM and AM noises were similar to the previous designs that used frequency multiplication and narrow band filters [6]. The temperature coefficient is less than 0.1 ps/ ^{o}K to 0.5ps/ ^{o}K depending on the output frequency.

In the present paper we give an update on the most recent work done at NIST on the Cs synthesiser. Secondly, we describe in block schematics how a general a microwave synthesiser that can be used to produce the various hyperfine clock transitions for Cs, Rb, H-maser, Hg^+ as well as an output to be locked to the pulse repetition rate (PRR) of a femtosecond (fs) lasers [7, 8].

2. Present Design of the Cs Synthesiser

The basic design details of our Cs synthesiser for PARCS [5] have been described in our earlier paper [4]. As shown in the Fig. 1, it is basically comprised of a 6.4GHz Dielectric Resonant Oscillator (DRO), which is phase locked to a 100 MHz Quartz oscillator and a 5 MHz quartz oscillator to improve spectral purity. The 6.4 GHz output is divided by a custom regenerative divider to yield outputs at 3.2 GHz and 9.6 GHz. The 3.2 GHz output is divided by 8 and further by 4 using commercial dividers to produce outputs at 400 MHz and 100 MHz respectively. The 100 MHz output and a 5 MHz, obtained by dividing it by 20, are used for the phase locking the 6.4 GHz DRO with the 100 MHz and 5 MHz quartz respectively. We use a 48-bit Direct Digital synthesiser (DDS), which is clocked by a 50 MHz (obtained by dividing the 100 MHz output by 2) to produce a 7.368 MHz with a resolution of 0.2 μHz. The 7.368 MHz output is mixed with the 400 MHz in an upper side band (USB) mixer to produce 407.368 MHz. The use of an USB eliminates the need for a narrow band filter to reduce the unwanted 7.368 MHz sidebands. This is again mixed with the 9.6 GHz to produce the final Cs output of 9.192....GHz to drive the hyperfine clock transition. A 9.192 GHz bandpass filter with a width of 180 MHz is used to eliminate the unwanted 407 MHz sidebands. The primary user output for measurements is at 100 MHz, although outputs at 5 MHz and 10 MHz are also available. To be useful for precision standards work, the phase delay between the 9 GHz and 100 MHz outputs should be stable with time and changing environmental parameters such as temperature and supply voltage.

Since there are no highly tuned band pass filters or multipliers in the present design, the temporal variation of the internal phase delay is small. The main delay variation appears to arise from temperature changes. Our investigations indicated that the uncompensated temperature coefficient of phase delay, which primarily arises from the digital dividers and the output amplifiers, is about 2 ps/K for the 100 MHz output and 25 ps/K for the 5 and 10 MHz outputs. Since the entire electronics is heat sunk very well to the metal body of the unit, there is a single time constant of temperature variation for all parts of the electronics. This results in a very stable temperature coefficient. It is quite simple to significantly reduce the temperature coefficient using a dc voltage proportional the temperature difference from room temperature to drive a RC phase shifter. The temperature sensor is heat sunk to the inside of the case containing the divider. The R in the phase shifter is the 50 Ω output impedance of the rf amplifier and the C is a varactor. Since the correction voltage is just the difference between the real temperature and the nominal room temperature set point, changing amplifier gain primarily changes the temperature coefficient and not the phase delay (varactor operating point). It then becomes a relatively simple matter to observe the phase of the synthesizer as the temperature is ramped up and down and adjust the gain to minimize the temperature coefficient. With appropriate scaling of the dc amplifier gain, a final temperature coefficient of approximately 0.1 ps/K was achieved for the synthesis from 9.2 GHz to 100 MHz. Similar procedures were used to compensate the 10 MHz and 5 MHz outputs to

achieve a temperature coefficient of approximately 0.5 ps/K. Typical results are shown in Fig. 2. Figure 3 shows the fractional frequency stability between the 9.192 GHz outputs of two synthesisers locked to the same 100 MHz reference.

Following our success with the two initial prototypes [4], several more units have been made with some changes to make them easier to use. These are

(1) Use of a single input dc voltage of 24 ±4 V with dc-to-dc converters to provide the specific voltages needed for different circuits. This makes it easy to batteries and charging circuits to provide failsafe power to the unit for long periods of time. We find that there is a phase shift of approximately 1 ps/V change in the power supply voltage. We have not yet identified which sub system is responsible for this voltage coefficient, however systems with a voltage stability of 0.1 V are readily available.

(2) Digital control of the coarse tuning of the 100 MHz and 5 MHz oscillators. Previously one had to mechanically tune the oscillators every several years to compensate for long-term drift. This is incompatible with PARCS and inconvenient for many other applications. The dc control should provide tuning over the lifetime of the oscillators of approximately 25 years.

(3) Use of RS 432 for all control and monitor functions. We use this addressable type of serial communications to control the DDS synthesizer(s), to control the tuning of the crystal oscillators and to monitor all the servo voltages

3. Design of a More General Microwave Synthesiser

A novel feature of our approach to the Cs frequency synthesis as described above, is that it is quite simple to generalise this to produce several outputs applicable to other atomic frequency standards. We describe below such a design in block schematic. Fig 4 shows the basic divider unit. It consists of the 6.4 GHz oscillator, which is phase locked to the 100 MHz and 5 MHz quartz oscillators for spectral purity, as before. The 6.4 GHz output is first divided using a regenerative divider to produce the 9.6 GHz and 3.2 GHz outputs. The 3.2 GHz output is successively divided to 1.6 GHz, 400 MHz, 200 MHz, 100 MHz, 10 MHz and 5 MHz. At present for our Cs synthesiser, commercially available digital dividers have been used. But these have the disadvantage of introducing noise floors that compromise the advantage of phase locking with the quartz oscillators and also the low noise floor of the 6.4 GHz oscillator far away from the carrier. Therefore, at a later time it may be worthwhile to use regenerative dividers for the entire divider chain, which incidentally will have the advantage of lower temperature coefficient too [9]. Using this basic divider unit one can then go on to generate the various output frequencies as needed. This is described below.

3.1 Cs Output

Figure 5 shows the scheme for generating the Cs output of 9.192....GHz. This has already been adequately discussed in [4] and in the previous section above.

3.2 Rb output

Figure 6 shows the scheme for generating the Rb output of 6.834,... GHz. Here we can generate a 34 MHz output by mixing the roughly 9 MHz DDS signal with the 25 MHz derived by dividing the 100 MHz by 4, in an USB mixer. The use of an USB eliminates the need for a narrow band filter to reduce the unwanted 9 MHz sidebands. The 34 MHz is mixed with the 400 MHz in another USB mixer to produce 434 MHz. The 434 MHz is mixed with the 6.4 GHz to give the needed 6.834 GHz output. A 6.834 GHz band pass filter with a width of 180 MHz is used to eliminate the unwanted 434 MHz sidebands.

3.3 H-Maser Output

In an active H-maser the basic signal comes out at 1.420405.. GHz. It is usual to phase lock a local oscillator to this signal using double super heterodyning. Thus, in the first stage one uses a local oscillator of 1.4 GHz to get an intermediate frequency of 20.405 MHz. This is then mixed with a synthesised 20.405... MHz to generate the error voltage used to lock the local oscillator. One can also have further stages of heterodyning if desired.

In our approach (Fig. 7) the generation of the 1.4 GHz would be obtained by mixing 1.6 GHz and 200 MHz. The 20.405...MHz would be generated by subtracting the roughly 4.595 MHz DDS from 25 MHz derived by dividing the 100 MHz by 4, in a lower sideband mixer (LSB)

3.4 Hg^+ Output

The hyperfine transition of Hg^+ is at 40.5073... GHz. The basic scheme for its synthesis, shown in Fig. 8, is similar to that described above. We could use a 25 MHz, obtained by dividing the 100 MHz by 4, to mix with the DDS output of 1.825... MHz in an USB mixer to produce 26.825... MHz. The use of an USB eliminates the need for a narrow band filter to reduce the unwanted 1.825 MHz sidebands. The 26.825 MHz signal could then be successively combined with 100 MHz and 400 MHz. The resulting 526.825... MHz signal is combined with 9.6 GHz to give 10.126825... GHz. A band pass filter with a width of roughly 180 MHz is used to reduce the unwanted 526 MHz sidebands. The 10.126 GHz signal could then be multiplied by 4, using a step recovery diode (SRD) or active multiplier to generate the needed Hg^+ output. A waveguide filter could be used to reduce the unwanted harmonics.

3.5 Femtosecond Laser Output

Mode-locked fs pulse laser provides ultra-short pulses (~30 fs) at the pulse repetition rate (PRR). This is typically 100 MHz to a few GHz. This modulation yields a comb of frequencies given by

$$\nu_o = nPRR + \nu_{offset}, \qquad (1)$$

where, n is the harmonic number and ν_{offset}, is the offset of the comb from zero [7, 8]. The shortness of the pulse requires phase coherence between all the comb lines, even to the

optical region. Mode-locked fs lasers have been used to make frequency comparisons between the PRR or multiples of the PRR and optical frequencies with unprecedented precision and accuracy. A particularly attractive scheme allows one to lock ν_{offset} to a fixed value and then lock one of the comb lines to a stable optical frequency standard. The PRR then must be locked to the optical reference frequency. Such optical standards have the potential of achieving fractional frequency stabilities of order 1×10^{-15} at 1s and to 10^{-18} at a day and beyond [10].

The frequency of the PRR is sensed by detecting a portion of the optical signal on an optical photo diode. The broadband noise in the optical detector primarily originates from shot noise and thermal noise in the detector. The detector noise adds white PM noise that is independent of the comb separation (until the separation approaches the bandwidth of the detector). This white PM noise significantly limits the short-term frequency stability of the detected PRR. One method to improve the white PM level and hence the short-term frequency stability of the readout signal is to detect at as high a multiple of the PRR as possible within the 3-dB bandwidth of the photo detector and use the low noise frequency synthesis techniques of Figs. 3-4 to provide the link to a standard reference frequency. Readily available synthesizer frequencies are 10.0, 9.6, 9.2, 6.4, or 3.2 GHz. Detected frequencies as high as 40 GHz can be prescaled to the 10 GHz region using microwave regenerative dividers [11].

4. Conclusion

We have described refinements of our earlier work, on a precision synthesiser for the Cs hyperfine frequency of 9.192 GHz. This make it possible to easily synthesise frequencies corresponding to the Rb, 6.834 GHz; Hydrogen, 1.414 GHz; Mercury, 40.5 GHz with a resolution of ~0.2 μ Hz and a range of several MHz. The synthesiser may also prove useful for the lower portion of femtosecond laser synthesis from the optical to the rf.

The salient feature of our design is that it is mainly based on frequency division and requires no narrow band filter stages. This yields synthesisers with an internal fractional frequency stability of 1×10^{-15} at 10 s and 1×10^{-18} at 1 day. The temperature coefficient is approximately 0.1 ps to 0.5/K, depending on which output frequency is chosen. We have added digital control of the oscillators so that no mechanical intervention in needed to tune the oscillators over a 25-year lifetime. The units now accept a single input voltage of 24 ±4 V and uses RS 432 for all control and monitoring functions.

5. Acknowledgements

One of us (ASG) would like to gratefully acknowledge the funding support under the Indo-US collaboration program. We thank John Hall for many stimulating conversations about these topics over the past 30 years. We are also grateful to Leo Hollberg, Scott Diddams and Thomas Udem for many helpful discussions and Eugene Ivanov for helpful discussions and for providing data on PRR PM noise.

References

[1] A. Clairon, P. Laurent, G. Santarelli, S. Ghezali,, S. N. Lea and M. Bahoura, "A Cesium Fountain Frequency Standard: Preliminary results," IEEE Trans I&M, 44, pp. 128-131, 1995.

[2] D.J. Wineland, J.C.Bergquist, J. Bollinger W.M. Itano, D. J. Heinzen, S. L. Gilbert, C. H. Maney, and M. G. Raizen, "Progress at NIST towards Absolute Frequency Standards Using Stored Ions," IEEE Trans. UFFC, 37, pp. 515-523, 1990.

[3] J. D. Prestage, R. L. Tjoelker, R. T. Wang, G. J. Dick and L. Maleki, "Hg^+ Trapped Ion Standard with Superconducting Cavity Maser Oscillator," IEEE Trans. UFFC, 42, pp. 200-205, 1993.

[4] A. Sen Gupta, Darko Popovich and Fred L. Walls - Cs Frequency Synthesis: A New Approach, IEEE Trans UFFC, **47**, March 2000, pp 475-479

[5] N. Ashby, A. Demarchi, T. Heavner, L. Hollberg, S. Jefferts, J. Kitching, T. Parker, W. Phillips, S. Rolston, H. Robinson, D. Sullivan and F. Walls - PARCS: A Primary Atomic Reference Clock in Space, Proc. Joint European Freq. and Time Forum and Intl. Freq. Cont. Symp., pp 141-144, April 1999.

[6] J. F. Garcia Nava, F. L. Walls, J. H. Shirley, W. D. Lee and M. C. Delgado Aramburo, "Environmental Effects in Frequency Synthesizers for Passive Frequency Standards," Proc. of 1996 IEEE Freq. Control Symp., pp. 973-979, June 1993.

[7] Thomas Udem, Jorg Reichert, Ronald Holzwarth, Scott Diddams, David Jones, Jun Ye, Steven Cundiff, Theordor Hansch, and John Hall, "A new type of frequency chain and its application to fundamental frequency metrology," to be published in Hydrogen II, Ed. S. Karshenboim, Springer 2001

[8] Yun Ye, John Hall, and Scott A. Diddams, "Precision phase control of an ultrawide-bandwidth femtosecond laser:a network of ultrastable frequency marks across the visible spectrum,"Optics Letters, **25**, pp. 1675-1677, 2000.

[9] M. Mossammaparast, C. McNeilage, P. Stockwell and J. H. Searls, " Phase Noise of X-Band Regenerative Frequency Dividers", Proc. 2000 IEEE/EIA Intl, Freq. Control Symp, Kansas City, Mo, 531-535, 2000.

[10] Lisa M. Nelson and Fred L. Walls, "Environmental effects in mixers and frequency distribution systems" Proc 1992 IEEE Freq. Cont. Symp, Hershey PA, 183-187, 1992

[11] E. S. Ferre-Pikal and F. L. Walls, "Microwave regenerative dividers with low PM noise, IEEE Trans. UFFC., **46,** 216-219, 1999

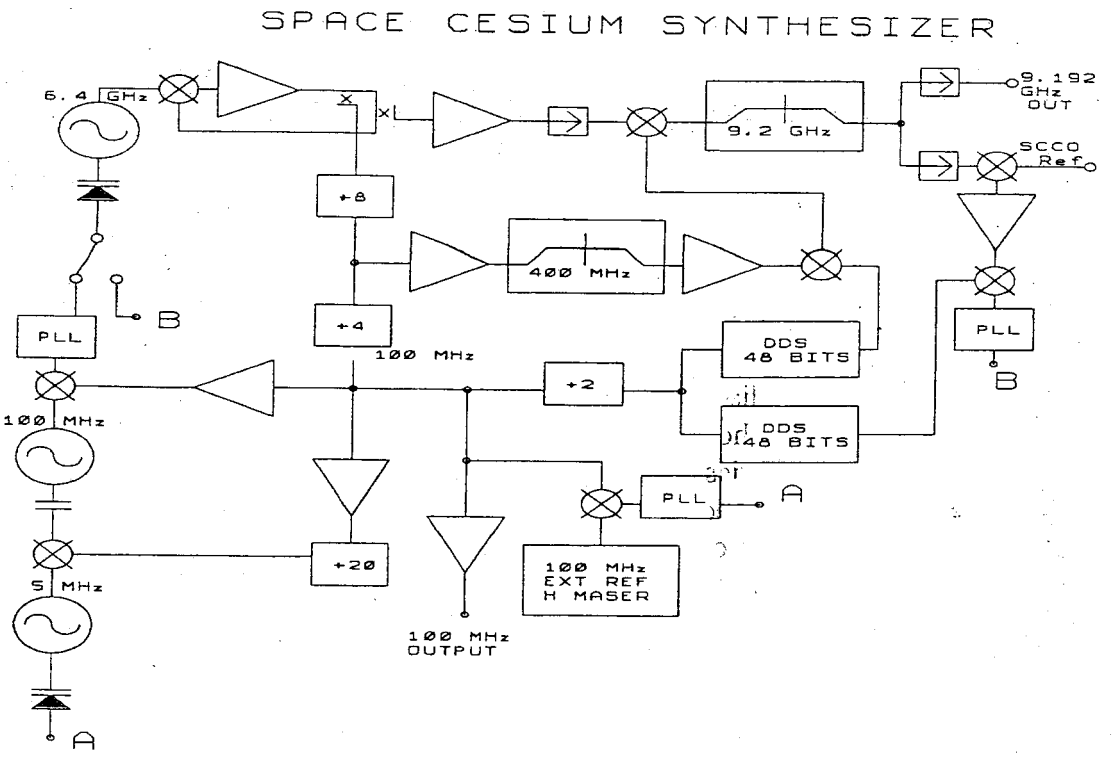

Figure 1. Block diagram of our Cs frequency synthesiser [4].

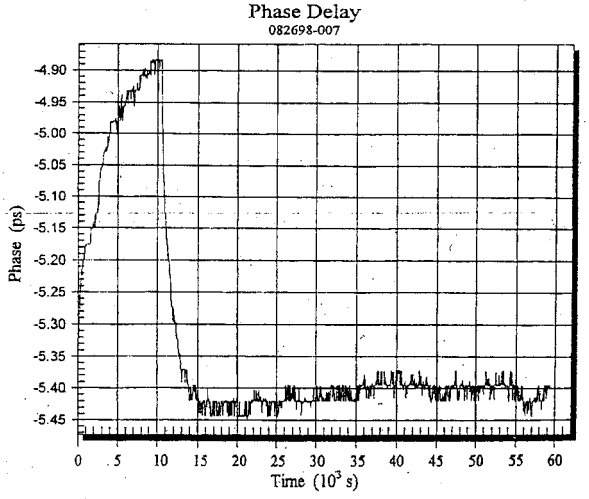

Figure 2. Compensated phase response of Cs synthesiser #2 for a temperature step up and back of 3.5 °K [4].

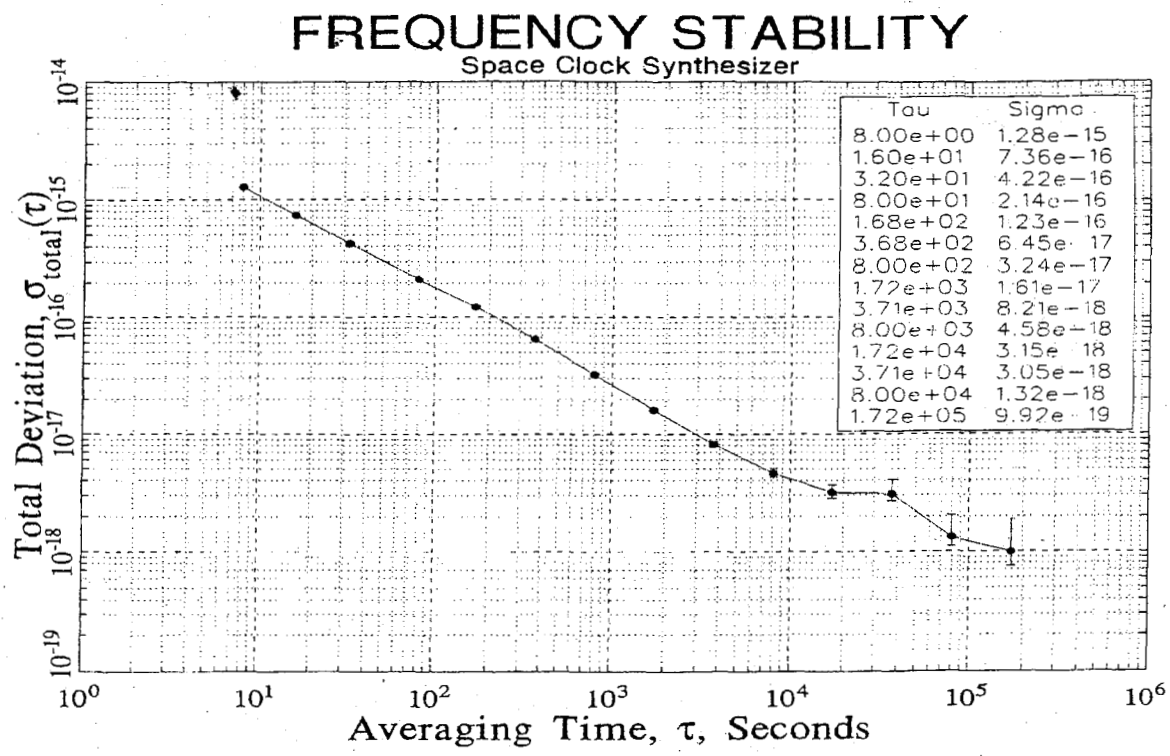

Figure 3. Allan deviation for a pair of our Cs synthesisers computed using total deviation.

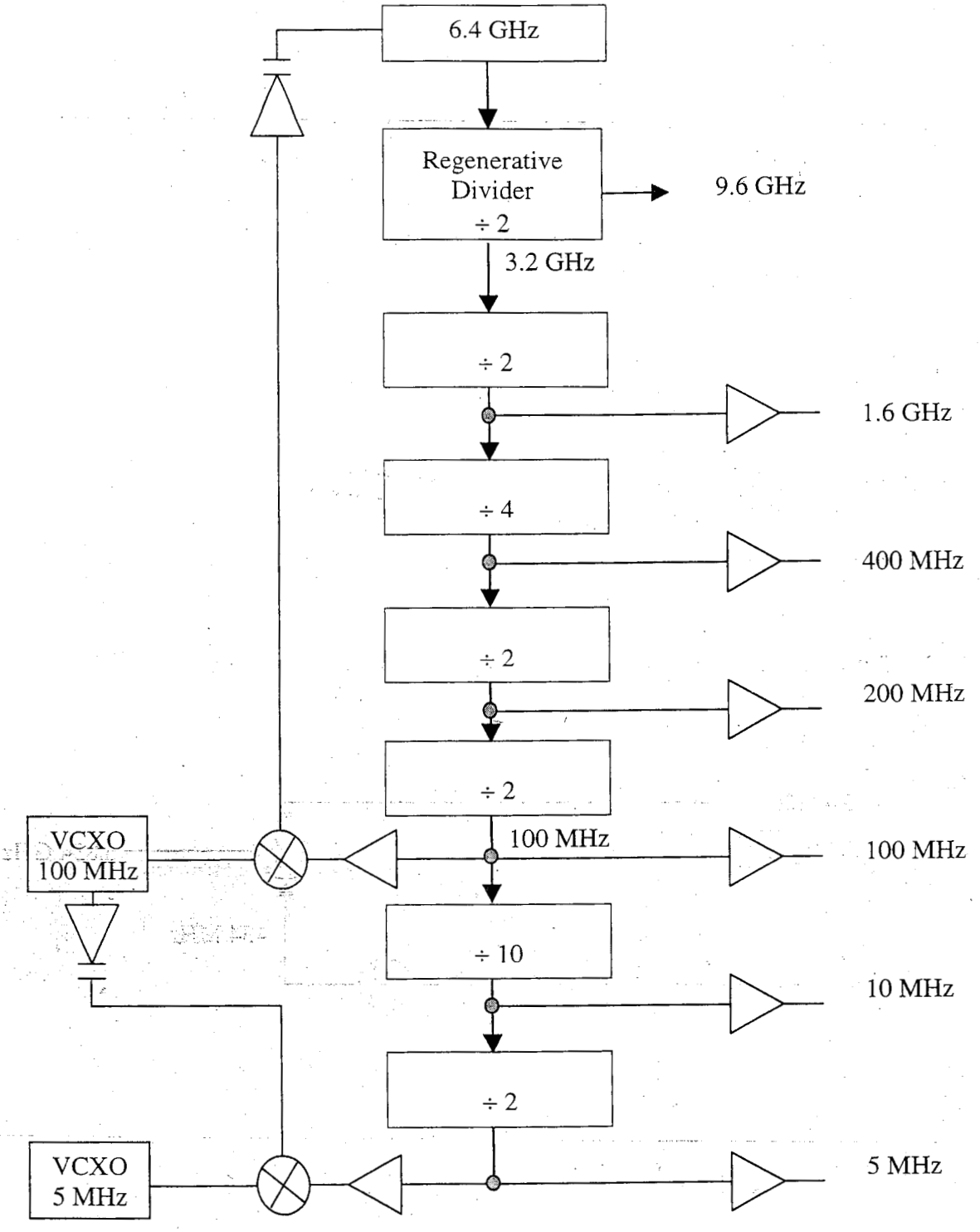

Figure 4. Basic oscillator, phase lock loops and divider chains in the proposed synthesiser

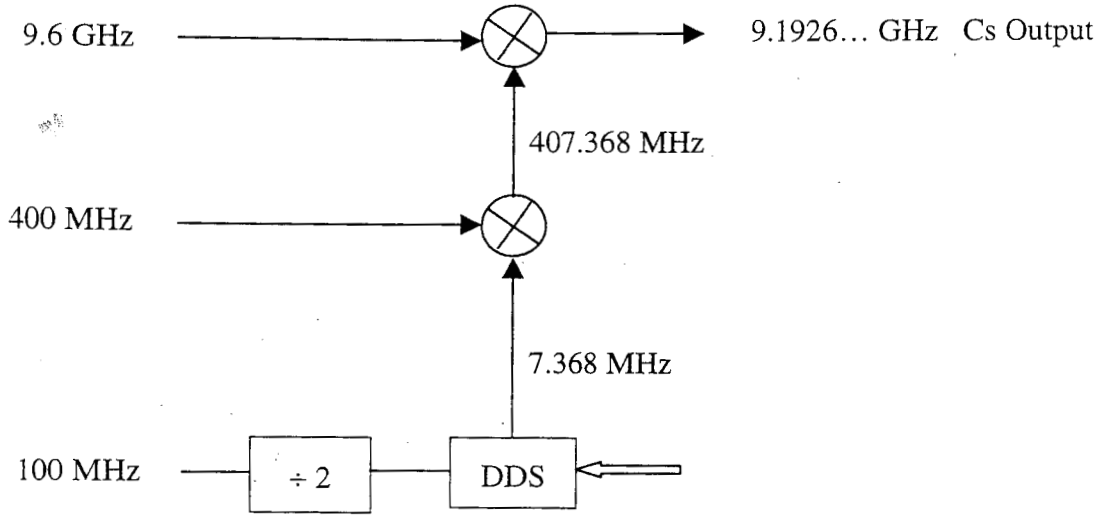

Figure 5. Synthesis scheme for producing output frequency corresponding to Cesium

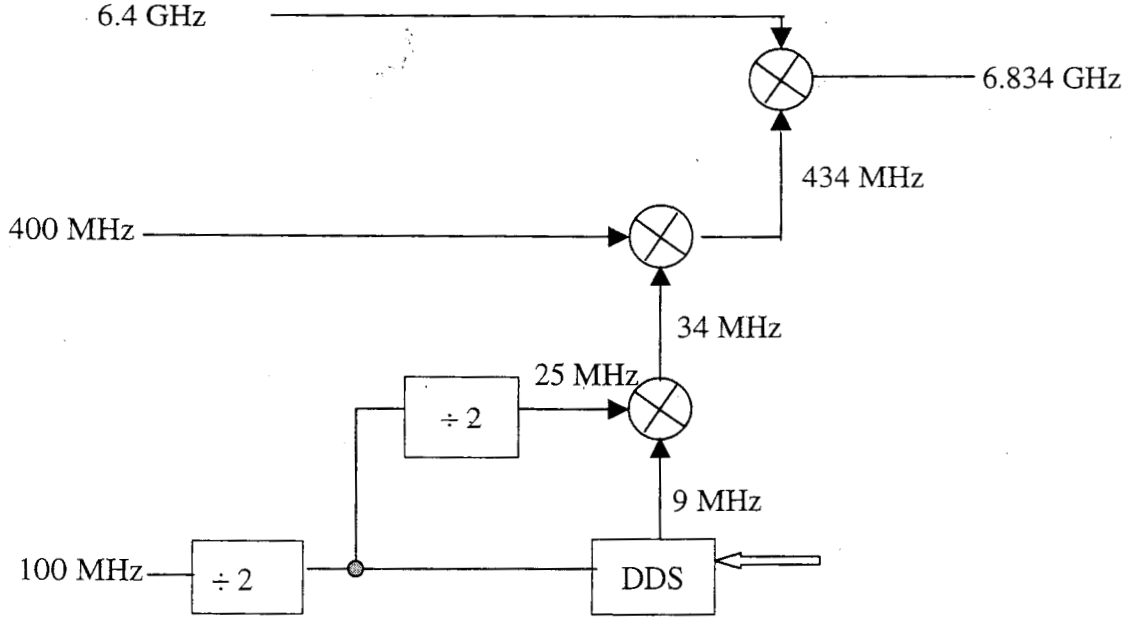

Figure 6. Synthesis scheme for the generating output frequency corresponding to Rubidium

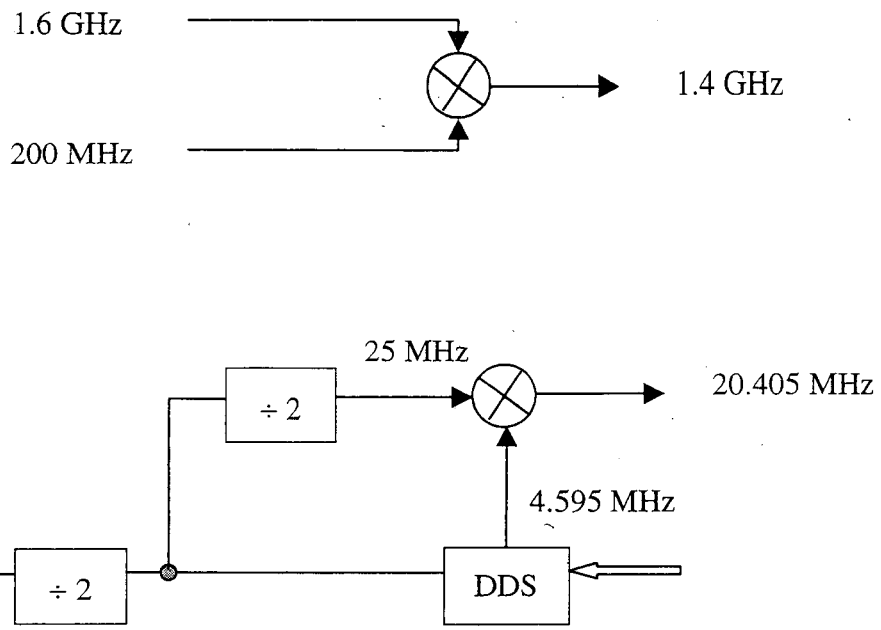

Figure 7. Synthesis scheme to generate outputs corresponding to an active H-Maser

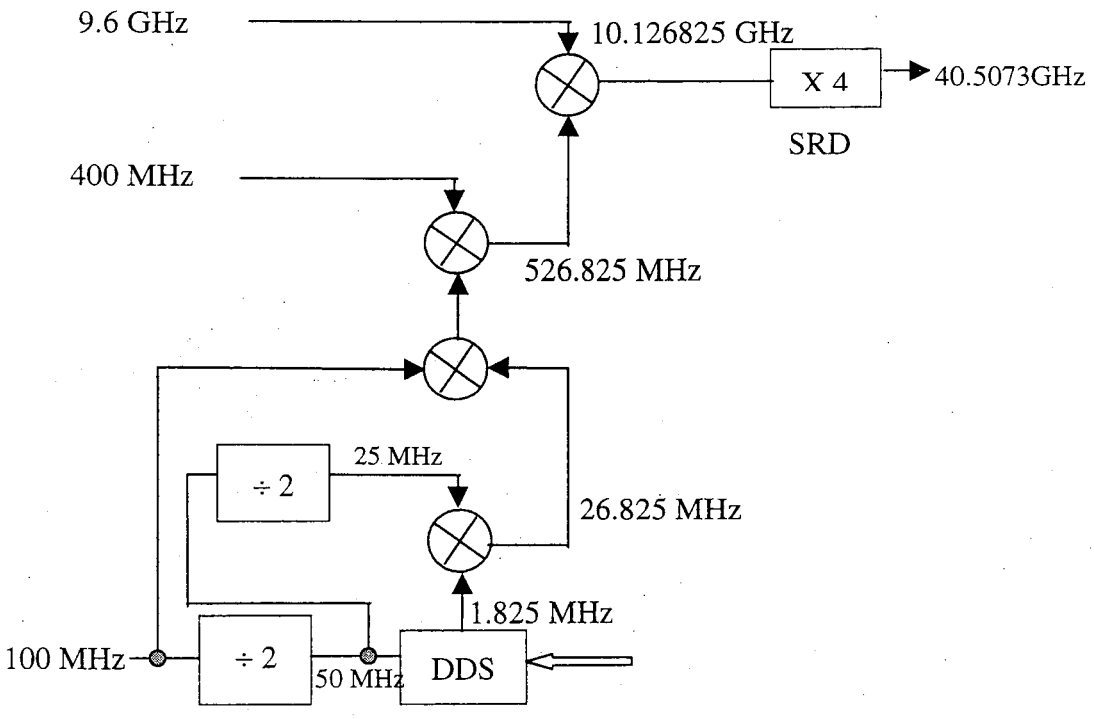

Figure 8. Synthesis scheme for generating the output frequency corresponding to Mercury ion