Cs Frequency Synthesis: A New Approach[1]

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Abstract—**This paper describes a new approach to synthesizing the Cs hyperfine frequency of 9.192 GHz that is designed to be sufficiently rugged for use in space, specifically for the Primary Atomic Reference Clock in Space (PARCS) planned for the International Space Station, as well as ground applications. This new approach requires no narrow band filters or frequency multiplication, and the primary source of cooling is conduction. Instead of frequency multiplication, it uses a custom regenerative divider stage followed by two commercial binary dividers and several mixing stages. A fractional frequency step of 2×10^{-17} is achieved by mixing the output of a 48-bit numerically controlled oscillator with the microwave signal. Preliminary tests on the new synthesizer design indicate an internal fractional frequency stability of 1×10^{-15} at 10 s and 1×10^{-16} at 1 d, dominated by the daily room temperature variations. The phase and amplitude noise are similar to our previous designs that used frequency multiplication and narrow band filters. The temperature coefficient is less than 0.2 ps/K.**

I. Introduction

Within the last decade, new generations of frequency standards based on laser-cooled atoms and ions with a fractional frequency stability approaching 10^{-16} at 1 d have been developed [1]–[3]. At this stability, the performance of the local oscillator and the microwave synthesis chain appear to be limiting factors. To support NIST's new standards, we have designed a new generation of microwave frequency synthesizers [4]–[6]. The basic criteria for these designs have been high resolution, low phase modulation (PM) and amplitude modulation (AM) noise, low spurs near the carrier, and very high phase stability with respect to environmental effects.

The aim of the present work was to design a microwave synthesizer for a laser-cooled Cs fountain compatible for use in space, specifically for a slow beam Cs primary atomic reference clock in space (PARCS) scheduled for flight on the International Space Station [7]. This required the use of components that are or can be space-qualified. Other major design goals were that the synthesizer be compact and robust; that it consume low power; and, very importantly, that all dissipated heat be removed by conduction and radiation as there is minimal convection in space. The performance goal was a frequency resolution of at least 10^{-15} and a fractional frequency stability at 1 d of lower than 1×10^{-16}.

In the following section, we describe our design. The approach yields a simple synthesis scheme that avoids frequency multiplication, narrow band filters, and phase-locked loops (PLL) but still produces an output that is settable with high resolution. We also discuss some initial performance results of the two units that were constructed. All performance goals were met or exceeded.

II. Design Details

Fig. 1 shows a schematic block diagram of the synthesizer. The output of a 6.4-GHz voltage-controlled dielectric resonant oscillator (DRO) drives a custom regenerative divide-by-2 circuit [8] composed of a mixer, a 3.2-GHz low-pass filter, and an amplifier in a closed-loop configuration. This regenerative divider provides low PM noise [9], a very low coefficient of phase shift with temperature, and simultaneous outputs at 0.5 and 1.5 times the input frequency, that is, at 3.2 and 9.6 GHz. The 3.2- and 9.6-GHz outputs are separated using a diplexer.

The 3.2-GHz output is divided to 100 MHz using a commercial divide-by-8 followed by a commercial divide-by-4[2]. The 100-MHz output of the dividers is low-pass filtered and buffered in a two-stage amplifier to provide the output reference frequency.

Another key constituent of the synthesizer is a numerically controlled oscillator using a direct digital synthesis (DDS) chip with 48-bit resolution[3]. This unit is clocked by a 50-MHz signal obtained by dividing the 100 MHz by 2. This DDS chip not only provides the high resolution and low spurs, but it is also available in a space-qualified version. The DDS output is a sine wave, which can be set to a resolution of 0.2 μHz and a rate up to 20 MHz using 14 data and control lines. Additionally, the frequency of the DDS can be switched to a new value without phase discontinuity in less than 1 μs. The frequency is nominally set at 7.368 MHz and is mixed with the 400 MHz from the binary divider using a simple upper sideband (USB) mixer, which gives more than 25 dB rejection at the carrier and lower sidebands. Additional suppression of these spurs could be obtained with further design refinements. The 407.368-MHz signal is mixed with the 9.6-GHz out-

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[2]The dividers were a Sciteq 1208 divide-by-8 (DSICOM Technologies, Inc., San Diego, CA) and a Plessey 8402 divide-by-4 (Mitel Semiconductor, Scotts Valley, CA). These are identified only for completeness and do not represent an endorsement by NIST.

[3]The DDS was a Stanford Telecom STEL 1173 (Stanford Telecommunications, Sunnyvale, CA), which is identified only for completeness and does not represent an endorsement by NIST.

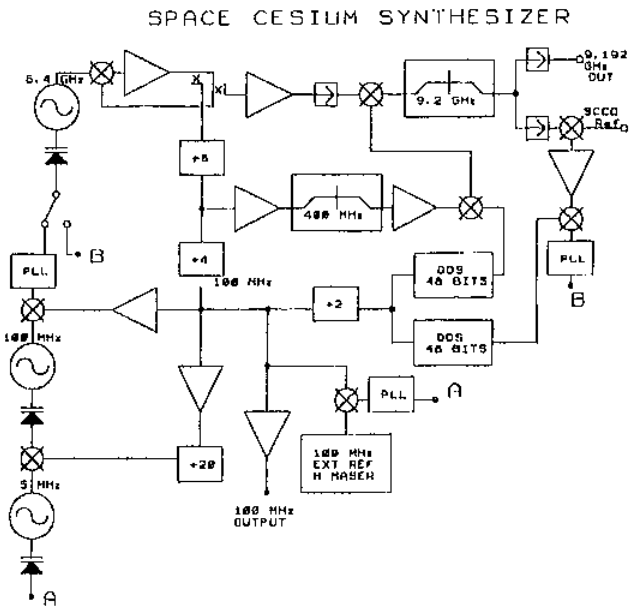

Fig. 1. Block diagram of the new Cs frequency synthesizer.

put of the regenerative divider to produce the 9.192-GHz signal, which is amplified and passed through a broadband filter and isolator to provide the final microwave output of the synthesizer.

As in our earlier synthesizer designs [4], [5], a 5-MHz oscillator controls the PM noise for Fourier frequency offsets up to approximately 50 Hz, and a 100-MHz oscillator controls the range from 50 Hz to 50 kHz.

The synthesizer output can be steered by voltage control of the 5-MHz oscillator using a DC error signal. This voltage control could be derived from the physics package of a Cs clock. The 100-MHz output from the synthesizer also drives a mixer, which can be used to detect the phase difference between the 100-MHz signal from a hydrogen maser or other high stability reference. This mixer output can be used to phase-lock the 5 MHz to this reference with a loop bandwidth of approximately 1 Hz. The low bandwidth was chosen to exclude spurs because of ground loops and pickup of electromagnetic interference. There is also a provision to phase-lock the synthesizer to a microwave reference such as a superconducting cavity oscillator (SCCO) as long as the frequency is within ±20 MHz of one of the internal reference frequencies (3.2, 6.4, 9.192, 9.6, or 10.007 GHz). To achieve this, we use another PLL with a second DDS set to the difference between the internal reference frequency and that of the SCCO. The output error of this PLL could correct the 6.4-GHz DRO with a bandwidth of up to approximately 300 kHz. It would also be possible to add an additional mixing stage to use a stable reference at the Rb hyperfine frequency of 6.834 GHz [10].

We constructed two prototype synthesizers of the above design. The mechanical assembly consisted of five interconnected modules with machined aluminum cases of 6-mm wall thickness. These were stacked tightly together. All circuitry, including the DDS, used surface-mounted components that were heat sunk to the printed circuit boards. The printed circuit boards in turn were heat sunk to the aluminum cases by mounting them flush against the bottom with thermally conductive film. In addition, metal straps connected the top of the few integrated circuits that dissipated significant heat to the sidewalls. (We have the ability to add external fins so that the units can be tested in air or on the ground, without the need for external fans). The entire microwave portion of the circuit was assembled in one module with the components mounted flush against the walls or the bottom. Thus, most of the heat dissipated in the synthesizer had a direct conduction path to the external heat sinks. This approach yielded a unit with thermal gradients across the modules that were less than 1 K, which proved very helpful as there is essentially only one temperature and one thermal time constant.

The unit is very compact and robust. The total size of each unit, excluding the external power supply and the removable heat sinks, was 22 × 13 × 18 cm. The volume could be reduced by roughly 40% by simply repackaging the present subassemblies. A careful finite element analysis of the thermal paths would allow us to determine how much additional metal can be removed from the modules and still maintain the required small thermal gradients, as well as verify the junction temperatures for long-term reliability. The total power consumption was approximately 22 W at 24°C. Although no quantitative vibration tests have yet been performed, many strong bumps, including the customary 10-cm drop test, produced no noticeable effects.

III. Results and Discussion

In this section, we describe results of tests made on the two units described previously. Extensive studies were made of the spurs and of the PM and AM noise.

Fig. 2 shows that there are no spurs within ±2.5 MHz of the 9.192-GHz output greater than 75 dB below the carrier (dBc). PM noise measurements were performed on the 100-MHz output using a three-cornered hat method involving two of the present synthesizers and one of the earlier type [4]. The results are summarized in Fig. 3. Also shown for comparison are the results of earlier designs [4], [5]. The results of measurements of AM noise and spurs at the microwave output are also very similar to those obtained with the earlier NIST synthesizers. These results indicate that frequency pulling by spectral impurities is of little consequence to present slow beam or fountain frequency standards [4].

The setup shown in Fig. 4 was used to study the phase stability with respect to environmental temperature variation between the microwave output and the user output at 100 MHz. The microwave outputs of the two synthesizers were phase-locked, and the 100-MHz outputs were used to drive a phase comparator and datalogger. The temperature of one of the synthesizers was kept constant, and

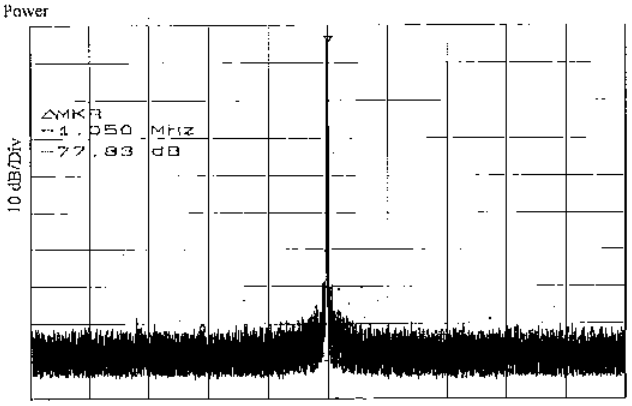

Fig. 2. Microwave power spectrum of the 9.192-GHz output from the new Cs synthesizer. The span is 5 MHz, and the resolution bandwidth is 1 kHz.

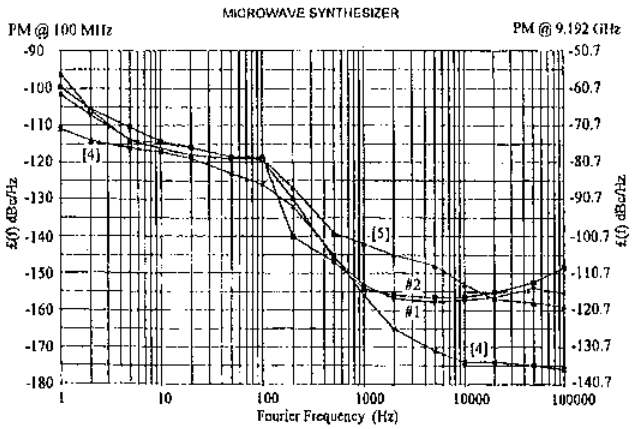

Fig. 3. Comparison of the PM noise spectrum of the new Cs synthesizer 1 and 2 to previous designs [4] and [5]. The vertical units are decibels below the carrier in a 1-Hz bandwidth.

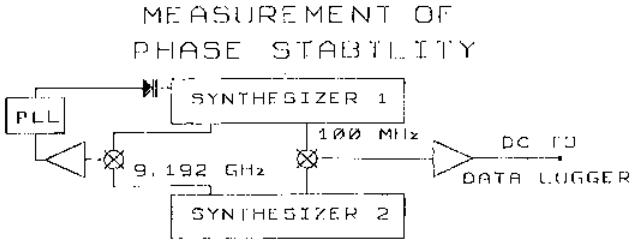

Fig. 4. Block diagram of setup used to measure the phase stability.

that of the other was varied. Fig. 5(a and b) show typical initial results of such temperature cycling from which we compute a phase temperature coefficient of 2.2 ps/K. An important point was that the phase temperature coefficient was almost identical for the two units and that there was less than a minute delay and almost no hysteresis between the temperature and phase variations. The reason for this is that the critical components are thermally well connected to the case so that there is essentially only one temperature and one thermal time constant. Further investigations revealed that the major part of the phase temperature coefficient arose from the last frequency divider and the output isolation amplifier. A very simple circuit consisting of a thermistor (heat sunk to the inside of the case containing the divider and the output amplifier) and a varactor to change the phase delay at the output of the 100 MHz in response to the temperature variations was successfully used to compensate most of the temperature coefficient. With several trials of scaling the variation of the voltage across the varactor, we were able to obtain a temperature coefficient of less than 0.2 ps/K as shown in Fig. 5(c). In subsequent tests, we obtained a very highly phase-stable 100-MHz output as shown for a 4-d stretch during which room temperature varied by approximately ±0.5°C (Fig. 6). Finally, we show, in Fig. 7, a typical plot of internal frequency stability obtained by processing the phase data with sampling times from 5 s to 1 d. We obtain a fractional frequency stability Allan deviation of 1×10^{-15} at 10 s and 1×10^{-18} at 1 d. The 1-d frequency stability is a significant improvement over stability results reported for previous designs [4].

IV. Conclusion

We have described a novel approach for synthesizing the microwave signal for a Cs standard. The realization of the design is simple, requiring no frequency multiplication or narrow band filters. Two prototype synthesizers were fabricated, keeping in mind the proposed use in space, and, hence, taking special care to ensure that all of the components could eventually be obtained in space-qualified versions. We also ensured that most components were heat sunk by thermal conduction to the case. This led to a very simple but effective means of compensating the temperature coefficient to lower than 0.2 ps/K and, consequently, obtaining internal frequency stability that reached 1×10^{-18} at 1 d. Another feature of the present design, the ability to set the microwave output with a resolution of 2×10^{-17}, is due to the use of a 48-bit DDS. Because there is no PLL in the final microwave synthesis, the phase excursions after switching frequency are small, and the settling time is less than 1 μs. Yet another feature of the synthesizer is the provision for phase-locking to an SCCO that is trimmed within 20 MHz of one of the internal reference frequencies (3.2, 6.4, 9.192, 9.6, or 10.007 GHz), providing for a much superior PM noise and short-term frequency stability than is possible using quartz oscillators.

Although the present synthesizers are already robust, compact, and consume low power, we estimate that further optimization should lead to a 70% reduction in volume and a 50% reduction in power consumption. Finally, although our present focus has been to synthesize the Cs hyperfine frequency, this approach could be adapted to produce similar performance at many other frequencies of interest (for example, the Rb frequency).

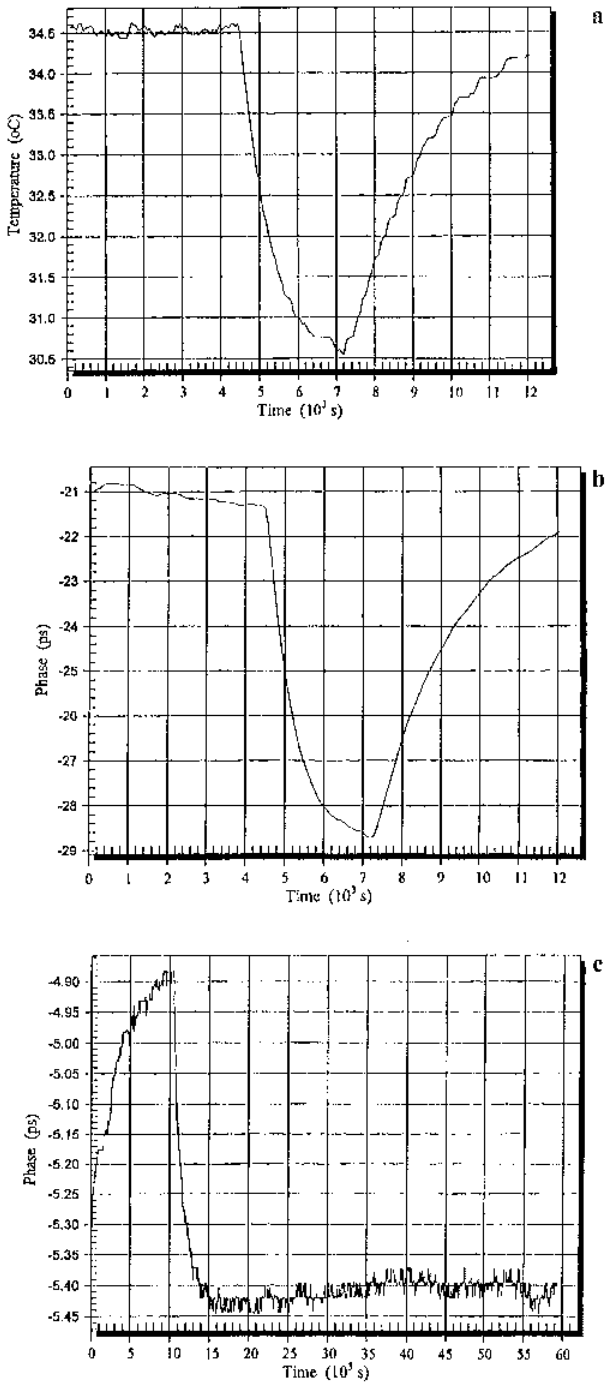

Fig. 5. a. Temperature change of synthesizer 1. b. Initial uncompensated phase response of synthesizer 1. c. Compensated phase response of synthesizer 2 for a temperature step up and back of 3.5°C.

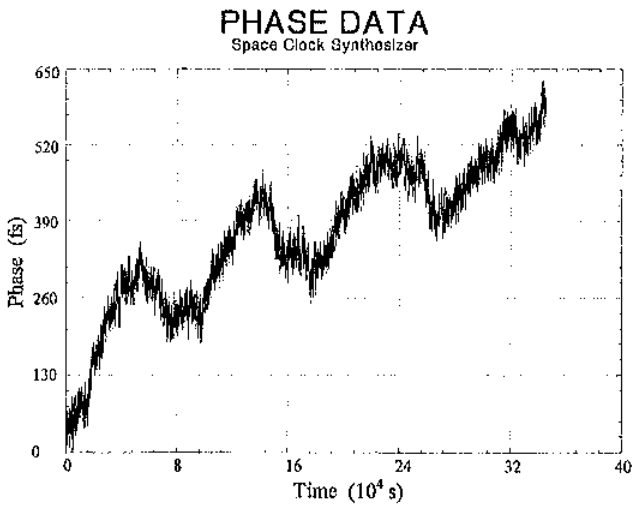

Fig. 6. Phase change between two synthesizers over 4 d.

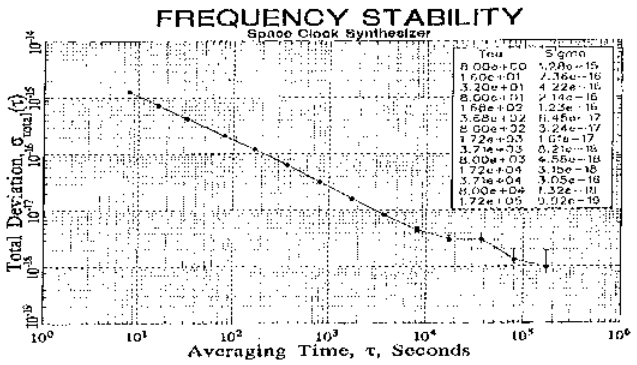

Fig. 7. Allan deviation for a pair of Cs synthesizers computed using total deviation and the data of Fig. 6.

Acknowledgments

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He received the 1995 European "Time and Frequency" Award from the Societe Francaise des Microtechniques et de Chronometric for "outstanding work in the ion storage physics, design and development of passive hydrogen masers, measurements of phase noise in passive resonators, very low noise electronics and phase noise metrology." He is the recipient of the 1995 IEEE Rabi Award for "major contributions to the characterization of noise and other instabilities of local oscillators and their effects on atomic frequency standards" and the 1999 Edward Bennet Rosa Award for "leadership in development and transfer to industry of state-of-the-art standards and methods for measuring spectral purity in electronic systems." He has also received three silver medals from the US Department of Commerce for fundamental advances in high resolution spectroscopy and frequency standards, the development of passive hydrogen masers and the development and application of state-of-the-art standards and methods for spectral purity measurements in electronic systems. Dr. Walls is a Fellow of the American Physical Society, a Senior Member of the IEEE, a member of the Technical Program Committee of the IEEE Frequency Control Symposium, and a member of the Scientific Committee of the European Time and Frequency Forum.