

## Cs FREQUENCY SYNTHESIS: A NEW APPROACH

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### ABSTRACT

This paper describes a new approach to synthesizing the Cs hyperfine frequency of 9.192 GHz that is designed to be sufficiently rugged for use in space, specifically for the primary atomic reference clock in space (PARCS) planned for the international space station, as well as ground applications. This new approach requires no narrow band filters or frequency multiplication and the primary source of cooling is conduction. Instead of frequency multiplication, it uses a custom regenerative divider stage followed by two commercial binary dividers and several mixing stages. A fractional frequency step of  $2 \times 10^{-17}$  is achieved by mixing the output of a 48 bit numerically controlled oscillator with the microwave signal. Preliminary tests on the new synthesizer design indicates an internal fractional frequency stability of  $1 \times 10^{-15}$  at 10 s and  $1 \times 10^{-18}$  at 1 day, dominated by the daily room temperature variations. The phase and amplitude noise are similar to our previous designs that used frequency multiplication and narrow band filters. The temperature coefficient is less than  $0.2 \text{ ps/}^\circ\text{C}$ .

### 1. INTRODUCTION

Within the last decade new generations of frequency standards based on laser cooled atoms and ions with stabilities approaching  $10^{-16}$  at 1 day have been developed [1-3]. At these stabilities, the performance of the local oscillator and the microwave synthesis chain appear to be limiting factors. To support NIST's new standards, we have designed a new generation of microwave frequency synthesizers [4-6]. The basic criteria for these designs have been high resolution, low phase modulation (PM) and amplitude modulation (AM) noise, low spurs near the carrier, and very high phase stability with respect to environmental effects.

The aim of the present work was to design a microwave synthesizer for a laser cooled Cs fountain compatible for use in space, specifically for a slow beam Cs primary atomic reference clock in space (PARCS) scheduled for flight the international space

station [7]. This required the use of components that are or can be space-qualified. Other major design goals were that the synthesizer be compact, robust, consume low power, and very importantly, that all dissipated heat be removed by conduction and radiation as there is minimal convection in space. The performance goal was a frequency resolution of at least  $10^{-15}$  and a fractional frequency stability at 1 day of lower than  $1 \times 10^{-16}$ .

In the following section we describe our design. The approach yields a simple synthesis scheme that avoids frequency multiplication, narrow band filters, and phase-locked loops while still producing an output that is settable with high resolution. We also discuss some initial performance results of the two units that were constructed. All performance goals were met or exceeded.

### 2. DESIGN DETAILS

Figure 1 shows a schematic block diagram of the synthesizer. The output of a 6.4 GHz voltage-controlled dielectric resonant oscillator (DRO) drives a custom regenerative divide-by-2 circuit [8], comprised of a mixer, a 3.2 GHz low-pass filter, and an amplifier in a closed-loop configuration. This regenerative divider provides low PM noise [9], a very low coefficient of phase shift with temperature, and simultaneous outputs at 0.5 and 1.5 times the input frequency, i.e., at 3.2 GHz and 9.6 GHz. The 3.2 GHz and 9.6 GHz outputs are separated using a diplexer.

The 3.2 GHz output is divided to 100 MHz using a commercial divide-by-8 followed by a commercial divide-by-4 [10]. The 100 MHz output of the dividers is low-pass filtered and buffered in a two-stage amplifier to provide the output reference frequency.

Another key constituent of the synthesizer is a numerically controlled oscillator using a direct digital synthesis (DDS) chip with 48 bit resolution [11]. This unit is clocked by a 50 MHz signal obtained by dividing the 100 MHz by 2. This DDS chip not only provides the high resolution and low spurs, but it is also available in a space-qualified version. The DDS output is a sine wave, which can be set to a resolution of  $0.2 \mu\text{Hz}$  and a rate up to 20 MHz using 14 data and control lines. Another feature of this DDS is that its frequency

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## SPACE CESIUM SYNTHESIZER

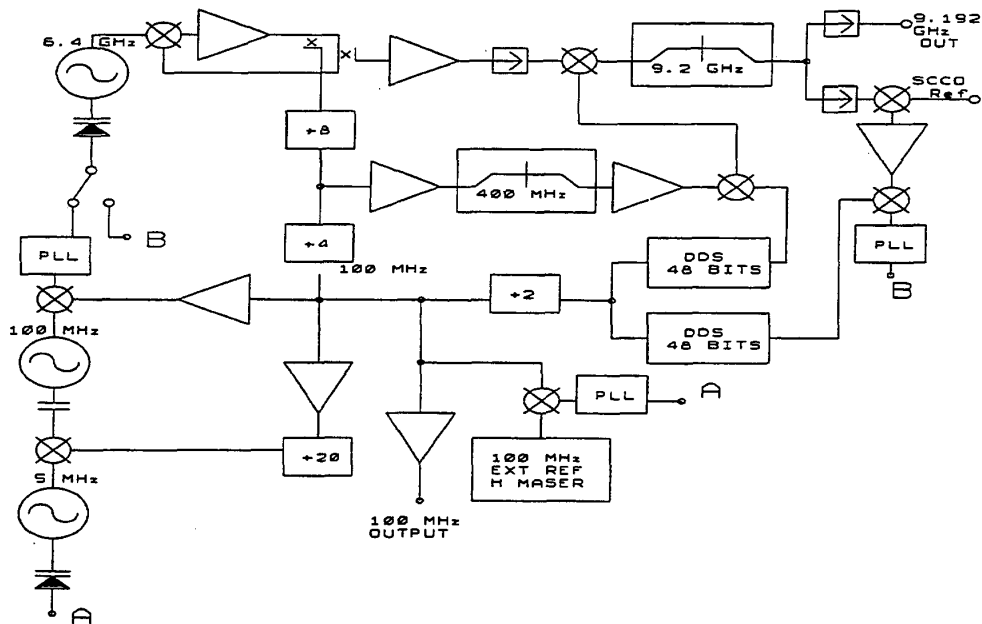


Figure 1. Block diagram of the new Cs frequency synthesizer.

can be switched to a new value without phase discontinuity in less than  $1 \mu\text{s}$ . The frequency is nominally set at 7.368 MHz and mixed with the 400 MHz from the binary divider using a simple upper sideband (USB) mixer, which gives more than 25 dB rejection at the carrier and lower sidebands. Additional suppression of these spurs could be obtained with further design refinements. The 407.368 MHz signal is mixed with the 9.6 GHz output of the regenerative divider to produce the 9.192 GHz signal, which is amplified and passed through a broadband filter and isolator to provide the final microwave output of the synthesizer.

As in our earlier synthesizer designs [4, 5], a 5 MHz oscillator controls the PM noise for Fourier frequency offsets up to approximately 50 Hz while a 100 MHz oscillator controls the range from 50 Hz to 50 kHz.

The synthesizer output can be steered by voltage control of the 5 MHz oscillator using a DC error signal. This voltage control could be derived from the physics package of a Cs clock. The 100 MHz output from the synthesizer also drives a mixer, which can be used to detect the phase difference between the 100 MHz signal from a hydrogen maser or other high stability reference. This mixer output can be used to phase-lock the 5 MHz to this reference with a loop bandwidth of approximately 1 Hz. The low bandwidth was chosen to exclude spurs due to ground loops and

pickup of electromagnetic interference. There is also a provision to phase lock the synthesizer to a microwave reference such as a super conducting cavity oscillator (SCCO) as long as the frequency is within  $\pm 20$  MHz of one of the internal reference frequencies (3.2 GHz, 6.4 GHz, 9.192 GHz, 9.6 GHz, 10.007 GHz). To achieve this we use another phase-locked-loop (PLL) with a second DDS set to the difference between the internal reference frequency and that of the SCCO. The output error of this PLL could correct the 6.4 GHz DRO with a bandwidth of up to approximately 300 kHz. It would also be possible to add an additional mixing stage to use a stable reference at the Rb hyperfine frequency of 6.834 GHz [12].

We constructed two prototype synthesizers of the above design. The mechanical assembly consisted of five interconnected modules with machined aluminum cases of 6 mm wall thickness. These were stacked tightly together with heat sink fins on two outer sides of the assembly. All circuitry, including the DDS, used surface mounted components that were heat sunk to the printed circuit boards. The printed circuit boards in turn were heat sunk to the aluminum cases by mounting them flush against the bottom with thermal conductive film. In addition, metal straps connected the top of the few integrated circuits that dissipated significant heat to the sidewalls. The entire microwave portion of the circuit was assembled in one module with the components mounted flush against the walls or the bottom. Thus most of the heat dissipated in the synthesizer had a direct conduction path to the external heat sinks. In

some applications the heat sinks could be removed and the assembly mounted to a thermally stabilized base plate. The unit is very compact and quite robust. The total size of the each unit, excluding the external power supply and the removable heat sinks was 22 cm x 13 cm x 18 cm. The volume could be reduced by roughly 40 % by simply repackaging the present subassemblies. The total power consumption was approximately 22 W at 24°C. Although no quantitative vibration tests have yet been performed, many strong bumps, including the customary 10 cm drop test, produced no noticeable effects.

### 3. RESULTS AND DISCUSSION

In this section we describe results of tests made on the two units described above. Extensive studies were made of the spurs and of the PM and AM noise.

Figure 2 shows that there are no spurs within  $\pm 2.5$  MHz of the 9.192 GHz output greater than -75 dBc. PM noise measurements were performed on the 100 MHz output using a three-cornered-hat method involving two of the present synthesizers and one of the earlier types [4]. The results are summarized in Fig 3. Also shown for comparison are the results from earlier designs [4, 5]. The results of measurements of AM noise and spurs at the microwave output are also very similar to those obtained with the earlier NIST synthesizers. These results indicate that frequency pulling by spectral impurities is of little consequence to present slow beam or fountain frequency standards [4].

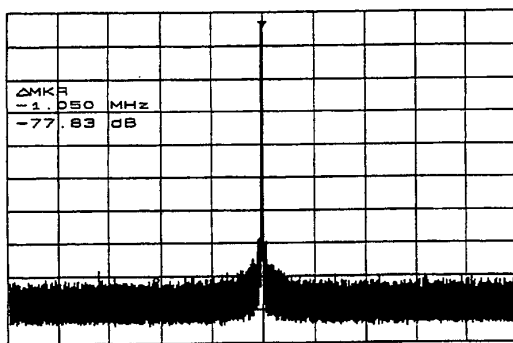


Figure 2. Microwave power spectrum of the 9.192 GHz output from the new Cs synthesizer. The span is 5 MHz and the resolution bandwidth is 1 kHz.

The set up shown in Fig 4 was used to study the phase stability with respect to environmental temperature variation between the microwave output and the user output at 100 MHz. The microwave outputs of the two synthesizers were phase locked and the 100 MHz outputs were used to drive a phase comparator and data

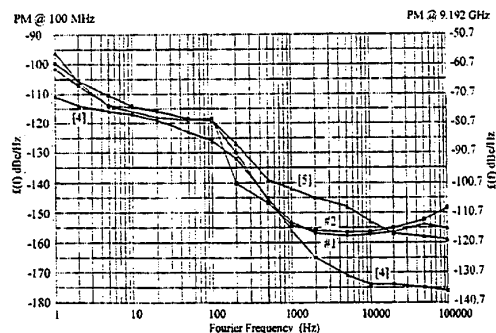


Figure 3. Comparison of the PM noise spectrum of the new Cs synthesizer #1 and #2 to previous designs [4] and [5].

logger. The temperature of one of the synthesizers was kept constant while that of the other was varied. Figures 5a and 5b show typical initial result of such temperature cycling from which we compute a temperature coefficient of 2.2 ps/°C. An important

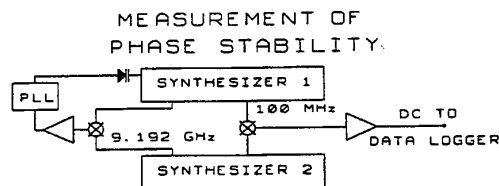


Figure 4. Block diagram of setup used to measure the phase stability.

point was that the temperature coefficient was almost identical for the two units and that there was less than a minute delay and almost no hysteresis between the temperature and phase variations. The reason for this is that all the components of are thermally very well connected to the case. Further investigations revealed that the major part of the temperature coefficient arose from the last frequency divider and the output isolation amplifier. A very simple circuit comprised of a thermistor (heat sunk to the inside of the case containing the divider and the output amplifier) and a varactor to change the phase delay at the output of the 100 MHz in response to the temperature variations was successfully used to compensate most of the temperature coefficient. With several trials of scaling the variation of the voltage across the varactor, we were able to obtain a temperature coefficient of less than 0.2 ps/K as shown in Fig. 5c. In subsequent tests we obtained a very highly phase stable 100 MHz output as shown for a 4 day stretch during which room temperature varied by approximately  $\pm 0.5$ °C (see Fig. 6). Finally, we show in Fig 7 a typical plot of internal

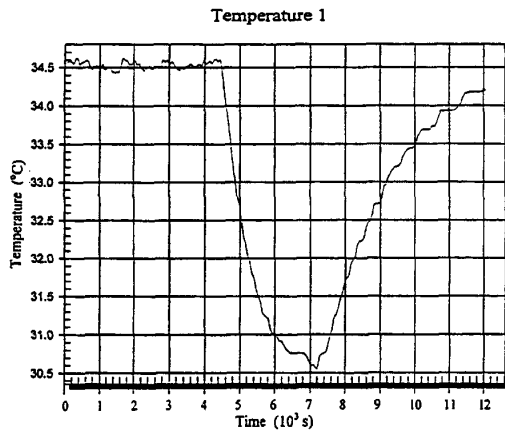


Figure 5a. Temperature change of synthesizer # 1.

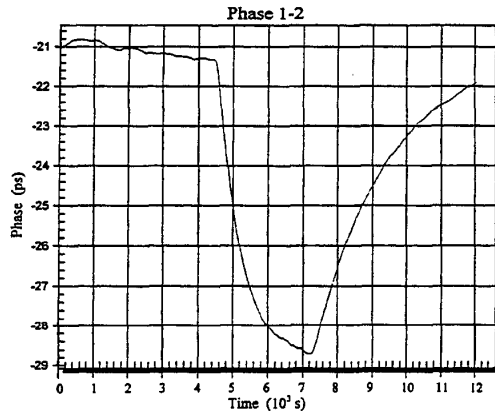


Figure 5b. Initial uncompensated phase response of synthesizer #1.

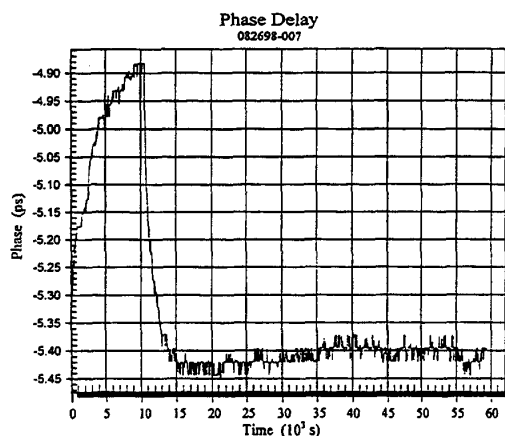


Figure 5c. Compensated phase response of synthesizer #2 for a temperature stepup and back of 3.5 °C.

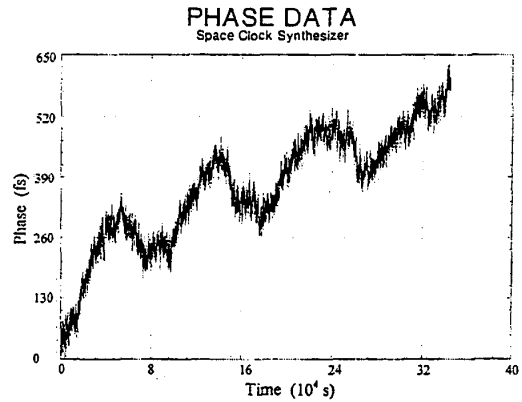


Figure 6. Phase change between two synthesizers over 4 days.

frequency stability, obtained by processing the phase data with sampling times from 5 s up to 1 d. We obtain a fractional frequency stability Allan deviation of  $1 \times 10^{-15}$  at 10 s and  $1 \times 10^{-18}$  at 1 d. The 1 d frequency stability is a significant improvement over stability results reported for previous designs.

#### 4. CONCLUSION

We have described a novel approach for synthesizing the microwave signal for a Cs standard. The realization of the design is quite simple, requiring no frequency multiplication or narrow band filters. Two prototype synthesizers were fabricated keeping in mind the proposed use in space and hence taking special care to ensure that all the components could eventually be obtained in space qualified versions. We also ensured that most components were heat sunk by thermal conduction to the case. This led to a very simple but effective means of compensating the temperature coefficient to lower than  $0.2 \text{ ps}/^\circ\text{C}$ , and consequently obtaining internal frequency stability that reached  $1 \times 10^{-18}$  at 1 d. Another feature of the present design, the ability to set the microwave output with a resolution of  $2 \times 10^{-17}$  is due to the use of a 48 bit DDS. Since there is no PLL in the final microwave synthesis, the phase excursions after switching frequency are small and the settling time is less than  $1 \mu\text{s}$ . Yet another feature of the synthesizer is the provision for phase locking to an SCCO which is trimmed within 20 MHz of one of the internal reference frequencies (3.2 GHz, 6.4 GHz, 9.192 GHz, 9.6 GHz, 10.007 GHz), providing for a much superior PM noise and short-term frequency stability than is possible using quartz oscillators.

Although the present synthesizers are already very robust, compact, and consume low power, we

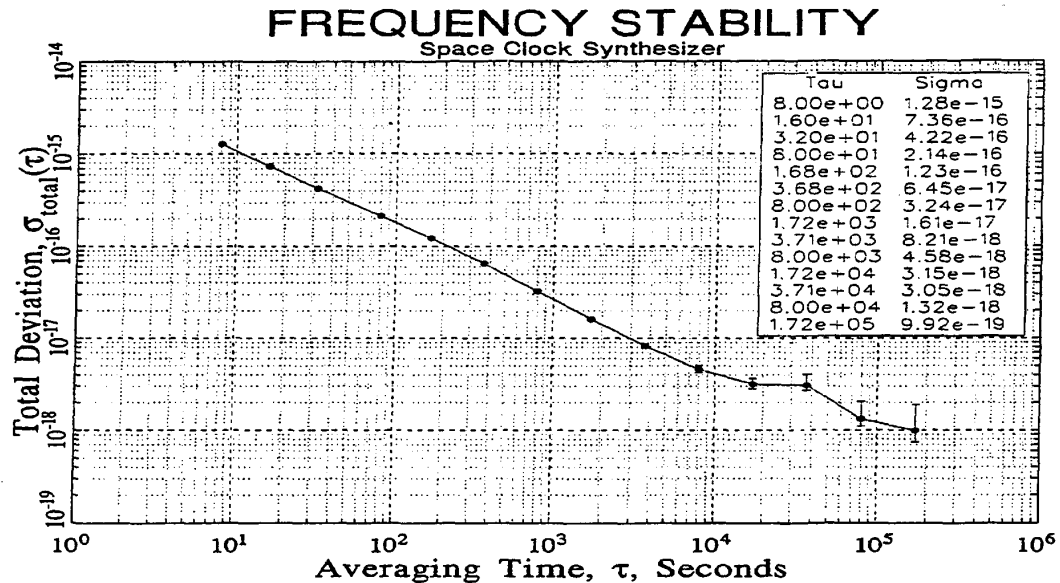


Figure 7. Allan deviation for a pair of Cs synthesizers computed using total deviation and the data of Figure 6.

estimate that further optimization should lead to a 70 % reduction in size and a 50 % reduction in power consumption. Finally, although our present focus has been to synthesize the Cs hyperfine frequency, this approach could be adapted to produce similar performance at many other frequencies of interest (for example, the Rb frequency).

#### 5. ACKNOWLEDGEMENTS

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