1998 IEEE INTERNATIONAL FREQUENCY CONTROL SYMPOSIUM

PREDICTING 1/f AM AND PM NOISE IN Si BJT AMPLIFIERS: A New Computer Program

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Abstract - We show that a high-resolution software package can be adapted to calculate the amplitude modulation (AM) and phase modulation (PM) noise performance of Si Bipolar Junction Transistor (BJT) amplifiers. Our simulations predict that the PM noise induced by bias current noise can be greatly suppressed by operating at special bias conditions. Furthermore, a dc balance amplifier circuit is introduced to stabilize the base-to-collector voltage. The total sensitivity of PM noise to power supply noise using dc balance architecture can be reduced by 40 dB compared to basic amplifier architecture. This is experimentally verified.

I. Introduction

It has been previously shown that 1/f AM and PM noise in amplifiers originates from 1/f baseband noise in the DC operating point, i.e. bias current, bias voltage, active gain element as well as circuit components [1,2]. This work was based on analytical calculations of a simplified small-signal model of a Si bipolar junction transistor (BJT) and by extensive experimental measurements [1,2].

The up-conversion of baseband noise in the operating parameters of the amplifier can be conveniently characterized by sensitivity coefficients. These coefficients have the form of

$$L(f) = \frac{1}{2}[K_{Ic}^{PM}(f)]^2 \frac{1}{Ic^2} PSD[Ic(f)],$$

where L(f) is the single side band PM noise of the amplifier; PSD[Ic(f)] is the power spectral density of the changes in Ic as a function of Fourier frequency f, and $(K_{Ic}^{PM})^2$ is the PM noise sensitivity to Ic current noise: $K_{Ic}^{PM}(f) = Ic\frac{\delta\phi(f)}{\delta Ic}$. For simplicity, $(K_{Ic}^{PM})^2$ is denoted as PM~Ic. Similar coefficients can be defined for AM noise.

The analytical calculations of [1,2] indicated the general trends in the sensitivity coefficients for PM and AM noise with changes in parameters such as the dc base-to-collector voltage Vcb and dc collector current Ic. This work provided insight as to the major processes. It was however impractical to perform these analytical calculations with a realistic model of a BJT transistor. Experimentally it is difficult to change the operating point with high resolution to search for sharp resonance in the sensitivity of the PM and AM noise to noise in a particular operating parameter.

Although it is clearly much easier to manipulate different circuit parameters by software simulation, most computer-aided-design (CAD) programs for circuit analysis do not have sufficient resolution to detect the small noise modulation of the signal amplitude and phase that yield AM and PM noise. We have found that this can be overcome by using a CAD program to calculate the sensitivity functions by simulating the dc parameters with a resolution of 1×10^{-6}. This allows one to carefully analyze the PM and AM performance of an amplifier in the presence of baseband fluctuation in virtually any parameter. The program also allows one to enter a model for the active elements or to edit their model. In the following we explain some of our results using a traditional hybrid pi model of a Si BJT in several common-emitter amplifiers.

II. Common-Emitter Amplifiers

In this section, we describe three different designs of common emitter (CE) amplifiers. The first two circuits have been described in the literature before and are mentioned here for reference purposes [1,2]. The third circuit, a configuration with dc voltage balance, is the circuit used in our simulations and experimental measurements, to be presented in section III.

II.1 Basic Common-Emitter Amplifier Circuit

Figure 1 shows the circuit diagram of a basic CE amplifier. This configuration is widely used in commercial BJT amplifiers. It has a fairly high gain, but its AM and PM noise are generally high when compared to other designs (to be discussed later).

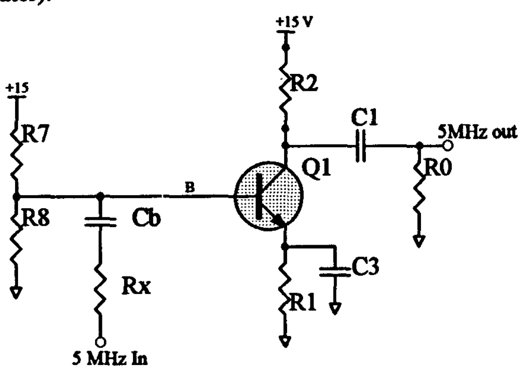

Figure 1. Basic CE amplifier circuit

II.2 Common-Emitter Amplifier with Low AM and PM noise

It has long been known that the PM noise of a CE amplifier could be reduced if an un-bypassed resistor is added to the emitter leg of the amplifier [3,4]. Nevertheless, the reason for this improvement was not understood. In addition most everyone, except [5], assumed the AM noise in amplifiers was negligible. The work of [1,2] was the first in the western literature to provide insight on the up-conversion of low-frequency noise into AM and PM noise and on the reasons for the improvements in PM noise with Re (un-bypassed emitter resistor). Considerable work on this and related configurations has been done at the Moscow Power Engineering Institute and their work is now available to western readers [6-7].

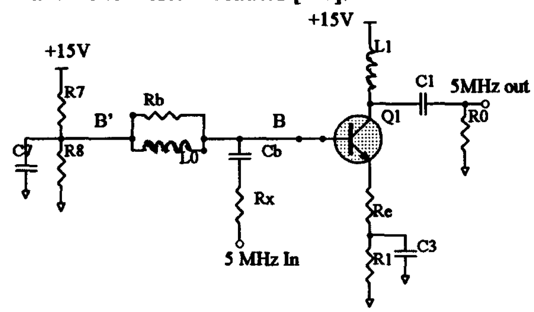

Figure 2. Improved CE amplifier circuit with added un-bypassed Re

Figure 2 shows an improved CE amplifier with an added un-bypassed resistor Re. A large inductor is used in place of the collector resistor, making the dc gain approximately 0. This is done to minimize the voltage fluctuations at the collector terminal. Filtering capacitors are added throughout the dc bias resistor ladder, including a large capacitor at point B'. Since point B' is a rf ground, a resistor and large inductor (in parallel) are added between points B and B' to provide an impedance between base and ground. The inductor (L_0) provides a near short circuit to ground for baseband frequencies, which helps minimize the voltage noise at the base terminal. Resistor (Rb) provides the termination for the rf input. The CAD simulation applied to this configuration generally matches the results of [1,2]. We have however discovered in the simulation that there exist special values of Ic and Re that yield a deep notch in the value of $K_{I_c}^{PM}$. This result was not apparent in [1,2] because the base-emitter capacitance was neglected. The effect is shown in [6,7].

II.3 DC-Balance Amplifier Circuit And Vcb Noise Control

If the CE circuit of Fig.2 is operated at the notch in the $K_{I_c}^{PM}$ value, the Vcb voltage noise will become the most significant contribution to added PM noise. Figure 3 shows a circuit diagram of a CE amplifier where the bias voltage and DC gain have been carefully chosen to minimize the fluctuation in Vcb due to changes in V+.

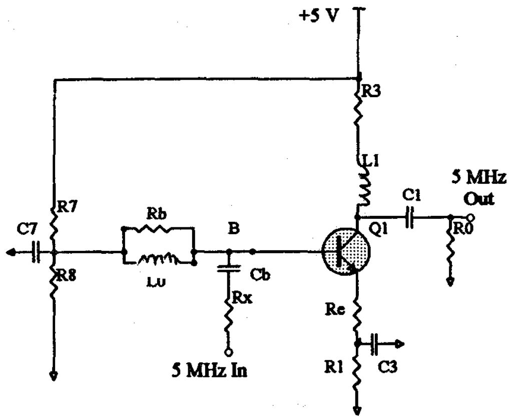

Figure 3. CE amplifier circuit with DC-balance for Vcb.

In Fig. 3, the same power supply V+ is used to bias the base and collector of the transistor. To achieve collector-base voltage balance (ΔVcb ≈ 0), the resistors in the circuit are chosen according to

$$\frac{R3}{\mathrm{Re}+R1}=\frac{R7}{R8},$$

which yields: $V_{CB} = 0.7\,R3 / (\mathrm{Re} + R1)$.

There is no filtering of the base voltage noise ΔVb, and thus a current noise component due to fluctuations in the base current, which is absent in Fig.2, is introduced in the circuit.

III. Simulations and Measurements

In this section we describe the simulation conditions and the measurement systems used. The results of the simulation and the experimental measurements are presented.

III.1 Simulation Setup

We used our new high-resolution software to simulate the voltage-balance CE amplifier in Fig. 4. The AM and PM sensitivities to current and voltage noise were computed using the magnitude and phase of the gain obtained from the simulation.

The voltage noise ΔVcb was simulated by changing the dc bias voltage V+ by a small amount. The relative changes (ΔA/A, Δϕ) of the amplitude and phase of the gain were monitored and compared to the relative change of the DC voltage. The AM sensitivity to ΔVcb (AM~Vcb) was found by computing the ratio of the relative change of the gain amplitude to the relative change of Vcb. PM~Vcb sensitivity was obtained in a similar way.

The noise in the collector current Ic was simulated by adding a DC current source Ie paralleled with bypassed emitter resistor R1. (See Fig. 4.) Ie was set to be small compared to Ic. The relative change of Ic was used to find PM~Ic and AM~Ic.

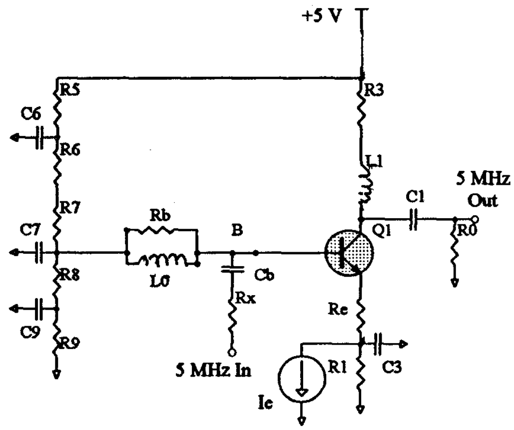

Figure 4 Simulation setup with current source Ie as current noise

III.2 Measurement Setup

Figure 5 shows the setup used to measure sensitivities to current and voltage noise. The measurements were made at a carrier frequency of 5 MHz and at a dc supply of +5V. The AM noise and PM noise of the amplifiers were measured using the NIST noise detection system [8].

To investigate the sensitivity to current fluctuations, we injected a 10 Hz sine wave into Re. This injected signal was measured and compared to the PM/AM measured at 10 Hz. The sensitivities PM~Ic and AM~Ic were obtained from these measurements.

To investigate the sensitivity to voltage fluctuations, we injected a 10 Hz sine wave at V+. This injected signal was measured and compared to the PM/AM measured at 10 Hz. The sensitivities PM~Vcb and AM~Vcb were obtained from these measurements. When a DC balance architecture is used, some adjustment of R3 is necessary to minimize the 10 Hz signal at Vcb.

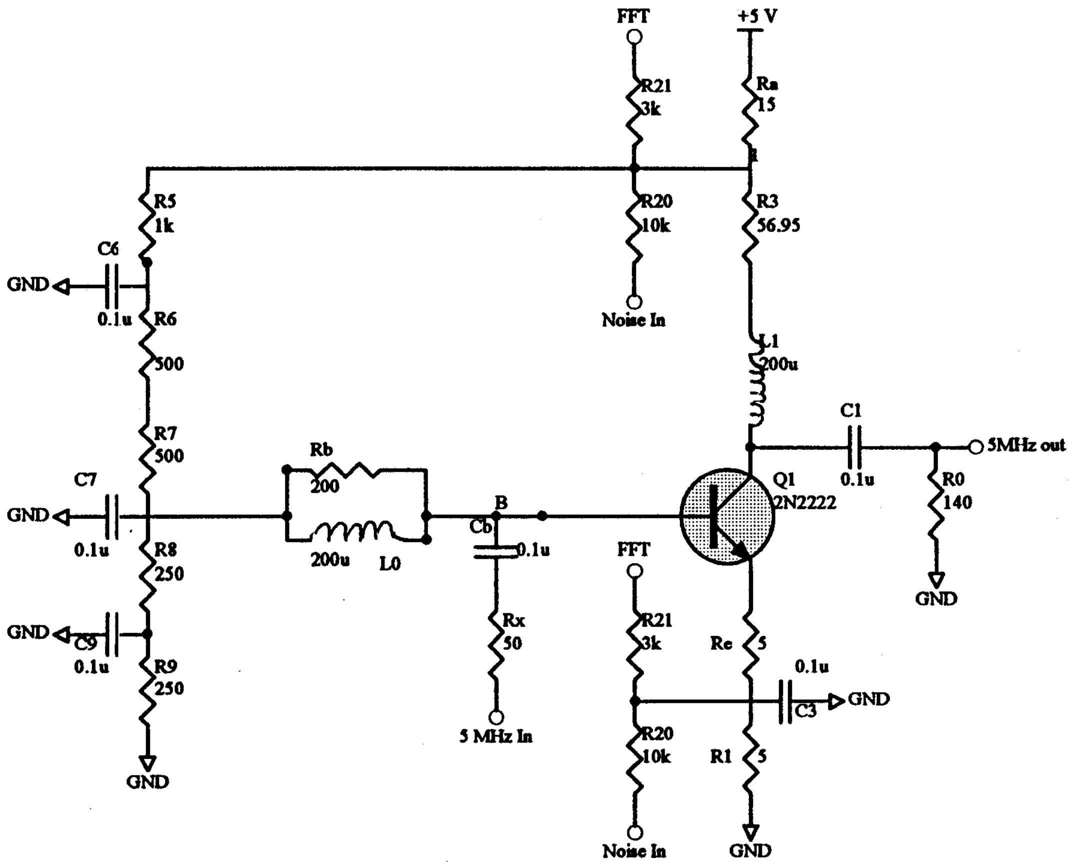

Figure 5 Sensitivity measurement setup

III.3 Results

Figure 6 shows experimental measurements of baseband voltage and current noise when using the dc voltage balance configuration. The injected noise at V+ is about -65 dB relative to the 5 V supply. The resulting Ic noise is -68 dB relative to the collector current Ic. The noise on Vcb with dc balance is about -99 dB relative to the base-collector voltage Vcb. The Vcb noise in this DC balance architecture has been reduced by more than 30 dB compared to the noise in the basic amplifier architecture.

Measurements and simulations were made to study AM and PM sensitivity changes with the unbypassed emitter resistor Re. Re was swept from 0 to 10 Ohms. To maintain the same dc bias and Ie, R1 was also adjusted to provide (Re + R1) = constant.

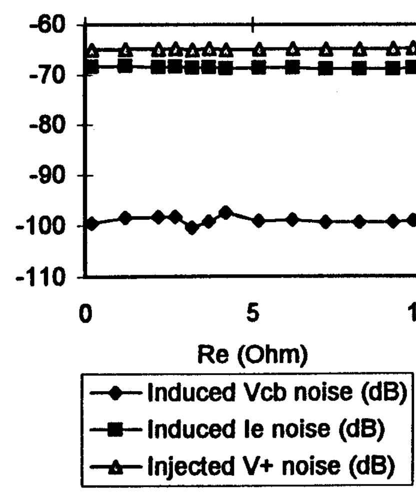

Figure 6. Baseband current and voltage noise of the DC balance circuit

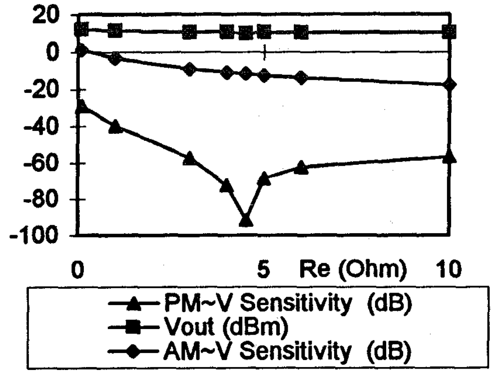

Figure 7. Simulation results for the PM and AM sensitivity to V+ noise (V+ = 5 V, Ie = 27 mA, Cjc=12.213pF, Cje=32.01 pF)

Figures 7 and 8 present the results of the simulations and measurements for the dc-balance architecture shown in Fig. 5. As the gain of the amplifier decreased with increasing Re, the input power was adjusted so that the output power remained at 10 dBm. This was done both in simulation and in the measurements. A notch in the sensitivity of PM~V+ was found around Re = 4 Ohm, both in the simulation and in the measurements, which is about 40 dB below the PM~V+ sensitivity in the basic amplifier architecture (Re =0). The Re value for the notch was similar in both cases, closer agreement for the position vs. Re can be obtained by adjusting the base-collector capacitance (Cjc) and base-emitter capacitance (Cje) parameters in the BJT model of the CAD program. The notch would probably be deeper if we had taken smaller steps for Re.

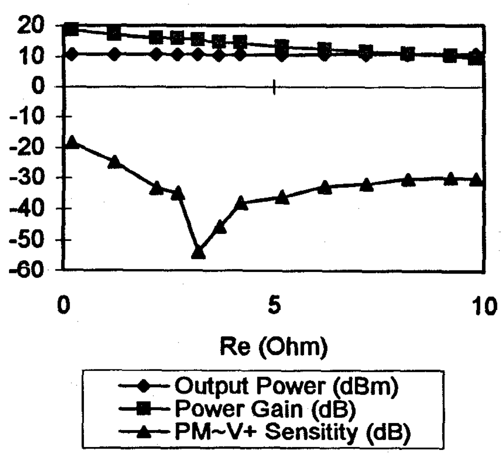

Figure 8. Experimental measurement results for the PM sensitivity to V+ noise

IV. Conclusion

We have shown that high-resolution simulation software can be used to predict the AM and PM sensitivities to voltage and current noise of amplifiers both qualitatively and quantitatively. Using this software we have shown that the collector-base voltage fluctuation due to fluctuation in the power supply can be reduced by more than 30 dB as compared to typical bias configurations by choosing appropriate bias parameters. These simulation predictions were confirmed experimentally. The software also predicted a notch of more than 40 dB in the PM sensitivity to power supply noise, which was confirmed by experimental measurements. Base-collector capacitor and base-emitter capacitor in the BJT model should be carefully matched to the actual values in order to obtain the Re at which the notch occurs.

The techniques used in our simulation can be applied to other circuit simulation programs to predict AM and PM sensitivities and to determine the dc parameters. The primary requirement for the software is that it determines the phase and amplitude to a resolution of at least 10^{-6}.

Acknowledgments

We thank V.N. Kuleshov and A. Sen Gupta for fruitful discussions on this topic.

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