The 5ns Peaking Time Transimpedance Front End Amplifier for the Silicon Pixel Detector in the NA62 GigaTracker

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***Abstract*—We present the design and test results of a front-end prototype circuit developed in 130 nm CMOS technology for the readout of the Gigatracker pixel detector experiment in NA62 at CERN. The main challenges for the front end amplifier are very high signal hit rate (dead time less than 100ns, average signal rate 100 kHz) and 100 ps timing resolution combined with the level of affordable power consumption (< 2W/cm^2) and noise (< 200 e$^-$ENC). The predicted ENC levels for the nominal detector capacitance of 250 fF and maximum leakage current of the order of 20 nA are below 200 e$^-$. The overall power consumed by the analogue and digital part of the pixel cell is in the order of 130 μW. The optimization of the design as well as test results of the prototype front end chip are evaluated and discussed.**

I. Introduction

NA62 experiment [1], [2] at the CERN SPS accelerator will be used to study the very rare decay of the charged K meson into a pion and neutrino-antineutrino pair. Beam particles with a momentum of a narrow momentum band of 75 GeV/c $\pm$1.2%. Only 6 % of beam particles are kaons, which are the subject of study. To study the momentum of the kaon, the beam is bent using four magnets in the GigaTracker (GTK), see Fig. 2 for a general layout of the experiment, as well as the location of NA62 within it. The GTK is composed of three tracker stations of hybrid silicon sensor modules cover a sensitive area of 60 $\times$ 27 mm^2 each, with a pixel size is 300 $\times$ 300 μm^2. The GTK measures the beam particle trajectory with an rms space resolution of 100 μm and a momentum resolution of 0.5 %. The SPS beam line is a continuous beam with an average particle rate of 800 MHz with a rate in the beam center of 140 kHz per pixel. To allow an effective reconstruction of the tracks in the entire experiment and to limit the inefficiency of the tracking correlation to less then 1 %, a time resolution of 200 ps in the GTK and 250 ps in each station is required and the electronics are specified to resolve the arrival time with a 100 ps binning of the time-to-digital converter. Prototype pixel ASIC has been designed for GTK detector at the NA62 experiment at CERN and is being tested now.

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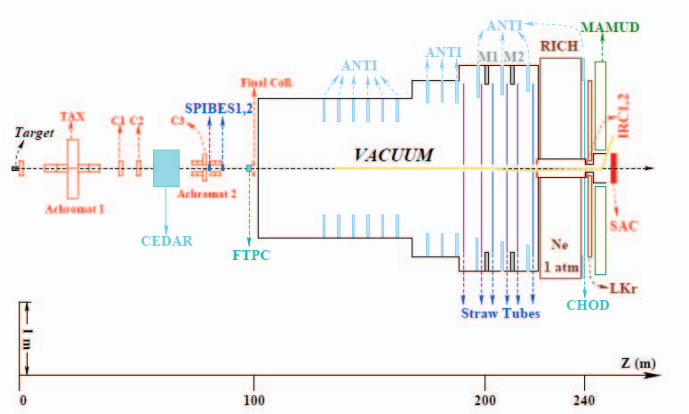

Fig. 1: Overall beam and detector layout for the NA62 experiment

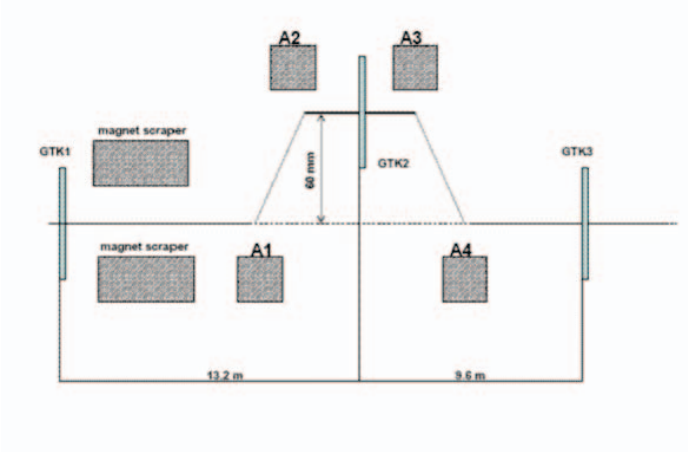

Fig. 2: Layout of the three station that are present in the GigaTracker, and the A1-A4: dipole magnets to provide the momentum selection and recombination

In this paper, Section II presents the details of the GTK detector characteristics, with detailed explanation on the two options for readout prototypes that are presented in Section II-A. The next Section III introduces the general architecture that has been designed using the End Of Column architecture, explaining both the analog pixel circuitry in Subsection III-A, as well as the End Of Column peripheral circuitry in Subsection III-B. The next Section IV presents the results obtained from measurements on the analog pixel circuitry.

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II. The GigaTracker prototypes for the NA62 experiment

The GTK detector modules will be developed using bump bonded hybrid pixel detector assemblies. This technological approach, rather than a monolithic development, present advantages such as better speed performance at the read-out ASIC, which is one of the most demanding requirements. In addition to this specification, the need for low material budget ($< 0.5\%$ for a radiation length X_0), short sensor charge collection time and acceptable amplitude, has defined a sensor thickness of 200 μm, with a read-out chip thickness of 100 μm[3].

The radiation environment expected for the GTK shows very high intensity and non-uniform hadron beam, with an intensity up to 140 kHz/pixel in the center. The radiation dose expected in the readout chip and wire bonding is low, because they are located outside the active area, and ionizing radiation. The presence of the wire bonding will not influence the particle trajectory, because they will be located outside the beam profile.

One GTK station has a total of 18000 pixels processed by 2 rows of 5 readout chips, each one of them has 45 rows $\times$ 40 columns. To correlate the particle hit information in the GTK and in the detector further downstream in the NA62 experiment, given the particle rate of 800 MHz a time resolution of 250 ps RMS is needed in the GTK so that a correct hit correlation can be performed in 99 % of particle hits. For the development, a maximum dissipation of 2W/cm^2 has been estimated for the pixel chips, yielding a maximum power dissipation of 32 W for one station.

The electronic charge delivered to the pixel front-end electronics is expected to be between 5000 and 60000 electrons, corresponding to between 0.8 fC and 10 fC. Taking into account that the full system needs to deliver at least a time resolution of 250 ps RMS. The design parameter for the pixel chip time-to-digital converter (TDC) time binning was set to 100 ps. Time walk affects the obtained results, generating different arrival times for different input signals. This effect can be compensated using different techniques, such as measuring the amplitude peak, measuring the time where the signal exceeds a single threshold or using constant fraction discriminators.

The total radiation dose on the stations within 100 days of operation is expected to be 10^5 Gray with a 1 GeV neutron equivalent flux of $2 \cdot 10^4$ cm^{-2}·s^{-1}. The sensor material has been selected as p-in-n material, which although known for relative good radiation resistivity, will degrade within 100 days of operation due to this dose.

For each particle hit, the position address and the arrival time is determined and needs to be sent to the off-detector electronics. Up to 32 bits are reserved for the hit transmission. The address of each pixel is given by 11 bits whereas the time information and hit quality information is sent with up to 21 bits. In the beam center each chip receives a hit rate of 132 MHz. This corresponds to a data rate of 4.2 Gbit/s. In order to account for statistical fluctuations the design data rate has been set to 6 Gbit/s. The hit information data will be sent directly out of the chip (triggerless architecture) as on-chip processing is considered impractical [4]. The data volume accumulated during on chip-processing time would be too high to be stored on the chip.

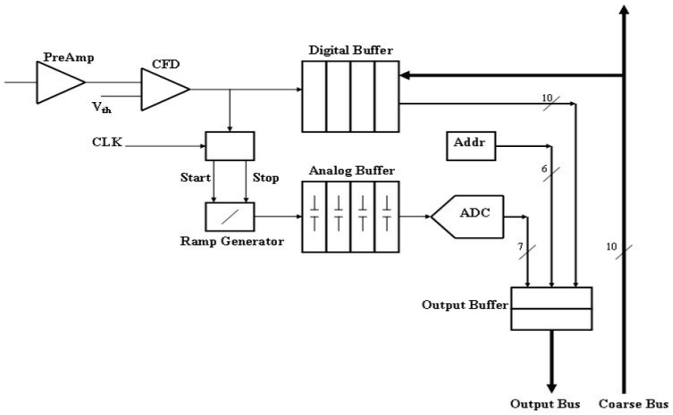

Fig. 3: Pixel building blocks for the on-pixel TDC pixel option

A. Two architectural solutions for the GigaTracker readout chip

Prototype read-out chips had to face severe specifications that are related to the elevated presence of high speed digital circuitry close to the sensitive analog circuitry at the pixel level. Another problem that have to be faced for this design, is the extremely precise time measurement, necessary to perform time walk compensation. To develop these read-out chips, two different approaches have been considered [5] and have been fabricated using 130nm CMOS technology.

The first solution considered is based on discriminating the analog signal and transmitting the result to the perifery, where an end-of-column (EOC) circuitry measures the leading and trailing edge timing. This approach has the advantage of separating the analog and digital signals, and that there is no need to transmit high precision clocks and readout arbitration signals throughout the pixel array. The only signals that have to be transmitted through the matrix are the results obtained from the discriminator, eliminating the need of in pixel buffering.

The second solution measures the arrival time at each single pixel cell and transmits the digital word obtained from each of the pixels to the periphery of the chip [6] based on a dual edge Wilkinson architecture. The success of this approach is based on the use of a jitter-free clock distributed to each of the pixels. In this aproach digital and analog circuitry is close and the crosstalk has to be studied. This solution studies the time walk compensation with two

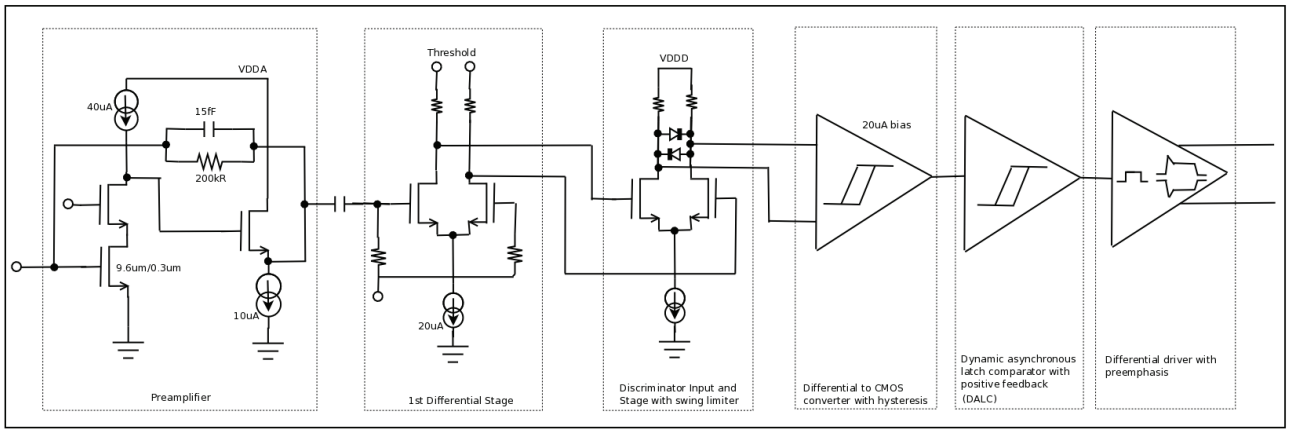

Fig. 4: Pixel cell representation as functional blocks.

approaches, see Fig. 3 for a schematic representation. The first uses a constant fraction discriminator (CFD). It measures the time of the zero crossing of the difference between the original input signal and a delayed and attenuated copy of the input signal. The second approach is the measurement of the time-over-threshold, where a single threshold is used. The comparison of the two methods shows that CFD measure one time value, reducing the data flow, but shows a higher power consumption and compensation quality depends on the input signal shape. Considering these two different approaches, two demonstrator ASICs, one for each of the two basic architectural approaches have been designed in 130 nm technology, and the one presented here correspond to the one EOC circuitry per pixel matrix.

III. General Architecture of the EOC Prototype

The required timing precision and high hit rate impose the use of a fast transimpedance amplifier with a very short peaking time, limiting the time walk of the comparator. The lower limit for the value of the peaking time is determined by the achievable charge collection time from the Silicon detector. Although the thinning of the detector down to 200 μm minimizes the charge collection time, the optimum value of the peaking time for the shaper is around 5 ns taking into account the signal speed in the sensor.

The pixel prototype architecture presented here employs the time over threshold time walk compensation technique. The demonstrator contains one full 45 pixel column which, in order to save silicon area, is folded back on itself. In addition to this column, test structures have been included for the characterization of the analog pixel cell. In the next subsections the architecture corresponding to the pixel is presented in Section III-A and the End Of Column circuitry is introduced in Section III-B .

A. Architecture of the NA62 pixel prototype

The pixel cell is formed by 7 functional blocks, that can be summarized as a transimpedance preamplifier, a first differential post amplifier, a first stage of the discriminator, a second stage of the discriminator with hysteresis, a dynamic asynchronous latch comparator with transitional positive feedback, a differential transmission line current driver with pre-emphasis and a coplanar transmission line.

The first 6 functional blocks are represented in Fig. 4, the transmission line is not included here. The preamplifier is built with the cascode amplifier with an NMOS input transistor of dimensions 9.6 μm width and 300 nm length with a simple resistive and capacitive feedback defining the pulse gain at the level of 30 mV/fC. The dimensions of the input transistor were optimized for the detector capacitance of 250fF. The low value of the input capacitance allows the use of a simple cascode stage offering very high bandwidth (1 GHz gain bandwidth product) at very affordable power consumption (60 μW). The rather moderate open loop gain is in the range of 45 dB, the input impedance of the preamplifier stays in the range of 1 to 2 kΩ for 1 GHz bandwidth, which is sufficiently low to provide the efficient charge collection from the detector. Crosstalk between neighboring pixels is expected to be less than 4 %.

The first differential pair translates the external differential threshold voltage V_{T1}-V_{T2} for the internal threshold of the comparator. The fully differential structure of the comparator provides very good rejection of common mode noise from the digital power supply and good threshold uniformity. The entire preamplifier-shaper circuit has a gain of 70 mV/fC. The overall shaping function of the preamplifier and shaper is equivalent to CR-RC3 with the peaking time around 5.5 ns.

The following 3 stages of the comparator provide high sensitivity together with very high speed at a reasonable power (50 μW). The simulated time jitter (transient noise simulation) of the full front end stimulated with 3 fC signal is in the order of 30 ps RMS which agrees well with the predicted ENC values, shown in Fig 5. These simulation results show that for a detector capacitance of 250fF the predicted ENC will be below 200e^-.

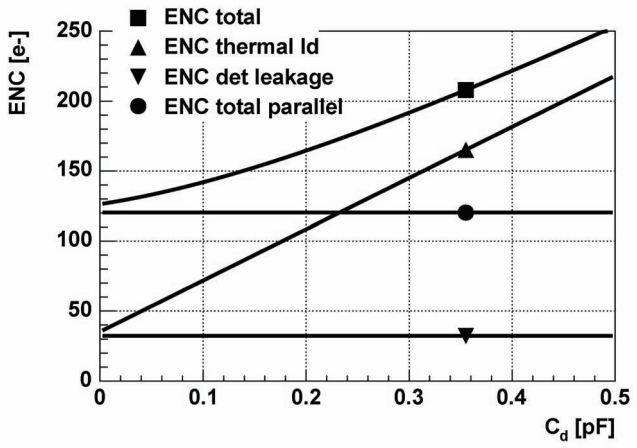

Fig. 5: ENC noise as a function of input capacitance for the 20 nA maximum detector leakage current.

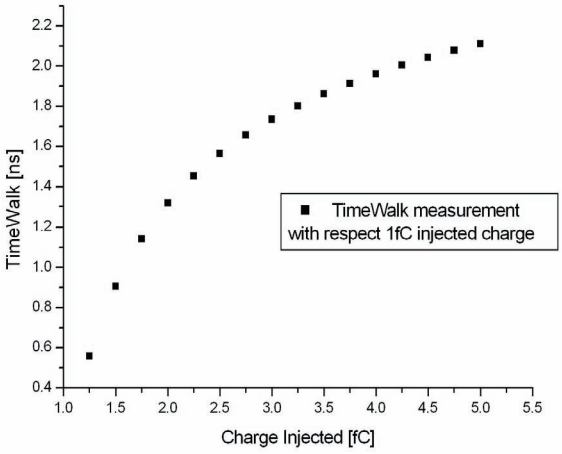

Fig. 6: Simulation results obtained for the time walk with respect to a 1fC injected charge at room temperature.

The next simulations that have been done correspond to the time walk and time over threshold calculations with a detector capacitance value of $\sim$ 250fF. This value show that time walk expected values present a maximum of $\sim$2.1ns for a maximum injected charge of 5.25fC (see Fig. 6). The simulation results obtained for the time over threshold values vary from a $\sim$8.45ns for an input injected charge of 1fC to a maximum of $\sim$14.4ns for a maximum injected charge of 5fC, as seen in Fig. 7.

B. Architecture of the Read Out for the NA62 pixel prototype

The transmission of the fast data that is generated with the current driver is done using differential transmission lines. The traditional use of CMOS inverters as repeaters stages cannot be used because they introduce delays that scale linearly with the wire capacitance and hence the wire length, also the big CMOS swing is an issue that limits the transmission speed, making it not the most suitable option.

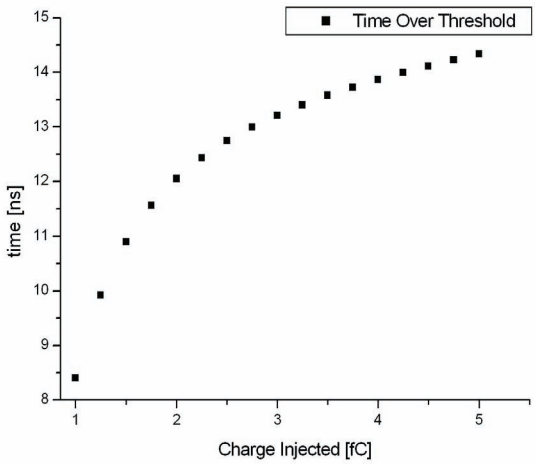

Fig. 7: Simulation results obtained for the time over threshold at room temperature.

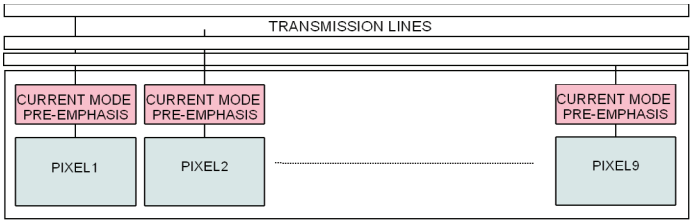

Fig. 8: Schematic of the transmission line use for a number of 9 pixel cells.

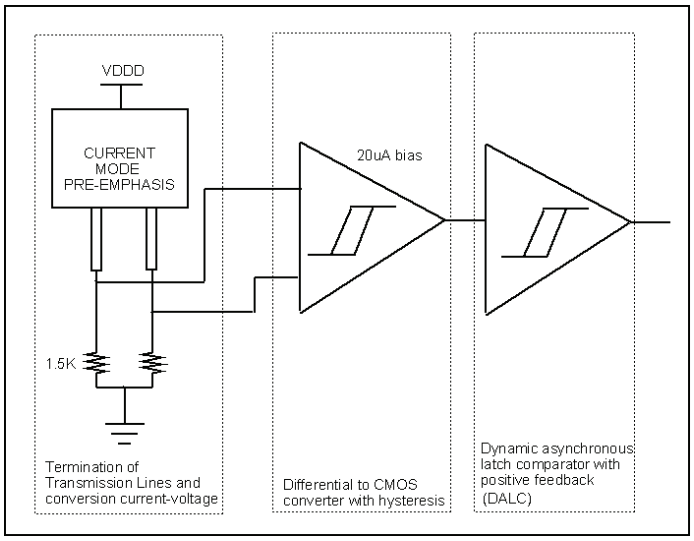

Fig. 9: Schematic of the Transmission Line receiver.

The use of a transmission lines assures that there is an attenuation on the resistive energy losses. The high frequency components of the signal travel more quickly than the low frequency, making the line RC limited. Other solutions that have been used before are low swing differential buses[7], or current mode signaling[8].

The approach that has been adopted connects each driver to a transmission line, up to a total of 45 to avoid pile up for the data/address lines, see Fig 8. The differential driver switches a current source with a value of 100μA when a hit occurs. The differential signal is transported in a cross-coupled transmission line, at a speed close to the speed of light. The presence of the pre-emphasis circuit that generates the differential current signal is explained by the non-ideal behaviour of the transmission lines and the losses that are present. The transmission line receiver [9] (see Fig. 9)generates the pulses with edges of 50ps to drive the TDC inputs. The receiver presents 2 different parts, the first one is a differential to CMOS converter with hysteresis with 20μA bias current and a second part that is a dynamic asynchronous latch comparator with positive feedback (DALC). The DALC generates the fast transition signals without static power. This circuit uses positive feedback during transition to increase transition speed.

The measurements for the time walk compensations are based on time over threshold correction (TOT) measurements. In this architecture the arrival time is measured using delay locked loop (DLL) based time-to-digital-converters (TDC), where buffers connected in series are used as base elements. The propagation speed of these buffers can be controlled, but they have been designed to operate with a delay per cell of τdelay $\sim$97.65ps. The current to bias the delay cell is $\sim$ 80μA, with an expected power consumption per delay cell of 96 μW. The base frequency is sent to the first buffer, using a reference clock of 320MHz. The phases between the input of the first buffer and the output of the last buffer is monitored. If the phase difference is positive (the output is too slow) then the control circuit of the DLL will increase the speed of the buffers and inversely decrease it in case of the a negative phase difference. Once the loop is locked, the phase difference is zero, and the delay of the individual buffers divide the base clock period corresponding to the number of buffers in the chain. When a hit arrives hit registers capture the state of these buffers and the state of the base frequency clock counter. Look at Fig. 10 for the details.

The demonstrator contains only two DLLs and the DLL buffer signals are distributed to the hit registers. Also it is not required that each pixel cell has its own hit registers. The required efficiency of 99% can be achieved by multiplexing several pixels to one hit register. Calculation and simulation show that combining 5 pixels in one hit register a dead time of less than 0.5% is achieved. Consequently 9 hit registers for the rising edge time and 9 hit registers for the falling edge time are used for the array of 45 pixels.

A digital arbiter circuit has been designed to send hit pulses to the TDC banks and block signals from the same group of 5 pixels in case they would overlap in time. These overlaps are flagged and the information is added to the output data stream. The end of column circuitry of the demonstrator comprises one receiver for each pixel, the arbiter circuit for a group of 5 pixels, one TDC bank, address encoding circuits and the digital logic for processing the hit data ready for transmission off chip. The TDC circuits used in the end of column logic are based on previous developments done in 0.25 μm CMOS technology [10] and in 0.13 μm CMOS technology [11]. Each TDC consists of two 32-bit hit registers, one for the leading edge and one for the trailing edge of the hit, providing double time stamping. The leading edge time stamp provides information of the hit arrival time and the trailing edge provides the additional input charge amplitude information needed to correct time walk. In addition at the time of the leading and trailing edge the coarse clock counter value is latched. The double time stamp with coarse counter and address information are stored in a line buffer, which is then serialized and sent off chip.

For the final ASIC, distributing DLL outputs to all the columns will be difficult as the load comprises TDC banks for high number of columns and a long distance. This problem is solved by adding strong differential buffers at the output of the DLL and receiving buffers at the input of each TDC bank. The output of the DLL buffer is differential and is converted to single-ended only at the input buffer of each TDC bank. The hit registers use single-ended CMOS level signals. The hit registers in the TDC are built using 32 D-type flip flops with rising edge trigger. The output of the receiver cell provides a rising edge trigger for both leading and trailing edge hit registers. The EOC circuits are outside the beam area and thus the radiation levels are very low. Therefore there is no need to use single-event-upset protection circuits or circuitry against leakage currents in NMOS devices. Also, as the sensitive analogue circuits are in the pixels and use a different power supply to the isolated EOC circuits, there is no need to use differential logic. EOC circuits have a very dense layout design since the receiver bank, the TDC bank and the digital circuits fit inside a 300 μm pixel wide periphery of each column.

IV. Measurements of the Analog Pixel

The first measurements of the chips, see Fig. 11, were performed by the end of August 2009. A surface analysis has been performed to measure the thickness and smothness of the chip, giving a thickness value that varies between the following values 256.2-275.4μm. During the initial test, the measured power consumption found in static consumption is $\sim$8 mA for the 1.2V Analogue bias (corresponding to a 133.3 μA power consumption per pixel), $\sim$100 mA for the 1.2V Digital bias and $\sim$14 mA for the 2.5V Digital. This measured values correspond to a situation where mostly of the circuit remains inactive, with the DLL having no input clock applied to generate the delayed signal. The high power consumption of 164.6mW has also been analyzed in terms of temperature distribution. Thermal imaging has been used to study the temperature distribution, showing a maximum measured temperature of 34.79^{0}C and a minimum of 26.9^{0}C.

The first analog measurement has been to measure the analog output, where a $\sim$ 2fC of charge has been injected,

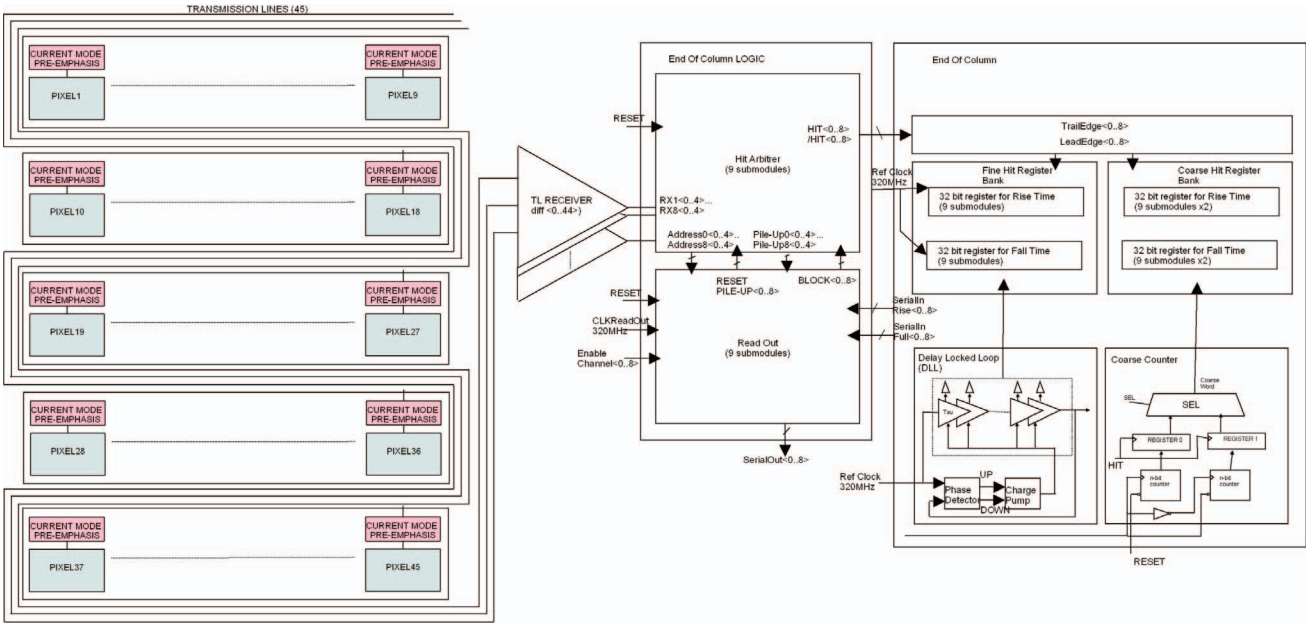

Fig. 10: End Of Column general architecture used in the GTK prototype

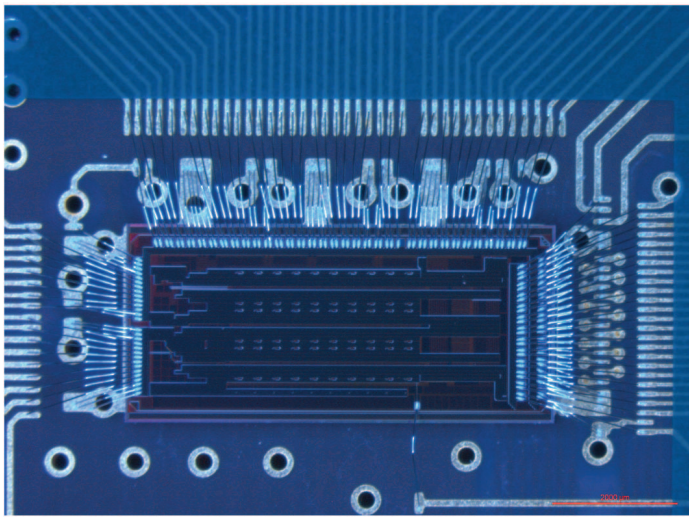

Fig. 11: Photograph of the bonded prototype of the GTK read-out chip.

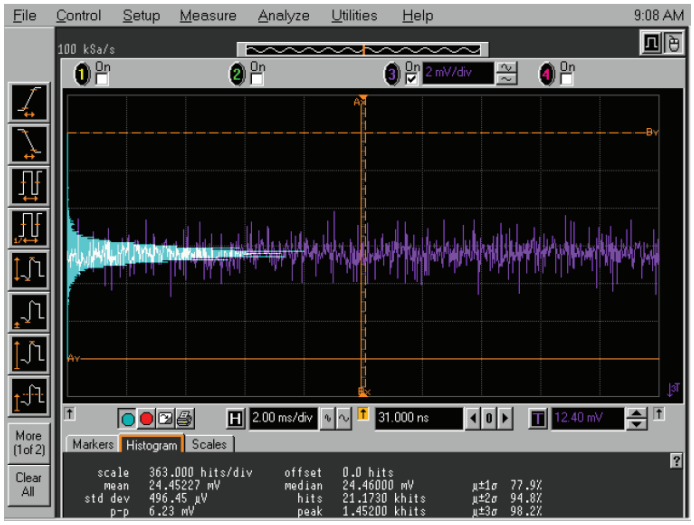

Fig. 12: Analogue output noise measured.

using a 100mV pulse into the 20fF capacitor, with a rise time of 0.5ns. Using this configuration the rms value of the analog output noise is $\sim$500μV, meaning an equivalent $\sim$56 e$^-$ ENC (see Fig. 12), which agrees with the simulation for case with no detector.

The next measurements correspond to the scan of the threshold over a fixed charge injected to a single pixel at a time, to obtain the corresponding S-curve. All 5 of the test pixels were measured, although just the results corresponding to pixel 10 are plotted in Fig. 13. The parameters used were V_{T1}= 1100mV, where falling edge pulse with a height of 150mV, injecting approximately 3fC and operating with negative polarity. The measurement begins with a trigger signal that is generated using a pulse generator, then there is an acceptance gate that lasts one clock cycle, corresponding to 25ns. After waiting for this fixed period of time, it is checked if the discriminator of the analog pixel test has fired during this specific time window. After this, the system sleeps for 1ms and then this action is repeated 10,000 times. After this extensive measurement, the threshold is changed, making a V_{T2} swepted based on the minimum DAC count of $\simeq$300μV. To finalize the measurements the charge injected is swept and increased 10 steps of 0.5fC each. The input voltage is applied after using an attenuator that decreases the signal by 10, and the whole process repeated after a settling time of 500ms, with an 250fF input capacitance. Gain and Offset statistics measurements have been done for the 5 test pixels present in the design, as can be seen in Fig. 14 and Fig. 15. The results presented here have been obtained using

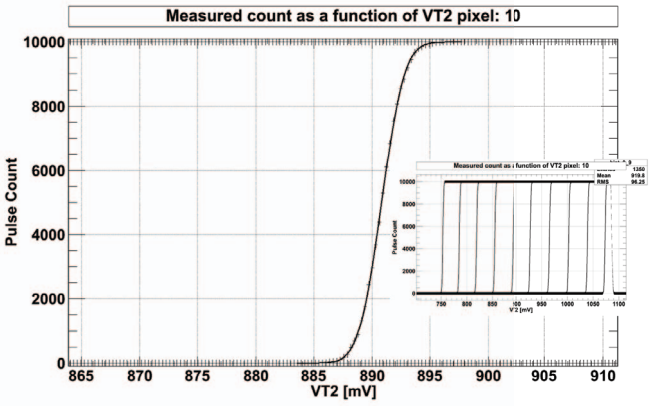

Fig. 13: S-curve plot for pixel 10, when setting VT1 to a fixed value and varying the VT2.

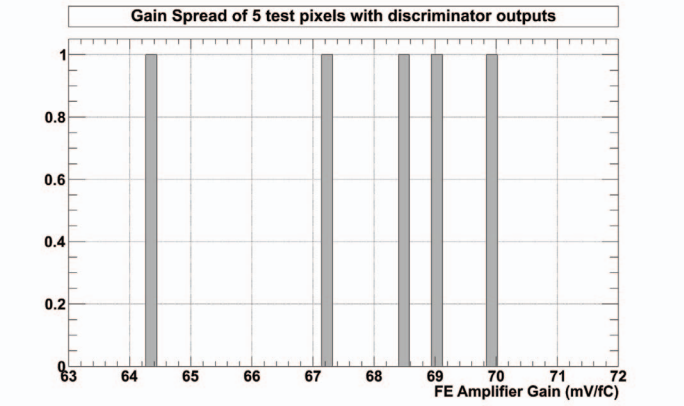

Fig. 14: Gain values extracted from the S-Curve for the 5 test pixels at linear region 1-3fC

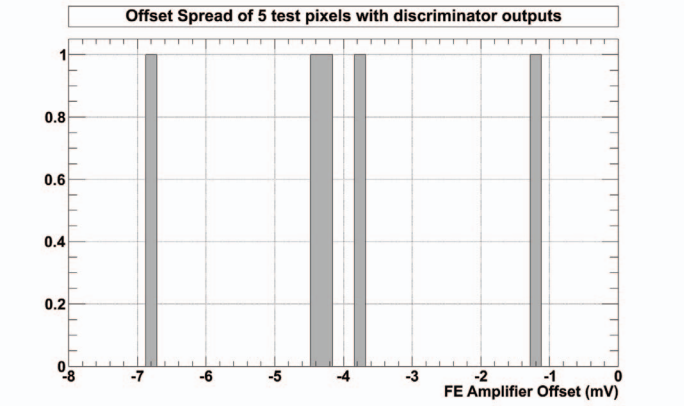

Fig. 15: Offset values extracted from the S-Curve for the 5 test pixels at linear region 1-3fC

the measurements corresponding to the linear gain region where the injected charge is from 1 to 3fC. The gain values obtained present a mean value of 67.81mV/fC, with respect the 70mV/fC expected value. This value is is lower that the simulated one, but it has been found to increase once the complete chain (including the discriminator) is used for the test measurement. The offset measurements obtained show a mean average value of -4mV. This value comes from process

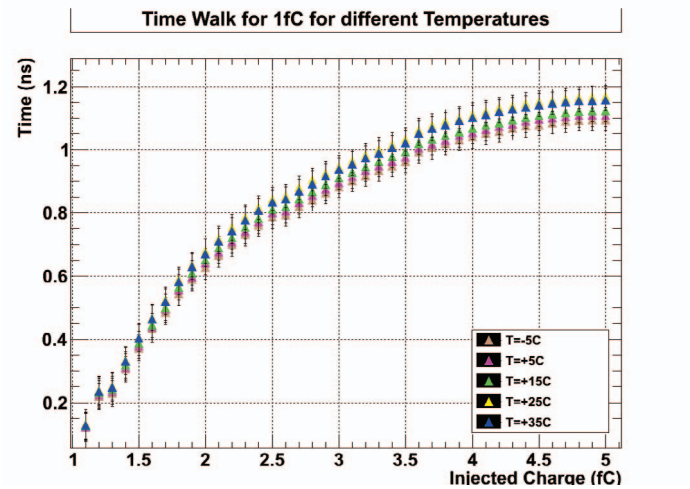

Fig. 16: Time Walk measurements obtained with respect 1fC injected charge for a range of temperature from -5^{0}C to 35^{0}C.

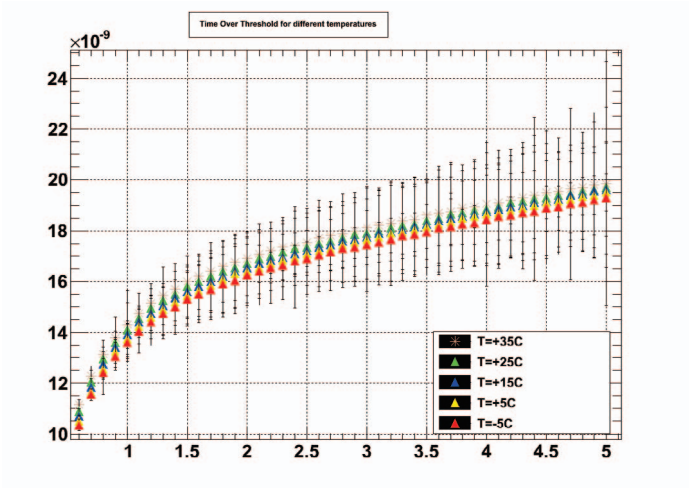

Fig. 17: Time Over Threshold measurements obtained for a range of temperature from -5^{0}C to 35^{0}C.

variations and inhomogeneities in the design chip fabrication.

A. Temperature depence of the EOC

Temperature measurements using a temperature control chamber have been performed, using one of the test pixels to evaluate the influence for the range from -5^{o}C to 35^{o}C. The two main aspects being analyzed have been the time walk and the time over threshold.

The results obtained for the time walk measurements are shown in Fig. 16. To compare the results obtained from the simulation with the results, the difference between the values at the 2 extremes of temperature is used, when considering an injected charge of 2fC. The simulated $\Delta\text{TW}_{from-5^0Cto+35^0C}$ ~0.13ns, but the measured value obtained is $\Delta\text{TW}_{from-5^0Cto+35^0C}$ ~0.1ns. The results obtained for the time over threshold measurements are found at the Fig. 17. To compare the results, a similar comparison as

has been made for the time walk results, also for an injected charge of 2fC. In this case the simulation value for the $\Delta\text{TOT}_{from-5^0Cto+35^0C}$ $\sim$0.6ns, in comparison with the measurements that give a value of $\Delta\text{TOT}_{from-5^0Cto+35^0C}$ $\sim$0.75ns

V. Conclusions

In this paper the GigaTracker pixel detector has been introduced, as well as the NA62 experiment, which takes place at CERN. The specifications of the pixel detector include high signal rate and and good timing resolution, low power consumption and low ENC. To obtain these goals, two different approaches have been proposed. The first approach uses pixels that digitize the shaper signal and convert it to current to then transmit it through the pixel matrix. The signal that arrives to the end of the matrix is measured in terms of leading and trailing edge using a TDC that will provide coarse/fine hit timing information and address. The second approach that is being studied measures the leading and trailing edge at the pixel cell level and then transmits the digitized information for further processing to the perifery of the chip. The two different approaches will allow a comparison in terms of power consumption, data flow and crosstalk between digital and analog circuitry. These designs have been fabricated using 130nm CMOS technology and the results of the analog measurements for the first approach are reported here. Measurements of the time walk and time over threshold are presented, showing good agreement between simulation and measurements over a range of temperatures from -5^{0}C to +35^{0}C. In the next months the digital circuitry test will be finalized, including the 320MHz DLL and a complete test with the bump bonded detector will be performed.

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