Fine-Time Resolution Measurements for High Energy Physics Experiments

Lukas Perktold and Jørgen Christiansen

Abstract Fine-time resolution measurements are attracting increasing attention in the high-energy-physics (HEP) community, where a large number of measurement channels must often be realized with a single ASIC. In this contribution, a multi-channel time-to-digital converter (TDC) architecture with a delay-locked-loop (DLL) in its first stage and a resistive interpolation scheme in its second stage is presented. The size of the TDC's least-significant-bit (LSB) is controlled by a reference clock and so can be continuously adjusted from 5 to 20 ps. A global calibration scheme that avoids the need to calibrate each channel separately is also used. Critical design aspects like device mismatch, supply noise sensitivity and process-voltage and temperature (PVT) variation are discussed. When realized in a 130 nm technology, the prototype ASIC achieved a single-shot resolution of better than 2.5 ps-rms. The measured integral-non-linearity (INL) and differential-non-linearity (DNL) were found to be ± 1.4 LSB and ± 0.9 LSB respectively.

1 Introduction

Many physical quantities like crossing time or energy of a particle can be determined on the basis of time measurements. Recently, high-energy-physics (HEP) detectors have emerged that achieve sub 10 ps-rms resolution, see [1, 2]. To realize their full potential, time measurements in the ps-rms resolution domain are required.

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This chapter presents the design of a multichannel, fine-time resolution TDC ASIC aimed at fulfilling the requirements of upcoming HEP detectors like the ATLAS AFP/CMS HPS [3] or LHCb TORCH [4] and others. Accurate absolute time measurements are then required, since it is often necessary to correlate measurements. For this purpose, a time reference is distributed across the experiment to synchronize the generated time stamps. To meet the requirements of many different experiments, a flexible TDC architecture that does not put any constraints on the measurement signal is desired. This rules out the use of START-STOP or noise-shaping TDC architectures.

Today, device mismatch together with jitter due to power supply and thermal noise represent the limiting factors in state-of-the-art TDC design. In recent designs, single-channel time resolutions in the order of 1 ps have been achieved, see [5] or [6]. However, this then necessitates the use of calibration techniques to compensate for device mismatch. Especially in a multichannel environment, calibration on a per-channel basis can lead to considerable circuit overhead and represent a time-intensive task during production.

In this work, a multi-channel TDC architecture is presented. It employs a global calibration scheme that avoids the need for per-channel calibration. Important design trade-offs such as device mismatch and power supply noise susceptibility are discussed, and measurement results on a prototype implemented in a 130 nm technology are presented.

2 Time Measurements in HEP

In HEP and other closely related fields, e.g. positron emission tomography (PET) [7] or fluorescence lifetime imaging microscopy (FLIM) [8] to mention just a few, it is crucial to measure the characteristics of the physical particles that encounter a detector. Quantities such as position, crossing time, momentum or energy of a particle need to be measured with high precision. Whereas crossing point location can be resolved by dividing the sensor into smaller units, crossing time as well as energy can be derived from time measurements.

The block diagram of a single-channel time measurement chain often employed in HEP detector designs is shown in Fig. 1. Often several hundreds or thousands of channels are required to cover the physical area of interest. The charge induced in a sensor is collected and amplified by a charge preamplifier, thus generating an analog signal. By discriminating the signal's amplitude, the crossing time and time-of-arrival of a particle can be extracted. The width of the resulting pulse, which is still continuous in time, can then be digitized using a TDC. In contrast to the traditional approach in which the amplitude of the analog signal is digitized using an analog-to-digital converter (ADC), employing a TDC-based scheme allows system complexity to be drastically reduced, as well as the amount of data generated. As the signal induced in the sensor may be non-ideal, a signal pre-processing stage might be added to suppress glitches and/or define a minimum

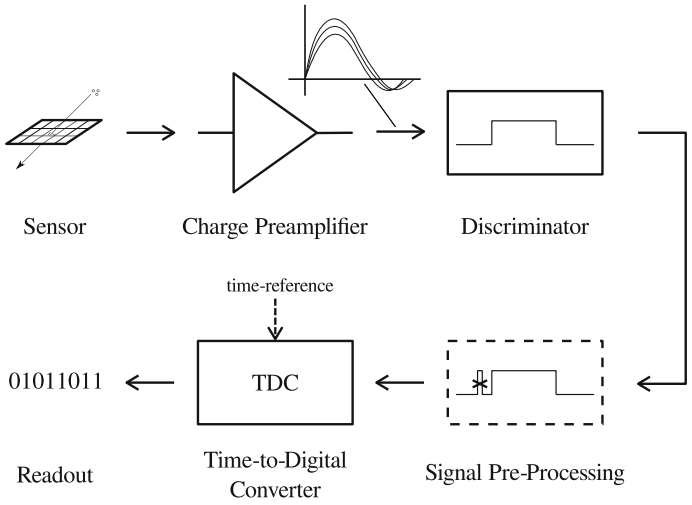

Fig. 1 Time-measurement chain in HEP

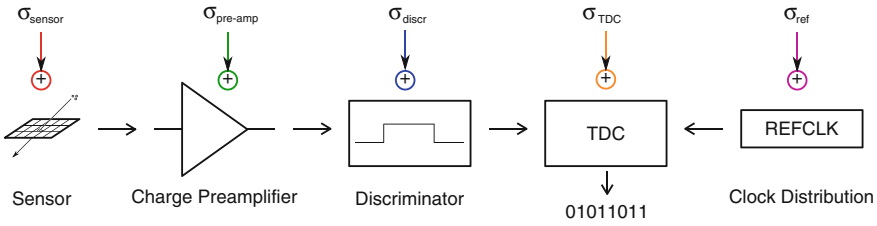

Fig. 2 Timing uncertainties of a typical detector design

pulse width and gap. Depending on the rate at which particles encounter the detector, a great amount of data might be generated, so a dedicated readout scheme to selectively access and retrieve this data is required. As illustrated in Fig. 2, the TDC's timing uncertainty represents only one of many timing uncertainties in the system. As a result, the TDC's timing uncertainty (σ_{TDC}) is often required to be negligible, thus making its design rather challenging.

3 Fine-Time Resolution TDC Design

The time resolution of an ideal TDC is only limited by the size of its LSB. For a uniformly distributed sequence of events, the standard deviation of the error, a function more often referred to as the TDC's quantization noise, can be calculated from Eq. 1. At some point, however, other error sources will become dominant,

making further reductions in LSB size unnecessary. As a rule of thumb, the LSB size should be chosen to match the required rms-time resolution. This allows the quantization error to be kept well below the desired resolution.

$$\sigma_q = \frac{LSB}{\sqrt{12}} \tag{1}$$

In a real implementation, the resolution will be degraded by device mismatch as well as by the jitter introduced by power supply and thermal noise. In the case of uncorrelated error sources, which usually is the case in a real application, since the errors originate from different sources, the expected time resolution can be written as

$$\sigma_{TDC} = \sqrt{\sigma_{qDNL}^2 + \sigma_{wINL}^2 + \sigma_{noise}^2 + \sigma_{ref}^2}. \tag{2}$$

Where the rms sum of the quantization error of a specific bin is represented by σ_{qDNL}, the effect of integral non-linearity is denoted by σ_{wINL} and the rms jitter due to thermal and power supply noise is denoted by σ_{noise}. Although jitter introduced by the reference signal is referred to as σ_{ref}, it does not represent an inherent contribution of the TDC itself, nevertheless, due to measurement restrictions, it is often directly included in the TDC's resolution.

3.1 Device Mismatch

Due to device mismatch, the size of each LSB will vary and manifest itself in integral-non-linearity (INL) errors as well as differential-non-linearity (DNL) errors. If measured in advance, however, INL errors can be corrected off-line whereas DNL errors cannot. For uniformly distributed events, larger bins, due to their higher probability of being hit, will collect more events. This will lead to a degradation in time resolution, as larger bins also suffer from larger quantization error. To account for this behavior, the standard deviation of the quantization error needs to be calculated based on the real value of LSB size taking into account their relative probability p_i to receive a hit, defined as LSB_i/T_{ref}. This relation is more clearly expressed by

$$\sigma_{qDNL} = \sqrt{\sum_{i=0}^{N-1} \left(\frac{LSB_i}{\sqrt{12}}\right)^2 \cdot p_i}. \tag{3}$$

where N represents the number of TDC bins. In a similar manner the standard deviation of the INL can be represented by the rms sum of the INL error of each specific bin also weighed by its relative probability to get hit p_i, expressed as

$$\sigma_{wINL} = \sqrt{\sum_{i=0}^{N-1} \left(INL_i - \overline{INL}\right)^2 \cdot p_i}, \quad \text{with} \quad INL_i = \frac{\Delta LSB_i}{2} + INL_{i-1}, \tag{4}$$

where $\overline{INL}$ represents the mean INL error, ΔLSB_i represents the deviation from the mean LSB size and INL_i the accumulated time error with $INL_{-1} = 0\,\text{ps}$.

If the variation of the LSB size is small compared to its nominal value, the non-weighted standard deviation of the DNL and INL across all bins represents a good estimate. However, in the case of large device mismatch, a weighted representation of the TDC's nonlinearities leads to a more precise estimate of the expected rms-time resolution. From Monte-Carlo simulations, the effect of device mismatch can be well estimated early in the design phase.

3.2 Jitter

Timing variations due to power supply and circuit noise modulate the switching time of the circuit, leading to timing errors. As illustrated in Fig. 3, voltage variations can be well modeled as threshold voltage shifts in the vicinity of a switching point as denoted by σ_{vth}. Thereby, the generated timing error is proportional to the slew-rate (SR) of the signal. From small signal analysis, voltage variations in the vicinity of switching point due to circuit noise as well as power supply noise can be calculated. A periodic-steady-state (PSS) analysis following a periodic-noise (PNoise) simulation as proposed by [9] can be used to calculate σ_t as expressed by Eq. (5).

$$\sigma_t = \sigma_{vth} \cdot \frac{1}{SR} \tag{5}$$

Mathematically, jitter can be expressed on a per bin basis by

$$\sigma_{t_i} = \lim_{M \to \infty} \sqrt{\frac{1}{M} \sum_{n=0}^{M-1} \left(t_n^{ideal} - t_n^{real}\right)^2} \tag{6}$$

where t_n represents the nth crossing of a signal and M the number of cycles. More often such a definition of jitter is referred to as time-interval-error (TIE). If all error sources are assumed to be uncorrelated, the standard deviation of jitter across all bins, denoted by N, can be expressed by Eq. 7

$$\sigma_{noise} = \sqrt{\frac{1}{N} \sum_{i=0}^{N-1} \sigma_{t_i}^2}. \tag{7}$$

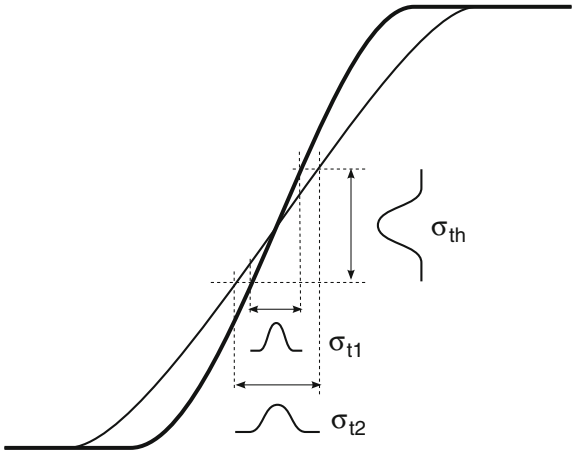

Fig. 3 Timing error dependence on signal slew-rate

Unfortunately, for low-frequency power-supply noise variations, the jitter of adjacent bins will not be truly uncorrelated, making a mathematical representation difficult. Depending on the exact nature of power supply noise, the timing error might not manifest itself as jitter at all. Power supply noise synchronous with the system clock will cause the LSB of the different bins to change by the same amount each clock cycle. This error will finally show up as a non-linearity errors causing an increase of σ_{qDNL} and σ_{wINL}.

Whereas jitter due to thermal noise can be well approximated during design time, timing variations caused by power supply noise are much more difficult to assess early in the design process. To limit the negative effect of power supply noise, it is good practice to minimize propagation delay as well as to employ fast signal edges of timing critical signals.

4 TDC Architecture

To reach ps-rms resolutions, an LSB size of 5 ps is envisaged. A block diagram of the proposed architecture is shown in Fig. 4 as reported in [10]. All measurements are referred to a reference signal allowing multiple TDCs to be synchronized to one common timebase. In a large system where multiple TDCs are operated in parallel, such a synchronization approach is vital. The reference clock signal serves as the time-base of the TDC and is connected to the fine-time interpolator and counter block respectively. Both the fine-time interpolator as well as the coarse counter are shared across all the channels, and so only need to be implemented once per ASIC. The fine-time interpolator generates a set of uniformly distributed signals, here referred to as the fine-time code of the TDC. A counter,

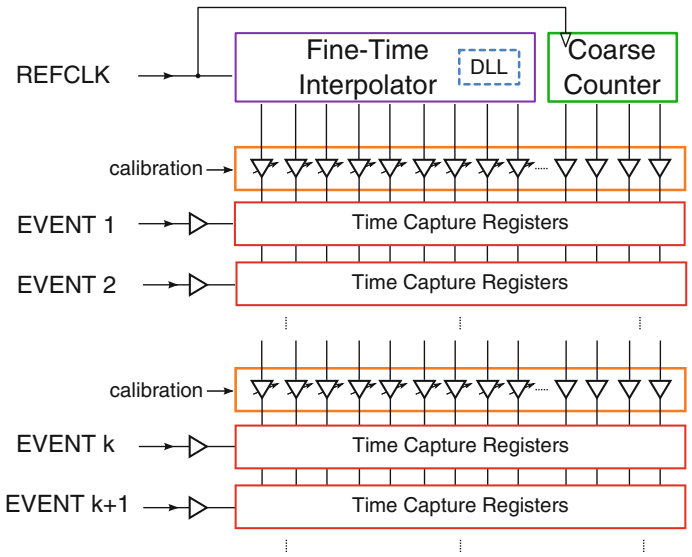

Fig. 4 Proposed multi-channel TDC architecture

which tracks the number of completed clock cycles, is added to efficiently extend the dynamic range of the interpolator by an amount that is only limited by the number of bits of the counter.

The TDC's finest LSB size is generated at the level of the fine-time interpolator. No local interpolation on a per-channel basis is required, thus reducing the complexity of a single channel to a minimum. The generated fine-time as well as the counter code are connected to the respective channels by so-called distributed buffers. To sustain sharp signal edges throughout the channel matrix, several channels are grouped into segments served by a dedicated set of buffers. This efficiently compensates for the RC-delay of the long wires. To compensate for the device mismatch introduced by the fine-time interpolator as well as by the distribution buffers, a calibration feature is integrated at the level of the distribution buffers. No calibration is required on a per-channel basis. PVT variations are compensated by a DLL implemented at the level of the fine-time interpolator block. By controlling the LSB size down to its smallest interpolation level, the LSB size can be adjusted solely by the reference clock frequency. This feature is highly appreciated by the HEP community as it allows time resolution to be traded off against power consumption and to precisely match the TDC's performance to the system requirements.

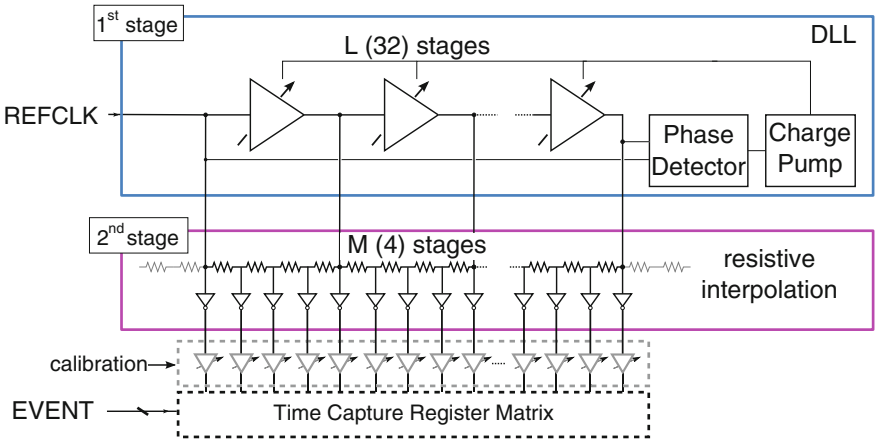

Fig. 5 A multi-stage interpolation concept. In the 1st-stage a DLL is used to reach gate-delay LSB size. In a 2nd-stage resistive voltage division is employed to achieve sub-gate delay resolution

4.1 Fine-Time Interpolator

To achieve sub-gate delay resolutions in conjunction with a large dynamic range, a multistage approach, as has been presented in [11], is pursued. In total $L \cdot M$ timing signals are generated, where L represents the interpolation ratio in the first stage and M the interpolation ratio in the second stage. In the first stage a DLL is employed to generate L uniformly distributed signals. Thereby, the delay of the delay-line elements is adjusted by the feedback loop so that the sum of all elements within the loop precisely match one reference clock period T_{ref}. In the locked condition, the delay of each delay element is equal to T_{ref}/L and is only controlled by the input frequency of the DLL. The second stage is based on resistive voltage division. Signals generated in the first stage serve as inputs of the second stage to derive finer delayed signals to overcome the propagation delay limitations of the technology. This allows LSB sizes as small as T_{ref}/LM to be achieved (Fig. 5).

To reduce the amount of propagation delay within the loop, it is advantageous to run the DLL at high frequencies. The higher this is, the less delay stages are required to achieve a given LSB size. Running the DLL at high frequencies also minimizes the effect of device mismatch and decreases the DLL's noise sensitivity. However, for practical purposes, to reduce potential difficulties with handling high frequencies off-chip, the DLL clock is preferably kept below 2 GHz. In a 130 nm technology, the gate delay is in the order of 20 ps. To ease digital coding later on in the system, integer interpolation factors of base two are preferred. To achieve the envisaged 5 ps LSBs, choosing $L = 32$ and $M = 4$ represents a good choice. Such a combination requires a DLL clock frequency of 1.5625 GHz.

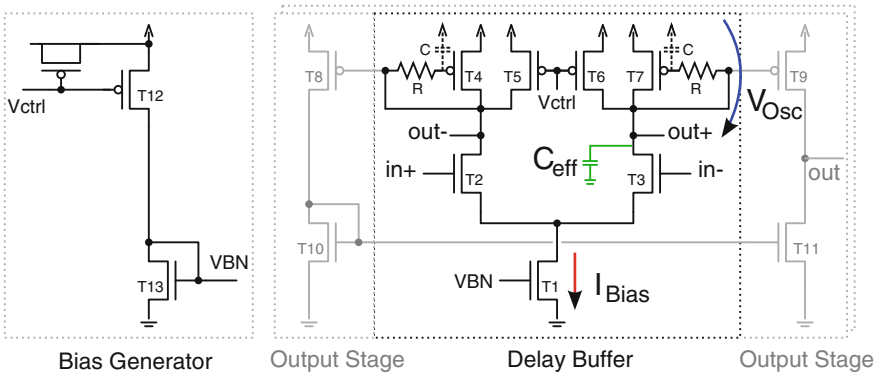

Fig. 6 Bias circuit and fast delay cell element of the DLL. An additional zero is added in the signal path to speed up the cell

4.2 Delay-Cell Element

Careful design of the DLL's delay-cell element is needed to achieve short propagation delays, and to reduce the complexity of the 2nd stage. A modified version of the fully-differential delay buffer presented in [12] is employed. A schematic diagram of the delay buffer together with its bias generation circuit is shown in Fig. 6. The inputs of the delay buffer *in*+ and *in*− are connected to the outputs *out*+ and *out*− of the succeeding cell. The propagation delay of the cell can be adjusted by means of V_{ctrl} which is adjusted to the desired delay by the feedback mechanism of the DLL. An operational transconductance amplifier (OTA) is employed to generate a single-ended signal that distributes the fine-time code across the channel matrix. Such an approach turns out to be feasible as the propagation delay introduced by the distribution buffers is small compared to the delay introduced by the delay-line itself. To increase the cells robustness against power supply disturbances, large signal swings are preferred.

The propagation delay of the cell can be very roughly estimated by $\tau \approx \frac{V_{osc} \cdot C_{eff}}{2 \cdot I_D}$ where V_{osc} represents the oscillation voltage, C_{eff} the total capacitive load at the output and I_D represents the current defined by *VBN*. To additionally speed up the cell, a zero is added to the signal path to hide the gate capacitance of the top PMOS diode by using resistive peaking [13]. From the equivalent half circuit of the cell, neglecting channel length modulation effects, an output impedance of

$$Z_{out} = \frac{1}{gm_2} \cdot \frac{1 + sRC}{1 + s\frac{C}{gm_2}} \tag{8}$$

can be derived. For $\frac{1}{RC} \ll s \ll \frac{gm_2}{C}$ the output resistance reduces to $\frac{sRC}{gm_2}$ making the load look like an inductor. This can be thought of as hiding the diode-connected load C during the switching cycle. With resistive peaking, an additional reduction

Table 1 Device dimensions of the circuit shown in Fig. 6

Device	Width (µm)	Length (µm)
T1 and T13	18	0.6
T2 and T3	4	0.12
T5 and T6	4.5	0.12
T4, T7, T8 and T9	3	0.12
T10 and T11	1.36	0.12
T12	7.5	0.12
R	11 kΩ	

in propagation delay of 9 % is achieved. The differential-to-single ended (DE/SE) converter is designed to provide similar current drive strength as in the main cell and is sized to reduce the propagation delay employing small length devices.

With the interpolation factors proposed in Sect. 4.1 the maximum propagation delay of the delay cell must not exceed 20 ps. With dimensions as given in Table 1 propagation delays as low as 16 ps can be achieved in a 130 nm technology when the cell is operated with a 1.2 V supply. Across process voltage and temperature, the delay is expected to be vary from 12 ps to 23 ps. To compensate for slow process corners, the supply voltage can be increased up to 1.5 V.

4.3 Resistive Time Interpolation

To overcome the propagation delay limitation of the technology used, a resistive division interpolation concept is employed [14]. Low power consumption as well as high robustness against device mismatches represent the most attractive arguments of a resistive interpolation concept. The basic structure of the concept is depicted in Fig. 7. A resistive voltage divider is connected across the outputs of the DLL. Due to the voltage drop across the resistive ladder finer time delays can be generated. The number of DLL elements involved during the switching cycle depends on the slope of the signals propagating down the ladder. To a first approximation, the number of elements involved in the process can be estimated from the signal slope as expressed by $\frac{t_{slope}}{LSB}$. Fast signal slopes require stronger drivers, whereas on the other hand, slower signal slopes are more sensitive to power supply noise and require more elements at the beginning and the end of the DLL to reach uniformity. To compensate for delays introduced by the RC delay characteristics of the scheme, a non-linear resistive divider has been implemented employing resistor values varying from 28 to 48 Ω. A good trade-off has been found for signal slopes of 120 ps. This involves approximately 6 delay elements or equivalently 24 LSB codes. To profit from the stronger NMOS driving capability, the negative edge is used to distribute the fine-time code across the channel matrix.

A nice feature of the passive interpolator structure is its device-mismatch filtering capability. In a similar manner as reported by [15], due to resistive coupling,

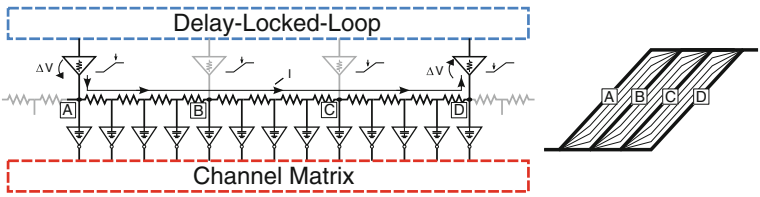

Fig. 7 Resistive voltage division principle

delay variations of adjacent cells are effectively averaged. To a first approximation, the expected 1-sigma standard deviation is scaled by $1/\sqrt{K}$ where K represents the number of elements involved in the signal transition. Due to the long tails of the transitions, a high coupling between adjacent cells is achieved. For the specific implementation, a reduction by more than a factor 5 could be achieved in the mismatch of the resulting falling edges. However, due to the small output buffers used to buffer these timing signals, additional mismatch is added. This finally leads to an improvement of "only" a factor of 1.6.

4.4 Calibration

To compensate for device mismatches introduced by the fine-time interpolator and distribution buffers, an adjustment feature has been included at the level of the distribution buffers. From Monte-Carlo simulations the expected standard deviation of the fine-time interpolator including the distribution buffers across all bins has been estimated to be 1.8 ps-rms. To not only allow DNL errors to be corrected but also INL errors of up to 6.4 LSB, a 5 bit adjustment feature has been implemented, see Fig. 8. Capacitive loading is employed to adjust the propagation of the timing signals. To avoid placing a large capacitive load at the output of the buffer, the adjustment feature is implemented after the first buffering stage. In total up to 64 fF in 2 fF steps can be added, allowing signals to be delayed by up to 32 ps in 1 ps steps. Due to the additional capacitive loading, the power consumption is increased by approximately 25 % compared to a cell without the calibration feature.

4.5 Time Capturing

To capture the time-of-arrival of an event, the actual state of the fine-time code as well as the counter value are stored in so called time capture registers (TCRs). As illustrated in Fig. 9 the event signal is connected to the CLK-input of the TCRs whereas the fine-time code is connected to the D-input of the registers. From the latched code (i.e. the 1 to 0 transition) the exact time-of-arrival can be resolved

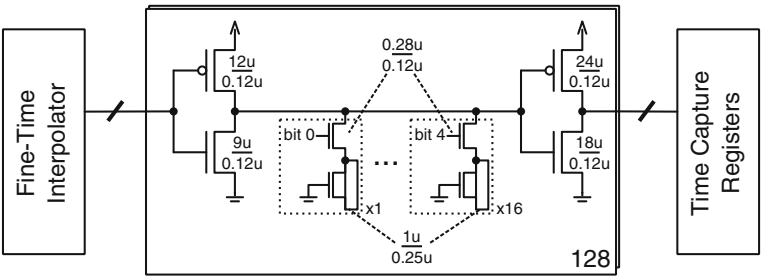

Fig. 8 Schematic diagram of the distribution buffers to distribute the fine-time code. Capacitive loading is used to adjust for device mismatches

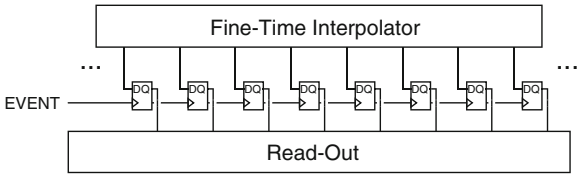

Fig. 9 Illustration of the time capturing concept. The time-of-arrival of an event is captured by sampling the state of the fine-time interpolator

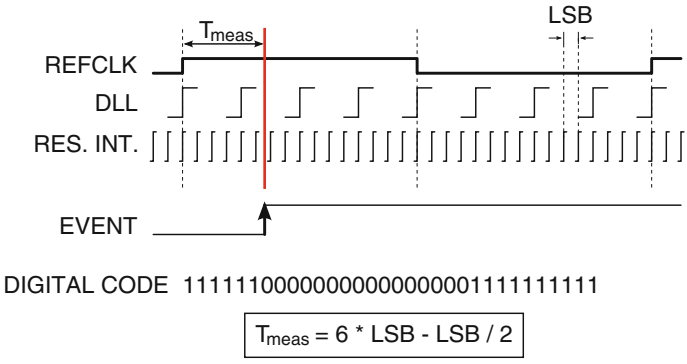

Fig. 10 Timing diagram of the time capturing process

(Fig. 10). For the event to be captured, the first latch of the TCRs needs to be kept transparent to allow the latch to follow the state of the fine-time code signals. This causes the 1st latch to switch with the frequency of the reference input, causing additional power to be consumed.

To balance power consumption and device mismatches of the registers, two different versions of the TCRs have been implemented. One register has been taken from the standard cell library together with its layout, whereas the other

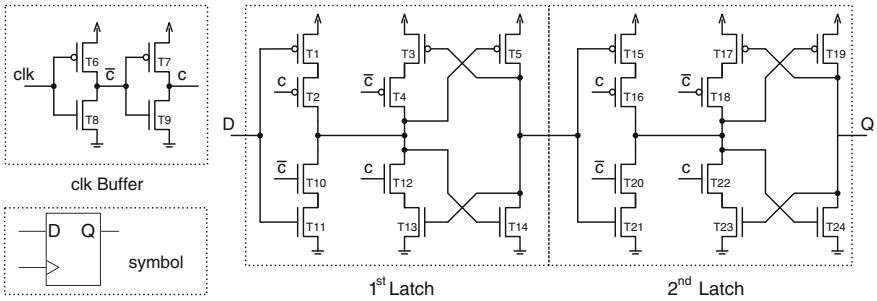

Fig. 11 Schematic diagram of the TCRs. The 1st latch is optimized for timing

Table 2 Device dimensions of the circuit shown in Fig. 11

Device	Standard cell TCR width (μm)	Custom TCR width (μm)	Length (μm)
T1–T7	1	3	0.12
T8–T14	0.5	1.5	0.12
T15–T19	1	1	0.12
T20–T24	0.5	1	0.12

Two different versions have been implemented to compare matching performance

register has been custom designed and laid-out to improve timing performance and reduce parasitic capacitances. The schematic diagram of the employed TCR is depicted in Fig. 11. The dimensions of both versions are listed in Table 2. In the custom TCR, the 1st latch has been optimized for good matching. From Monte-Carlo simulations, the expected 1-sigma variation of the time capturing point is about 2.4 ps-rms for the standard TCR and 1.3 ps-rms for the custom TCR respectively. Whereas, the custom TCR has been designed to achieve sufficient timing accuracy for a 5 ps LSB TDC the standard TCR is expected to be suitable only for a 10 ps LSB TDC. With either register, distinct channel pairs have been implemented to compare simulation results against measurements.

5 Experimental Results

A prototype has been designed and fabricated in a commercial 130 nm technology. In Fig. 12 a micro-photograph of the constructed ASIC wire-bonded to its carrier board is shown. The demonstrator consists of 8 channels, together with the fine-time interpolator as well as the distribution buffers and their bin adjustment feature. Different channel configurations were implemented to investigate the effect of device mismatch, input buffer architecture as well as time capturing concept. With the constructed test setup, the effect of different input buffer architectures was found to be negligible. The performance of the channels making use of the

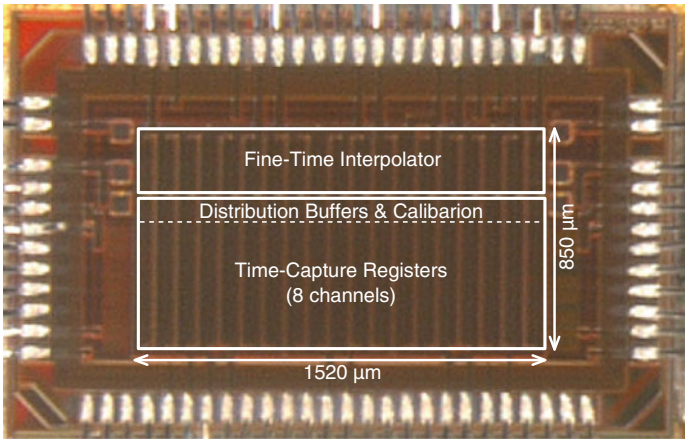

Fig. 12 Micro-photograph of the demonstrator ASIC

Table 3 Performance summary of the TDC for the standard cell and custom TCR

Technology	130 nm	
Supply voltage	1.3 V	
Chip area	1.2 mm^2	
# of channels	8	
	Custom TCR	*Standard cell TCR*
Ref. frequency	1.5625 GHz	781.25 MHz
LSB size	5 ps	10 ps
DNL	±0.9 LSB	±0.9 LSB
INL	±1.4 LSB	±0.7 LSB
Single shot precision	<2.5 ps	∼5 ps
Power consumption[a]	36.5 mW	13.3 mW
Dynamic range	640 ps (on chip)	1,280 ps (on chip)

[a] Per channel power consumption excluding shared components

time capturing concept described in Sect. 4.5 was also investigated. The TDC's time reference was supplied by a low jitter clock generator with a measured period jitter of <1 ps-rms. A summary of the resulting performance is listed in Table 3.

5.1 Non-linearities

To extract the transfer characteristic of the TDC, a uniformly distributed sequence of events was generated. From the number of samples collected by each respective bin, the actual LSB size can be approximated by $LSB_i = \frac{\#Events_i}{\#TotalEvents} \cdot T_{ref}$. A sequence of 10^5 events was found to approximate the LSB size with satisfying accuracy.

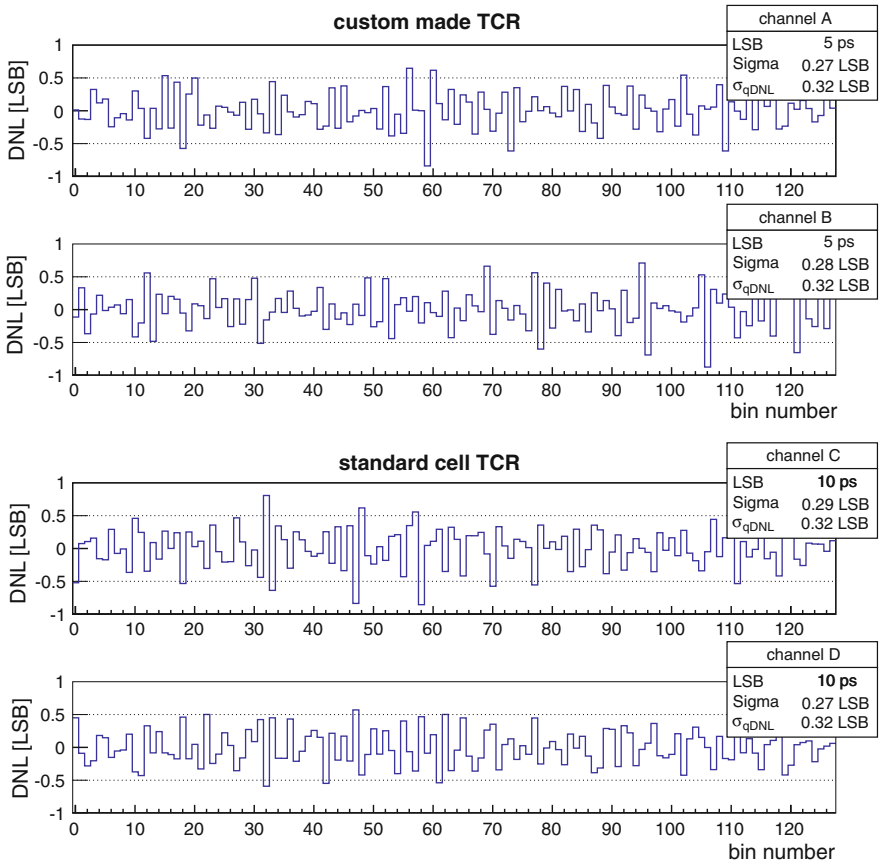

Fig. 13 Measured DNL of all 128 bins of the interpolator for *channel A–D*. The *boxes* list the 1-sigma distribution as well as the weighted DNL error calculated after Eq. (3)

In Figs. 13 and 14 receptively, the measured DNL and INL of channels A–D after global calibration has been applied is shown. For the channels employing the standard TCR (i.e. C and D) the reference clock period has been reduced to 781.25 MHz to account for the lower timing precision of the standard TCR. Across the whole dynamic range of the TDC no missing codes were observed. As a first estimate, the expected single-shot precision can be calculated by $\sigma_{TDC} \approx \sqrt{\sigma_{qDNL}^2 + \sigma_{INL}^2}$. This accounts for timing variations resulting from the TDC's quantization noise and non-linearities. From the measurement results, the expected time resolution for channels using the standard cell TCR and the custom-made TCR of 4 and 2 ps-rms respectively was calculated. From Monte-Carlo simulations, the achievable time resolution has been estimated to be 4.8 and 2.9 ps-rms respectively, well in line with measurements.

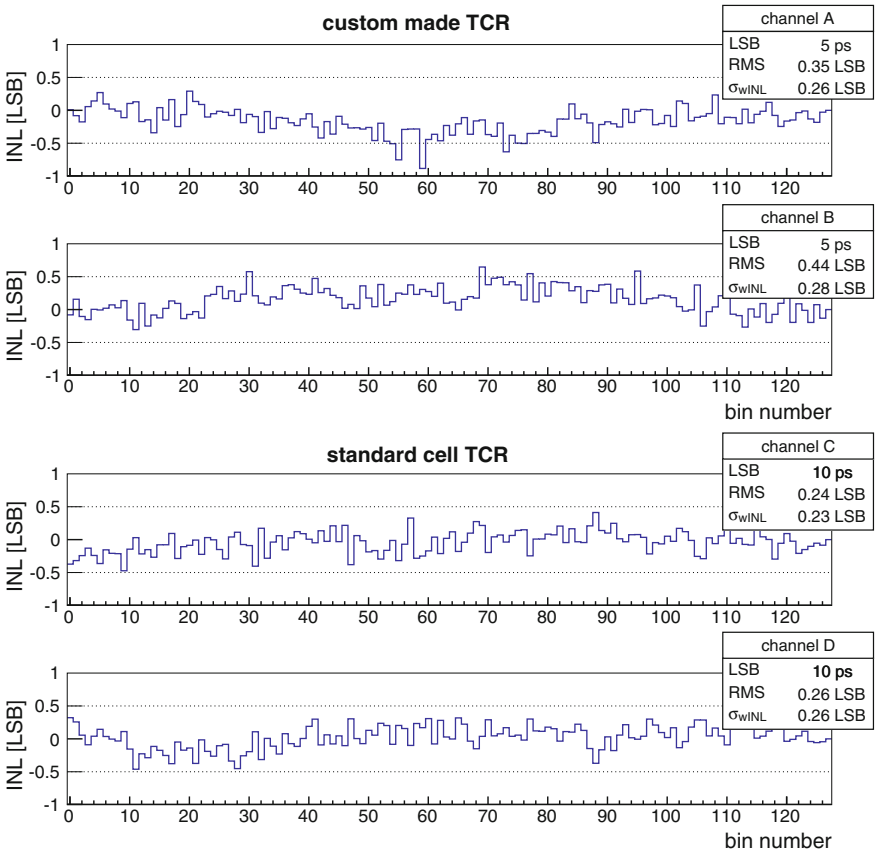

Fig. 14 Measured INL of all 128 bins of the interpolator for *channel A–D*. The boxes list the 1-sigma distribution as well as the weighted INL error calculated after Eq. (4)

5.2 Single-Shot Precision

To measure the actual rms-time resolution often also referred to as the single-shot precision of the TDC, a uniformly distributed sequence of events was generated and sent to two distinct channels. A fixed length of wire was added to one of the channels to generate a constant propagation delay between the two channels. This allows the generation of delay differences that only depend on the length of wire and so are robust to voltage and temperature variations. To generate two copies from a single event, a resistive power splitter is employed. From the collected samples, the bin number difference between the two channels is histogramed and the underlying Gaussian distribution is extracted. Its standard deviation is used to estimate the single-shot precision of the TDC. As two edges are involved in the measurement the standard deviation has to be scaled by the $1/\sqrt{2}$ as expressed by

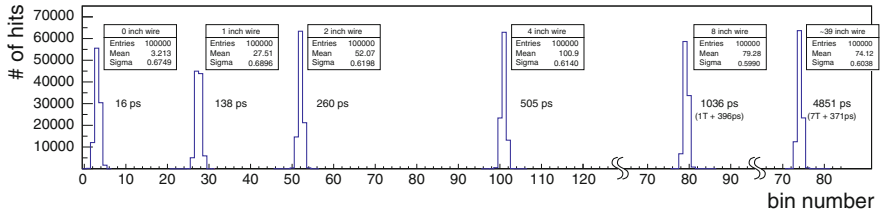

Fig. 15 Measured delay difference of channel pair A and B for a 4 in. length wire

Eq. (9). Using a time difference measurement, only timing contributions coming from the TDC itself as well as jitter resulting from the time reference signal are recorded by the measurement. Any contribution resulting from the event signal itself are excluded from the measurement.

$$\sigma_{TDC} = \frac{\sigma_{\Delta bin} \cdot LSB}{\sqrt{2}} \tag{9}$$

In Fig. 15 the recorded time difference of channel pair A & B employing the custom TCR for different wire delays is shown. For the custom TCR, the TDC reference clock was set to 1.5625 GHz resulting in a 5 ps LSB size TDC. In the case of the standard TCR, the TDC was operated with a 781.25 MHz generating 10 ps LSB sizes. Different time delay differences were generated to record the TDC's precision across its dynamic range. The delay difference between the two channels has been adjusted so that the event signal of the 2nd channel arrives (a) within one clock cycle, (b) one clock cycle later and (c) multiple clock cycles later. However, no notable influence of the wire length could be observed. After calibration, a single-shot precision of 2.5 ps-rms for the channels using the custom made TCR and 5 ps-rms for the channels employing the standard cell TCR has been achieved. This result is well in line with the expected time resolution derived earlier in Sect. 5.1.

5.3 Power Consumption

The power consumption of the TDC is extracted by means of a current-voltage measurement. For the architecture to capture an event, the first latch of the TCR has to be transparent. Lower power is consumed if acquisition is not running. When operated with a 1.5625 GHz reference clock an equivalent power of 34 mW to 42 mW per channel is consumed by the demonstrator. If a higher number of channels is implemented the contribution of shared components can be reduced. In Table 4 the power consumption contribution of a single channel (including 1.3 mW for the I/O buffer) is estimated from simulation to be 36.8 mW and 13.3 mW per channel, for channels employing the custom and standard cell TCR

Table 4 Performance comparison of different channel configurations

Channel	LSB (ps)	Single-shot (ps-rms)	Power per ch.		# ch. per segment
			Acqu. on (mW)	Acqu. off (mW)	
A and B	5	<2.5	36.8	23.8	9
A and B	10	~4	19.3	13.0	9
A and B	20	~7	10.9	7.6	9
C and D	10	~5	13.3	10.5	11

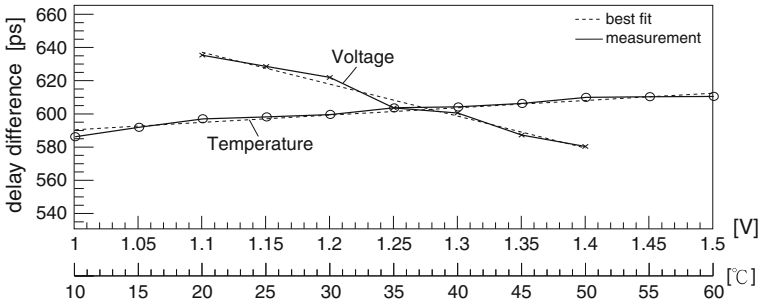

Fig. 16 Measured delay variations due to voltage and temperature shifts

respectively. Less power is consumed at lower reference clock frequencies, i.e. larger LSB size. For the estimate, the number of channels per segment has been chosen to equally load the output of the distribution buffers.

5.4 PVT Sensitivity

Any propagation delay not kept stable across temperature and voltage will suffer from propagation delay variation effects. In the proposed architecture, the LSB size is solely determined by the reference signal's frequency and is thus held stable across PVT variations. However, the event and reference clock I/O buffers as well as the distribution buffers are not adjusted by the loop. Any delay difference introduced in those two paths will show up as a constant time shift in the measurement. Depending on the absolute change in propagation delay, the sign can either be positive or negative.

To characterize the circuit's sensitivity to voltage and temperature variations, an event with a fixed phase relationship with respect to the reference clock was generated and recorded across voltage and temperature. As depicted in Fig. 16, a voltage sensitivity of −0.2 ps/V and a temperature variation of 0.4 ps/°C were measured. These variations were found to be negligible compared to the variations introduced by other building blocks within the measurement chain (e.g. charge preamplifier [16]).

Table 5 Performance comparison

References	Method	LSB (ps)	Single shot	Power[a]	Channels	Robustness[b]
[7]	Time amp.[c]	8.9	–	–	128	∼/+
[17]	RC-delay	24.4	15.8 ps-rms	125 mW	8	∼/∼
[18]	WaveUnion	3.7[d]	2.5 ps-rms	–	10	+/∼
[19]	Cap. scaling	12.2	13 ps-rms	20 mW	2	+/∼
[14]	Pas. interpl.[c]	4.7	3.3 ps-rms	3.6 mW[e]	1	∼/+
[5]	Time amp.[c]	1.25	0.6 ps-rms	3 mW[f]	1	−/∼
This	Pas. interpl.	5	2.5 ps-rms	43 mW	8	+/+

[a] Per channel
[b] PVT and mismatch /power supply noise
[c] START-STOP measurement
[d] Equivalent LSB size
[e] 180 MHz sampling frequency
[f] 10 MHz sampling frequency

6 Conclusion

A multi-channel TDC architecture precisely matched to the requirements of next generation HEP experiments has been presented. When operated with a 1.5625 GHz reference clock, 5 ps LSB sizes are generated. After calibration, a DNL and INL of ±0.9 LSB and ±1.4 LSB have been achieved. The single-shot precision of the TDC has been evaluated by means of a time-difference measurement for different wire length differences. For the better matching channels, a single-shot precision of better than 2.5 ps-rms has been demonstrated. The full prototype consumes between 34 mW/channel to 42 mW/channel. Lowering the input clock frequency to 781 MHz (=10 ps LSB sizes), the power consumption can be reduced to 21 mW/channel to 26 mW/channel respectively. The architecture exhibits a time shift in presence of voltage variations of −0.19 ps/mV and experiences a temperature dependence of 0.44 ps/deg. With the measurement precision of the test setup, inter-channel crosstalk between two neighboring channels has been evaluated to be below ±1 LSB.

In Table 5 a comparison with previously published TDCs is given. Compared to other high channel count TDCs, the presented architecture achieves very fine resolution with a high degree of robustness to power supply noise and PVT variations. The time measurements of the architecture are referred to a reference clock that can be common to many devices. In HEP experiments the event signal can arrive at any time, and so the TDC is required to run continuously as well as to offer a large dynamic range using a counter. The reader should observe that in such a continuously running environment, in contrast to START-STOP architectures, the interpolator cannot be disabled to reduce power consumption.

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