Compact and Low-Power Time to Digital Converters for High Granularity Silicon Detectors

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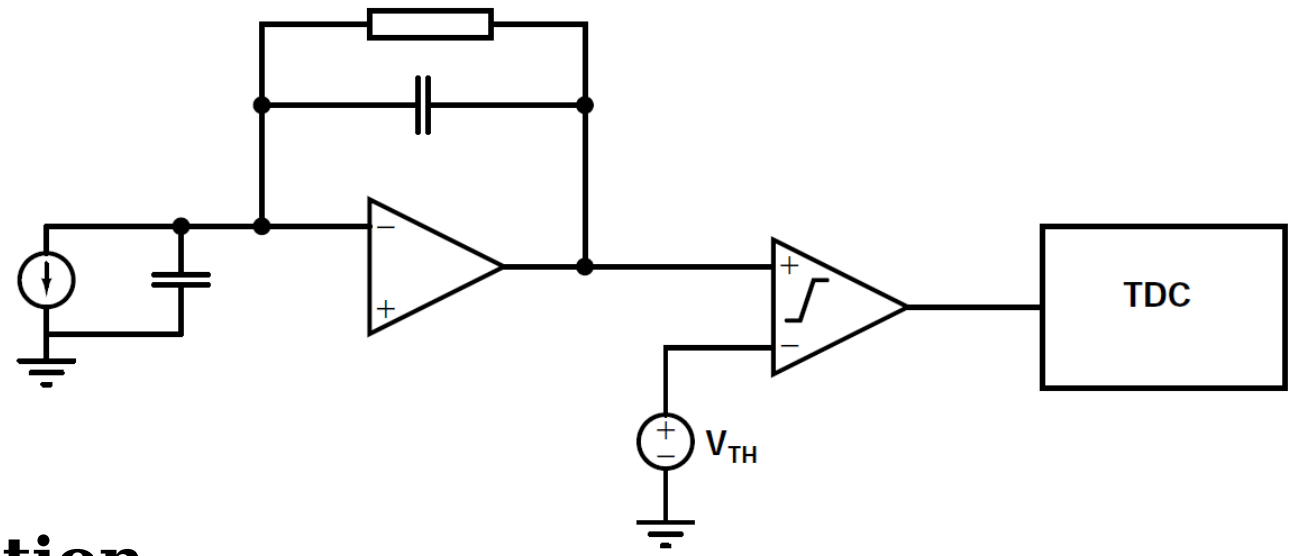
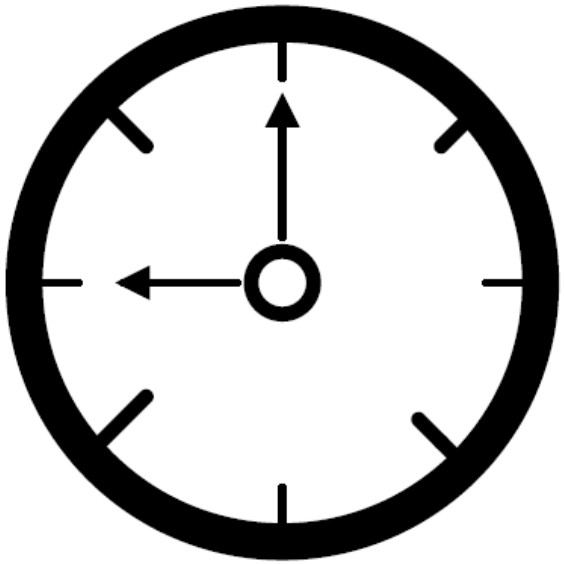
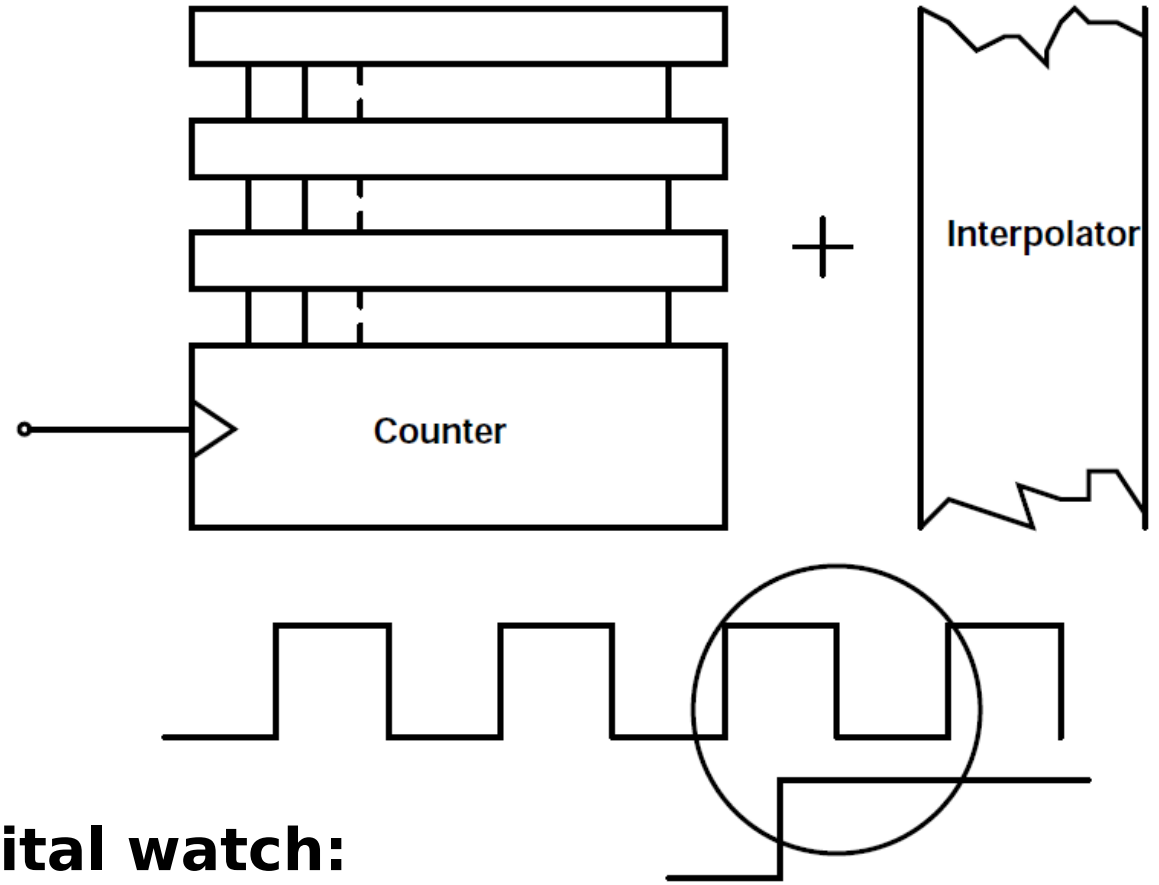
Outline



- **Introduction**
- **Overview of recent trends**
- **TDC for distributed systems:**
  - **Ring oscillators**
  - **Time to amplitude**
- **Conclusion and outlook**

TDC basics



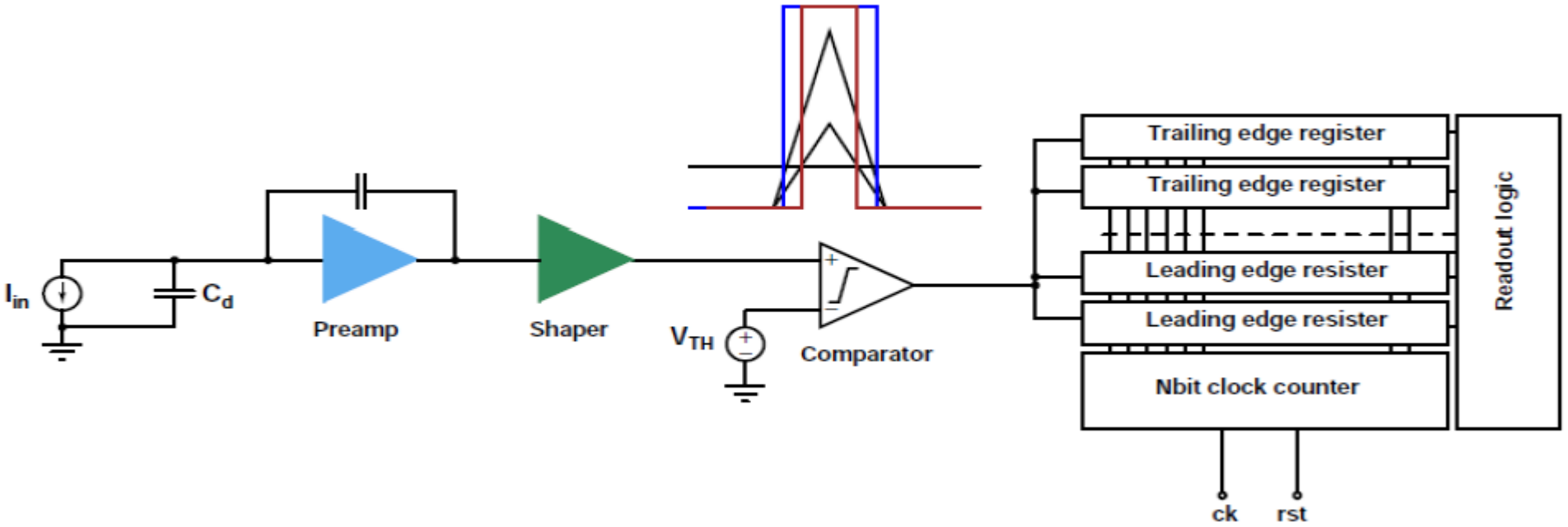


- **TDC = very accurate digital watch:**
  - **Sub 100 ps resolution;**
  - **Multi-channel (> 100) ;**
  - **Compact, low power and high rates.**

Interest of multi-channel TDC

- **Indispensable in high granularity timing systems:**
  - **Time resolved photon counting (analog and digital silicon PM).**
  - **4-D Tracking in HEP**
  - **Time-domain ADC.**

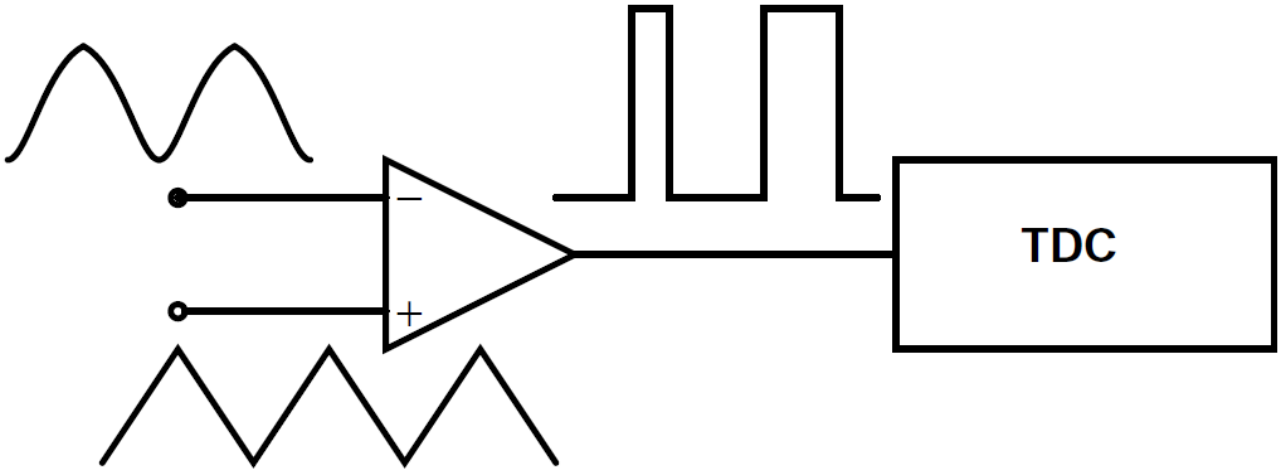
- **TDC=only digital gates or (in a few cases) analog circuits with low dynamic range: suitable for deep submicron technologies.**



2084 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 9, SEPTEMBER 2011

A 0.8 ps DNL Time-to-Digital Converter With 250 MHz Event Rate in 65 nm CMOS for Time-Mode-Based ΣΔ Modulator

Mohamed M. Elsayed, *Student Member, IEEE*, Vijay Dhanasekaran, *Member, IEEE*, Manisha Gambhir, *Member, IEEE*, Jose Silva-Martinez, *Fellow, IEEE*, and Edgar Sánchez-Sinencio, *Life Fellow, IEEE*



Trends in TDCs

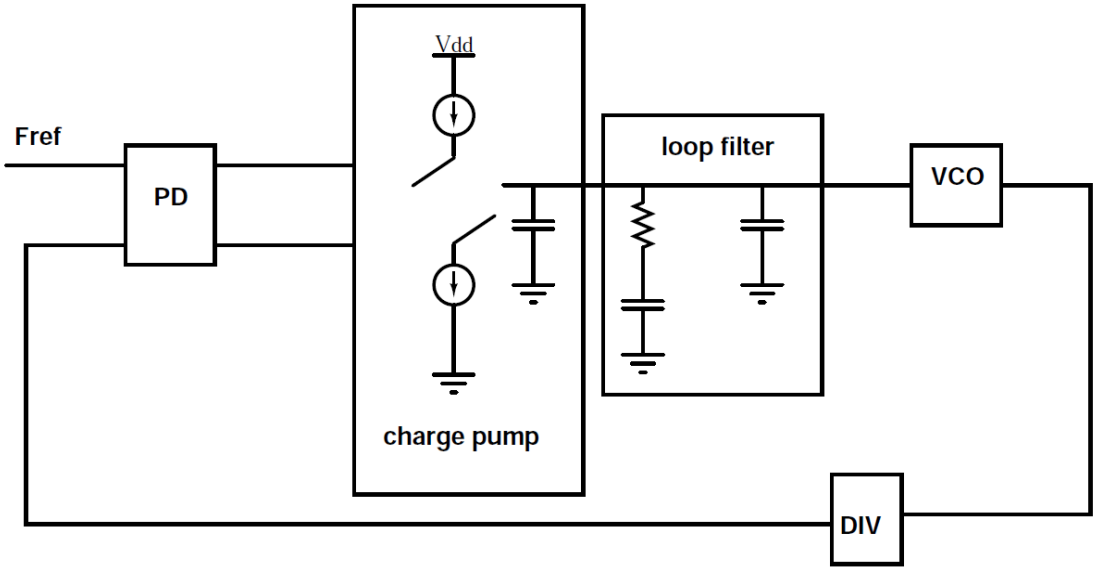
- TDCs were traditionally **stand-alone** components implemented on **dedicated** chips.
- Increasing interest in **embedded solutions**, where the converter is **part** of more complex ASICs.
- **Area** and **power consumption** are key parameters for embedded designs.
- ULSI technologies (**130 nm** and below) **not indispensable** for very good time resolution...
- ...but needed for **compact** cell size and **low power**.

Most published works on embedded TDC design address:

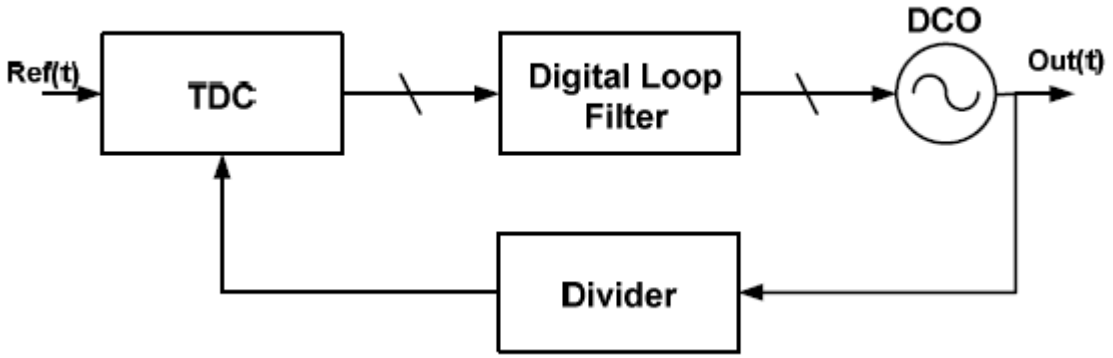
- ALL Digital PLL
- Digital SiPM

TDC in ADPLL (1)

Due to ADPLL, TDC became more general purpose components, with an significant increase on the number of published papers in the recent years.



Conventional analog PLL
Needs an analog filter



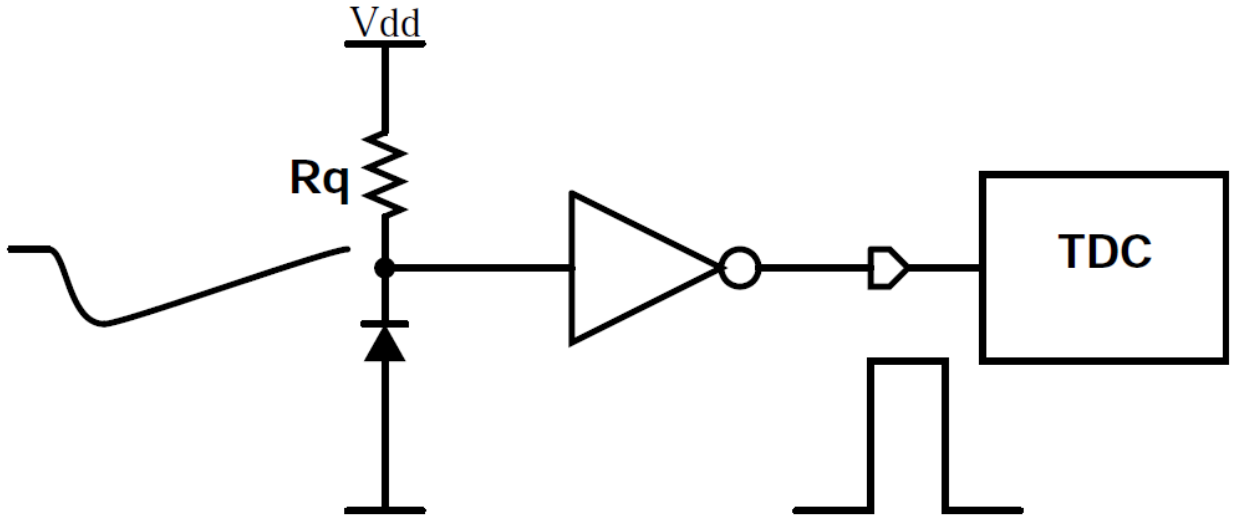
ALL Digital PLL
Phase difference measured with a TDC

TDC in ADPLL (2)

Ref	Technology	Architecture	Resolution (ps)	Sampling rate (MS/s)	Range (ns)	Power (mW)	Area (mm^2)
1	130 nm	GRO	1	50	12	2.2-21	0.04
2	130 nm	Vernier-ring	8	15	32	7.5	0.26
3	90 nm	Passive inter.	4.7	180	0.6	3.6	0.02
4	90 nm	Delay line	20	26	0.64	6.9	0.01
5	65 nm	2D delay line	4.8	50	< 0.6	1.7	0.02
6	90	Time Amp.	1.25	10	0.64	3	0.6
7	90	Vernier+GRO	3.2	25-100	40	3.6-4.5	0.027

- TDC in ADPLL targets extremely good resolution;
- Dynamic range less of a concern;
- Many different architectures;
- Timing resolution of future detectors will not be limited by the TDC.

TDCs in digital SiPM (1)



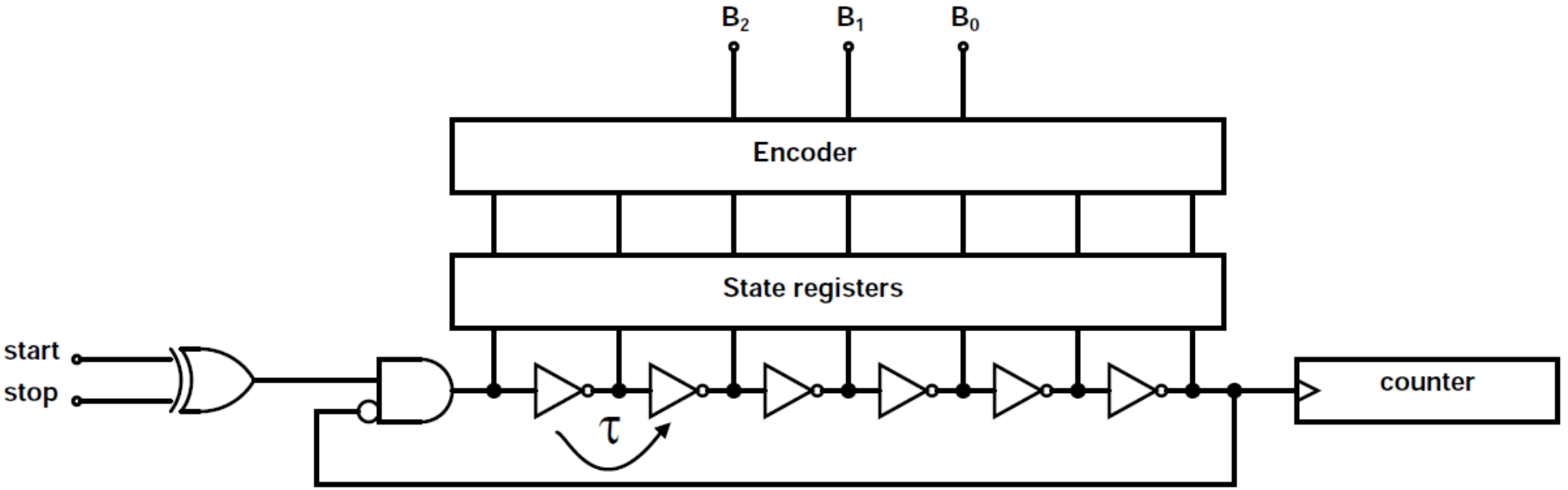
- Geiger mode sensor + front-end electronics in single chip;
- Typical pixel size: 50 um x 50 um to 300 um x 300 um;
- Sensor design not trivial: HV CMOS or imaging process used.

TDCs in digital SiPM (2)

Ref	Technology	Architecture	LSB (ps)	Range (ns)	Power (mW)	Area	Dead time (ns)
1	130 nm CIS	Delay lines	62.5	64			
2	350 nm HV	Delay lines	80	3.5			
3	350 nm	Delay lines	10	160	15	0.3 mm2	150
4	130 nm	GRO	55	55	0.64	< 50 um x50 um	
5	130n	GRO	64.56	261.59	1 mW		

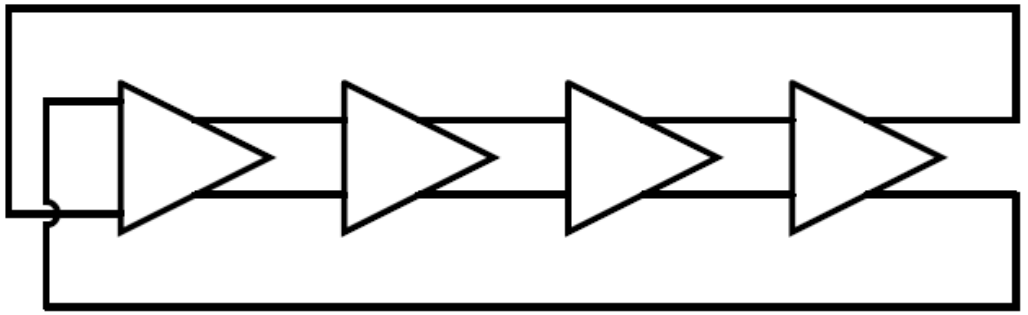
- Massive parallelism
- Low power
- Good but not extreme time resolution

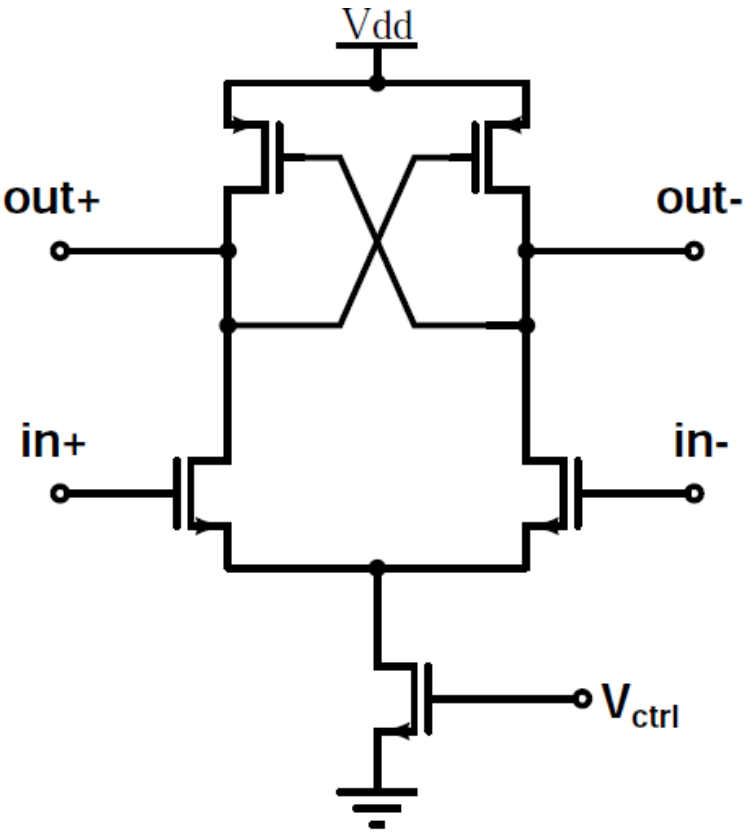
Ring oscillators



- Feed-back loop encompassing an odd number of inversions
- Binning=τ
- Latency=1/(Nτ)
- Oscillator active only when measuring.
- Compact and low power. Adequate as local TDC in pixellated systems.
- Sensitive to: Process, Voltage Supply, Temperature (PVT), matching..

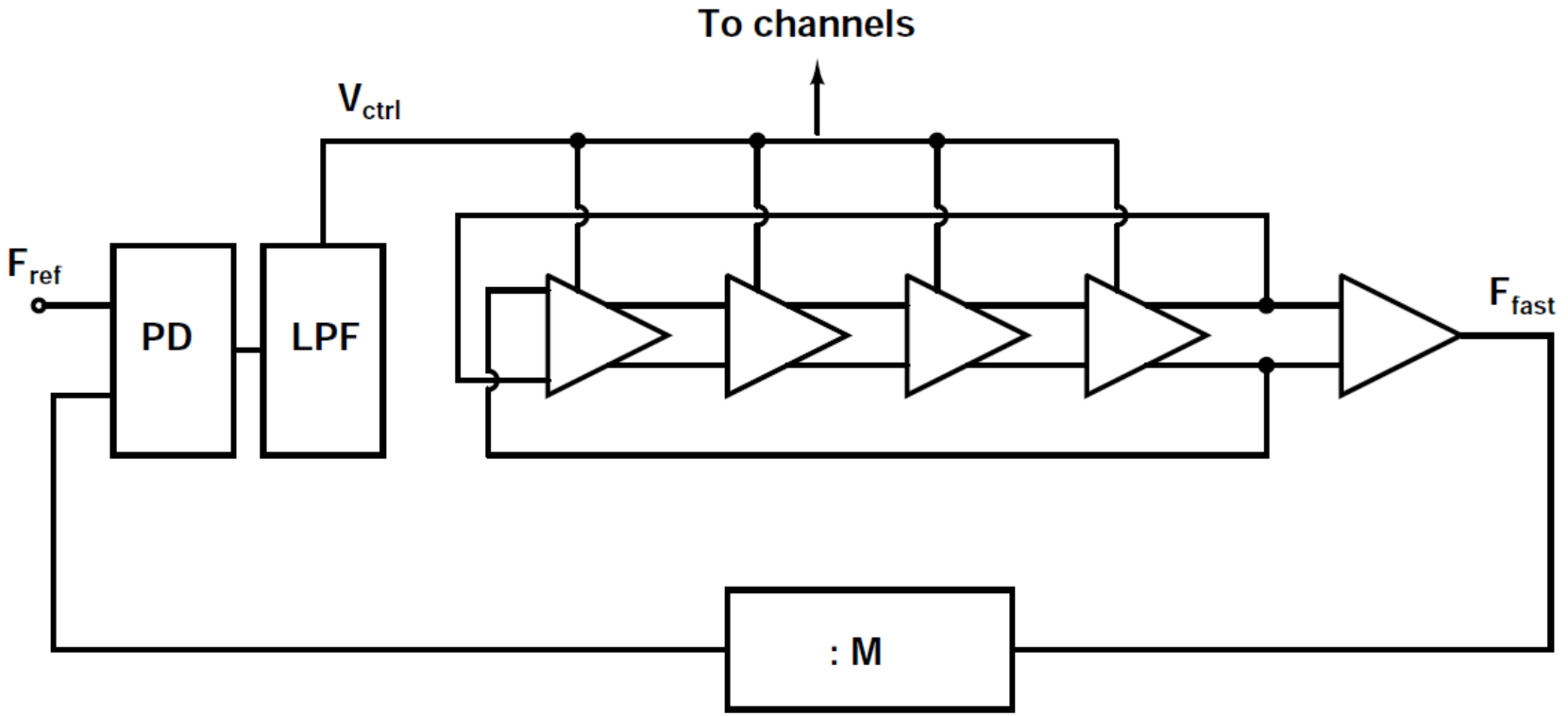
Differential RO topology





- **Differential structures improve PSRR**
- **Both phases can be used: 8 states from 4 differential cells**
- **PVT not yet adequate for high performance TDC.**

PVT stabilization through PLL



- **Ideally, each oscillator should be controlled by a PLL loop: cumbersome for distributed implementation (LPF area).**
- **Replica oscillator in PLL and distribution of the control low frequency signal.**
- **Mismatch between oscillators an issue.**

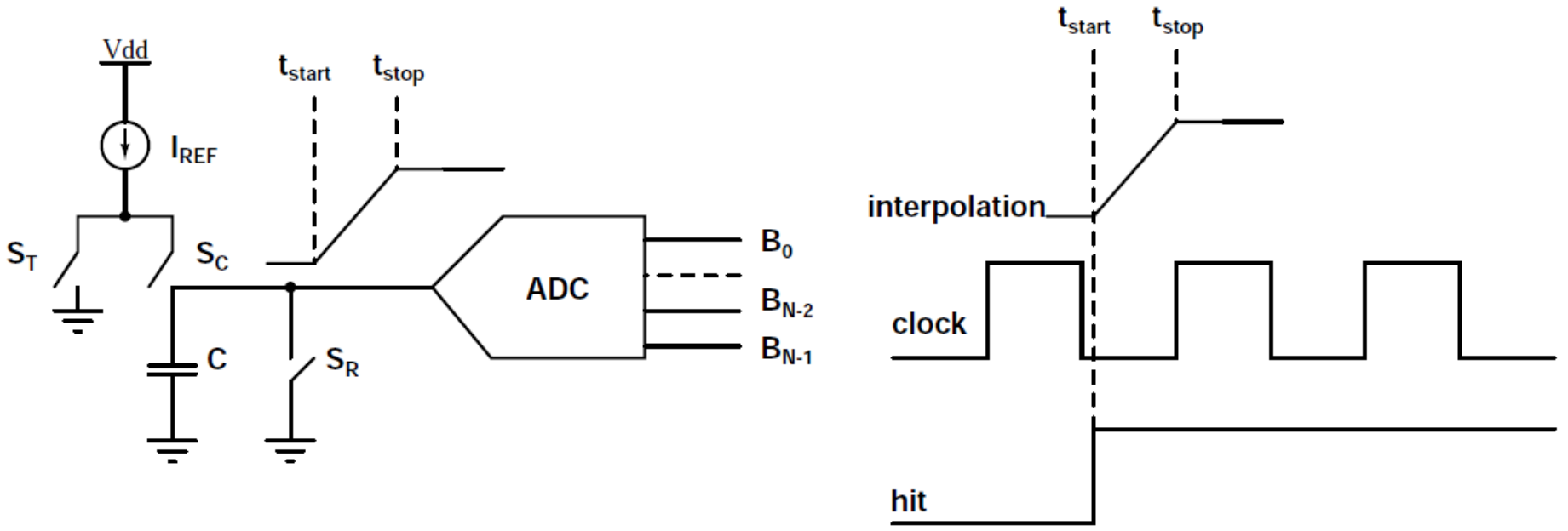
Towards used in HEP

GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors

C. Brezina, Y. Fu, F. Zappon, M. van Beuzekom, M. Campbell, K. Desch, H. van der Graaf, V. Gromov, R. Kluit, X. Llopart, T. Poikela, and V. Zivkovic

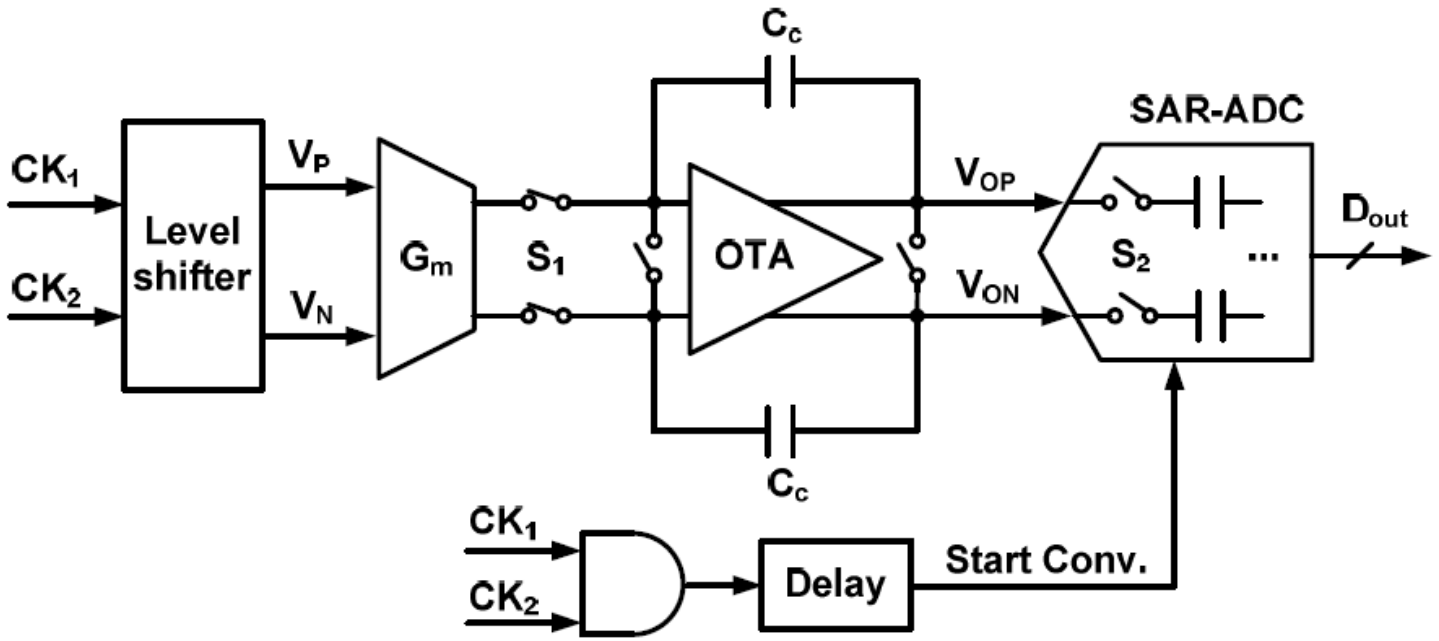
- **640 MHz ring oscillator.**
- **1.56 ns binning.**
- **40 MHZ x 16 clock multiplication**

Back to the origin: TAC



- **Charge a capacitor for the time to be measured and digitize the voltage.**
- **Requires ADC**
- **Today SAR ADC: 10 bit, 50 MS/s, 1 mW, 300 μm x 300 μm in 0.13 μm CMOS**
- **Interpolate 6.25 ns with 10 bits: 6 ps.**
- **Area for a 7 bit ADC (48 ps binning) 80 μm x 80 μm.**
- **Conversion time: O (50 ns)**
- **Estimated power at 1 MHz rate: < 0.5 mW**

Recent design and performance



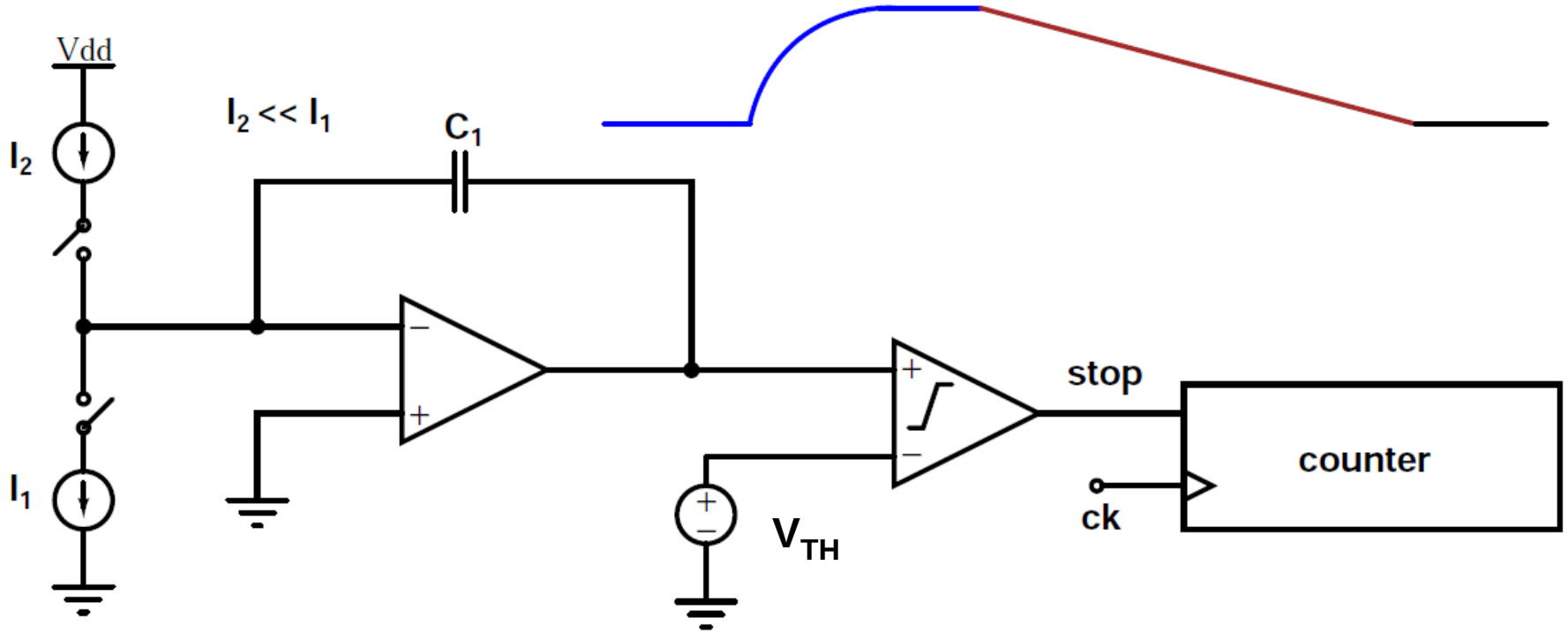
Zule Xu, Masaya Miyahara, and Akira Matsuzawa

A 1ps-Resolution Integrator-Based Time-to-Digital Converter Using a SAR-ADC in 90nm CMOS

IEEE 2013 NeW System and Circuit Conference (NEWCAS)

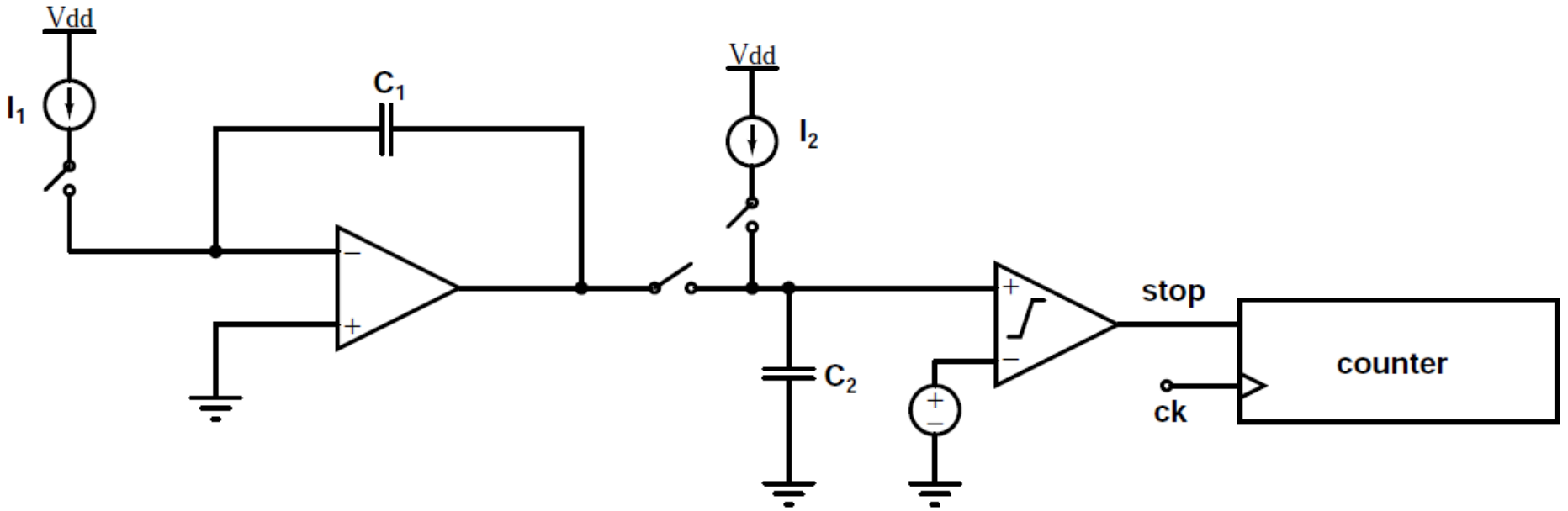
- **Time bin: 1ps**
- **Range: 9 bits**
- **Power: 20 mW**

The simplest: TAC + Wilkinson



- **Current flowing in opposite directions: NMOS and PMOS current source-matching issue.**
- **I_1 larger than I_2 : output impedance of I_1 smaller: virtual ground helps, although not indispensable.**
- **Amplifier does not need to keep a linear rising edge: bandwidth not a major issue.**
- **Clock: 12.5 ns: binning 100 ps I_1/I_2 128**

Building block details (1)

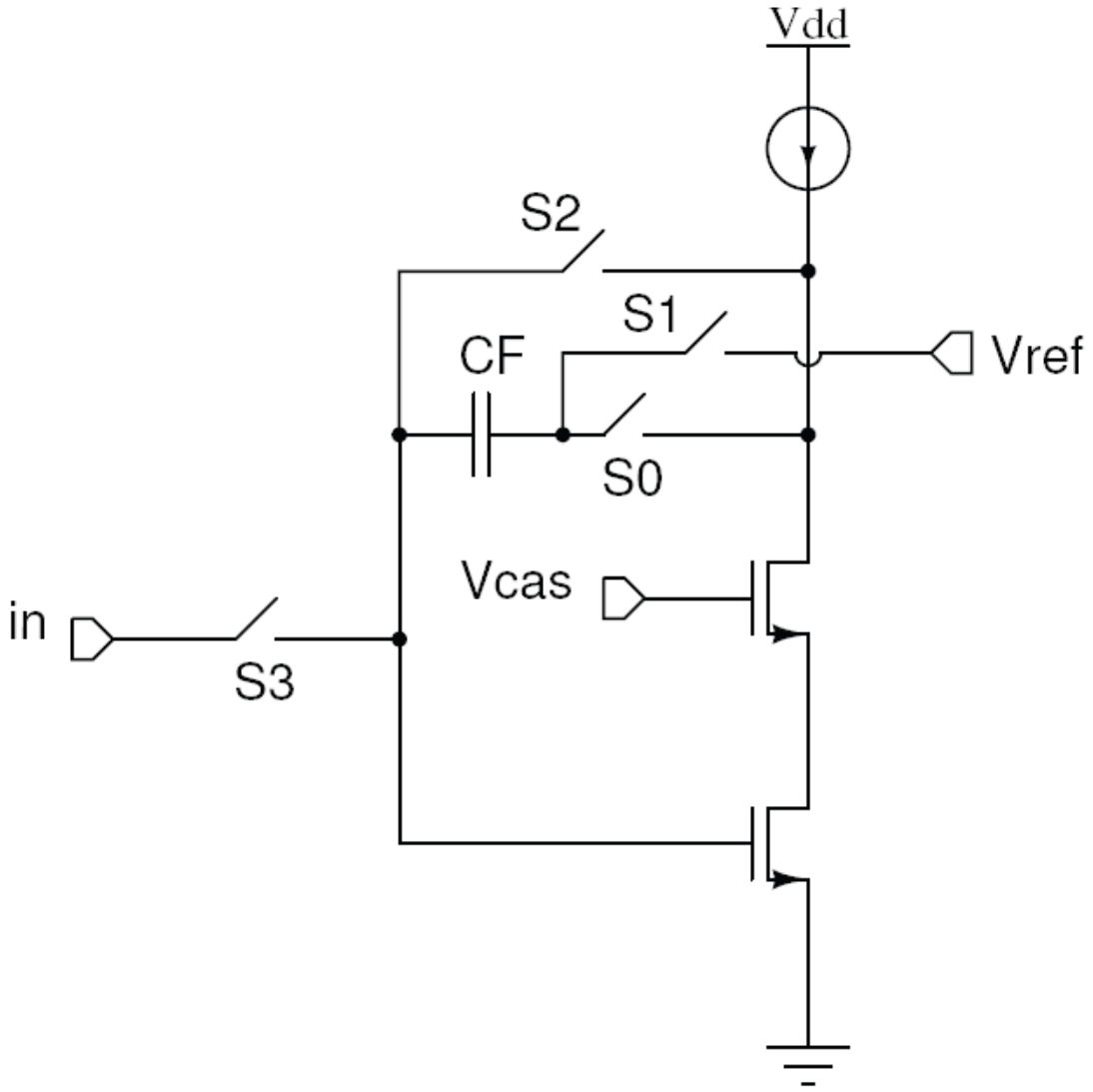


- Charge is transferred on C_2
- $C_2 = 4C_1$
- Ck=2 TDCck
- $I_1/I_2=16$

- Compact design
- Only capacitor and current ratio counts
- Easy to calibrate
- PVT stable

- Time interleaving for moderate rates (up to 1 MHz/channel)

TAC detail

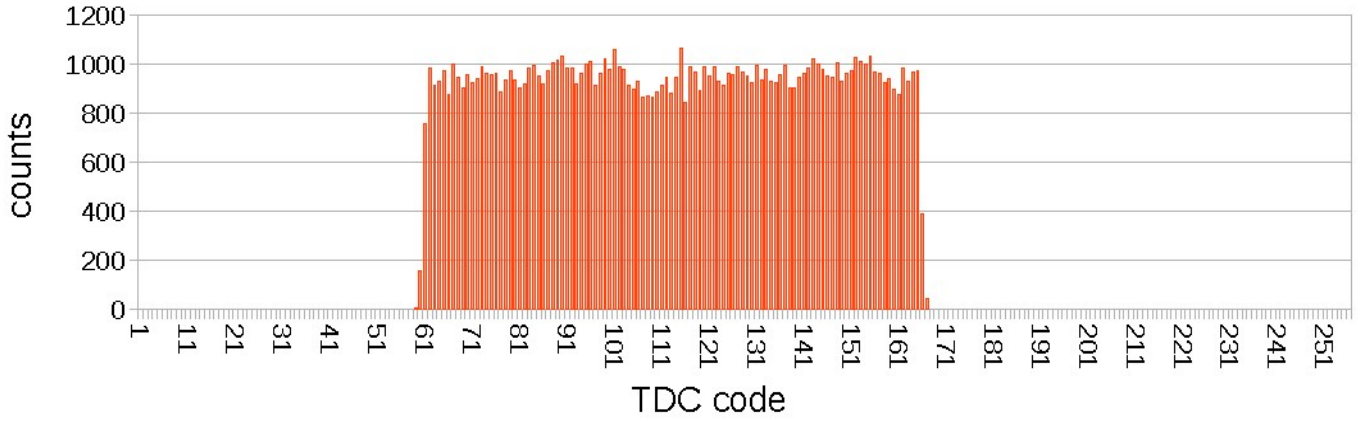


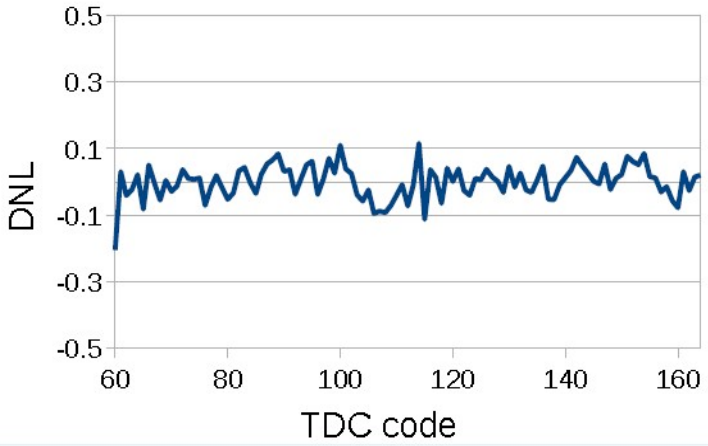
1. Reset/Arming:
S0, S3 open, S2, S1 closed

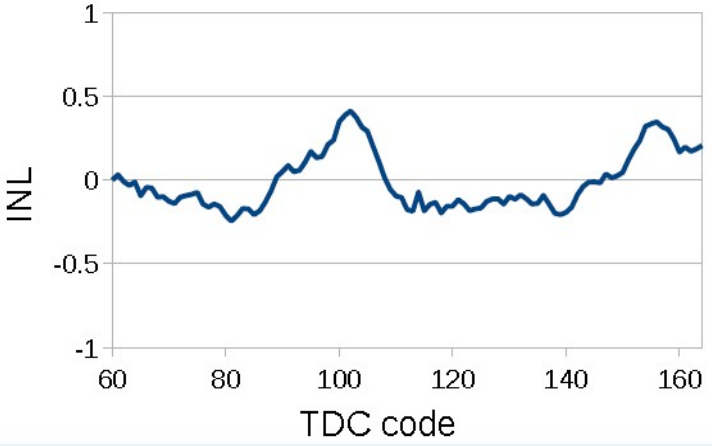
2. Idle
S0 closed, S1, S2, S3 open

3. Charging
S3, S0 closed, S1, S2 open.

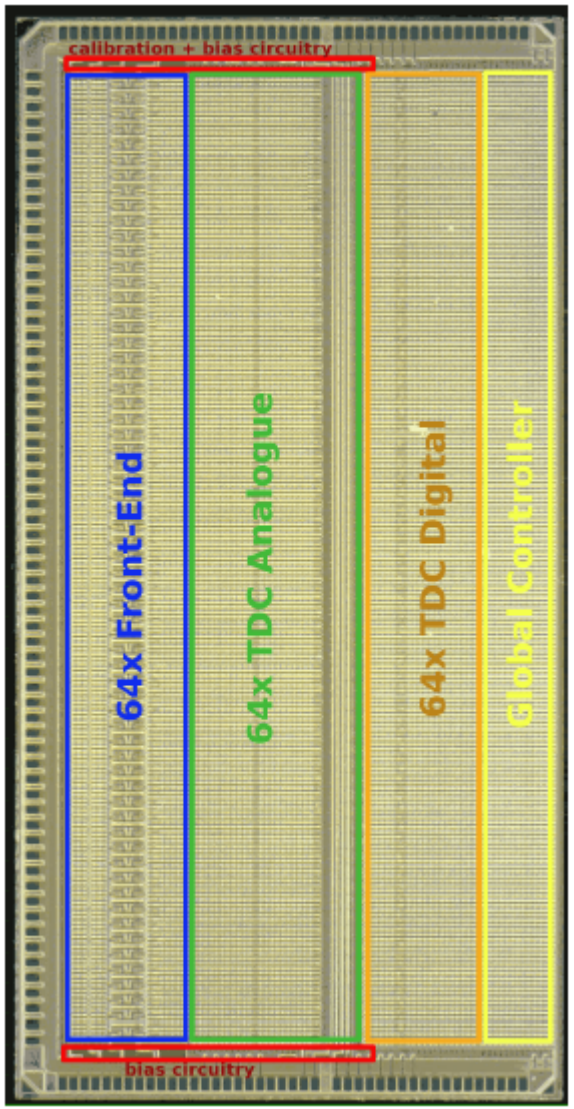
DNL – INL testing



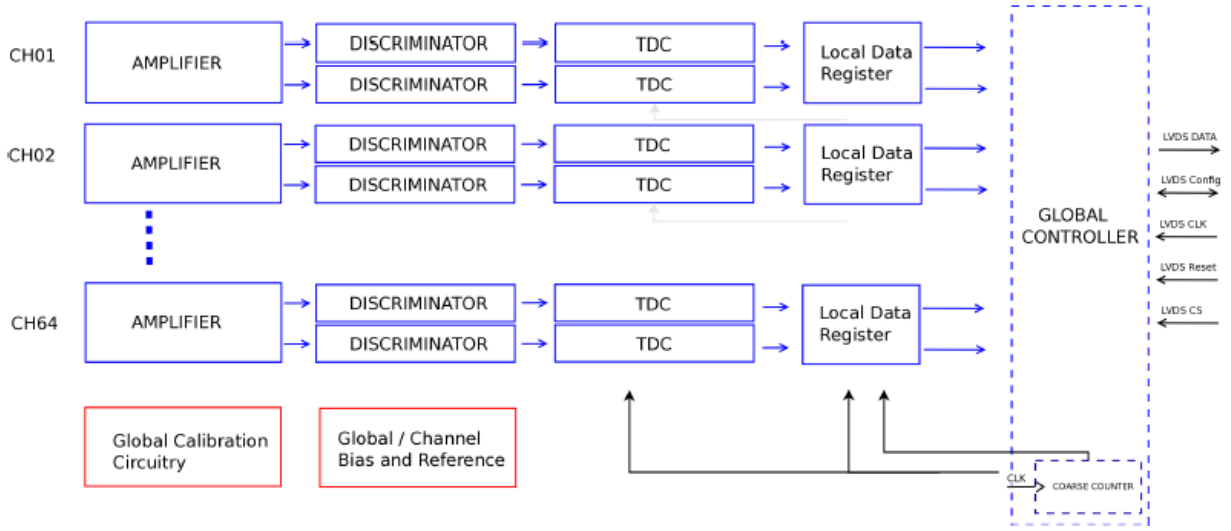




Example of chip using TAC



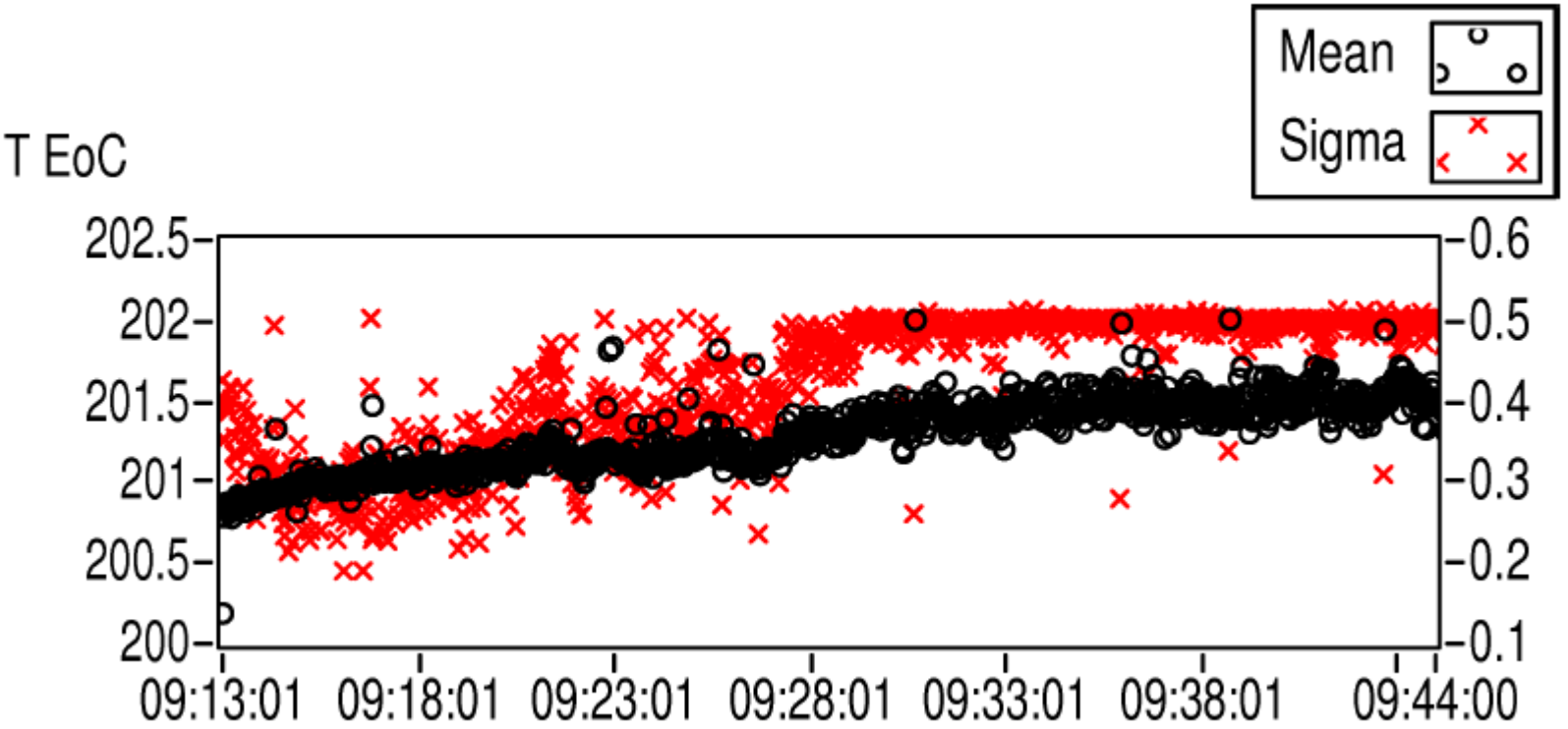
M. Rolo et al. "TOFPET ASIC for PET applications



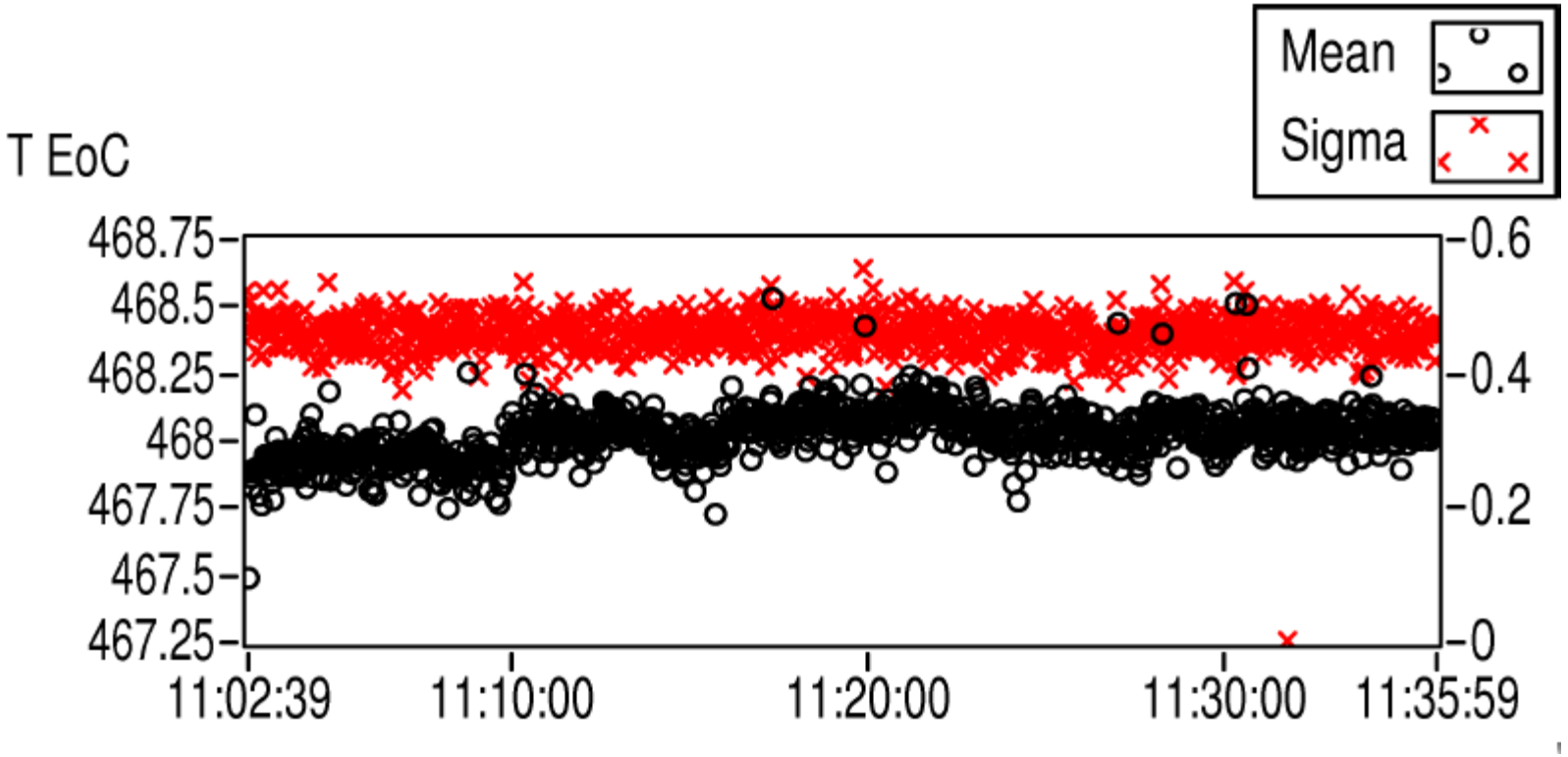
Readout for analog SiPM

2 TDC per channel with four time-interleaved TAC
Scalable binning down to 25 ps.
Rate > 100 kHz per channel

Temperature stability

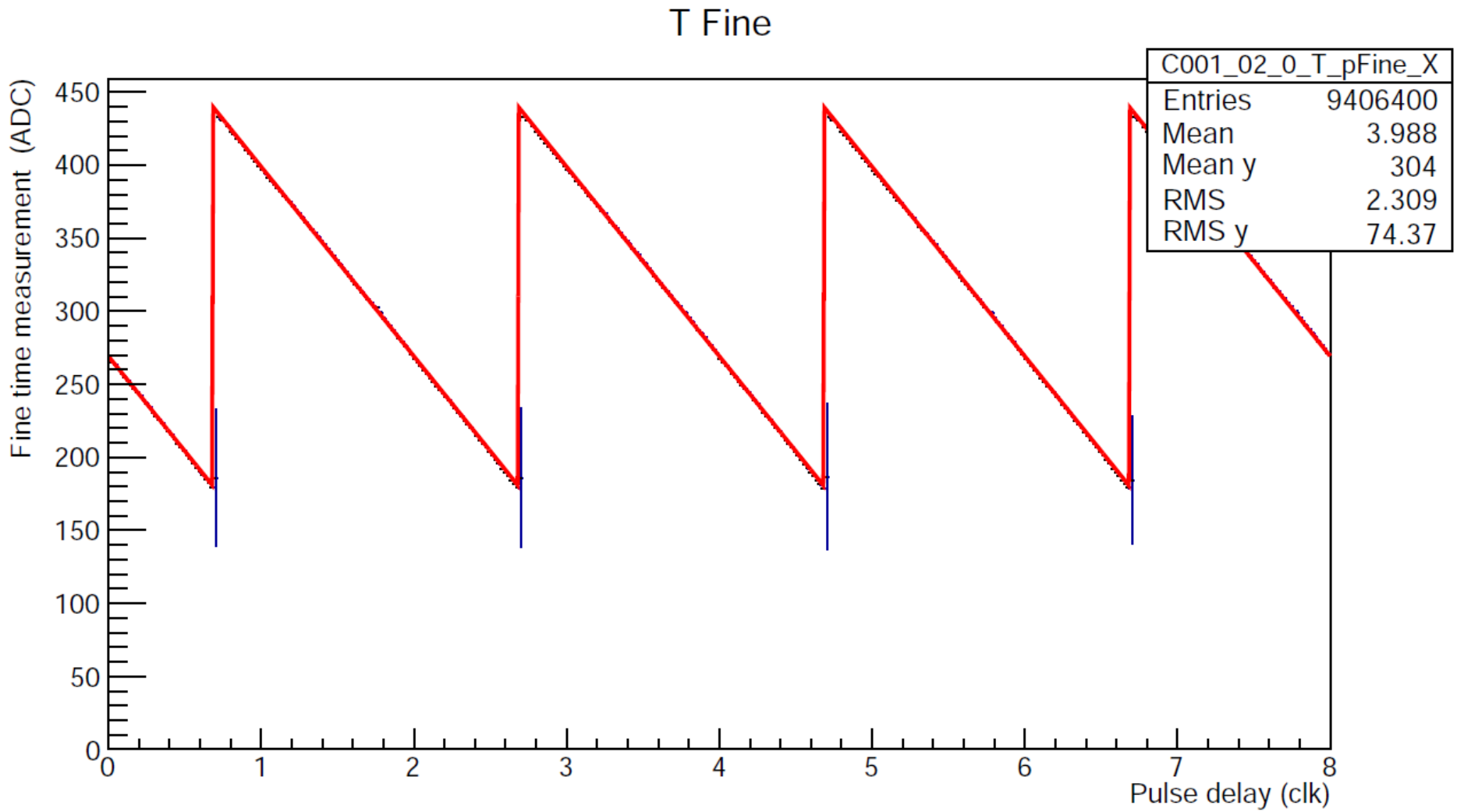


Long term stability

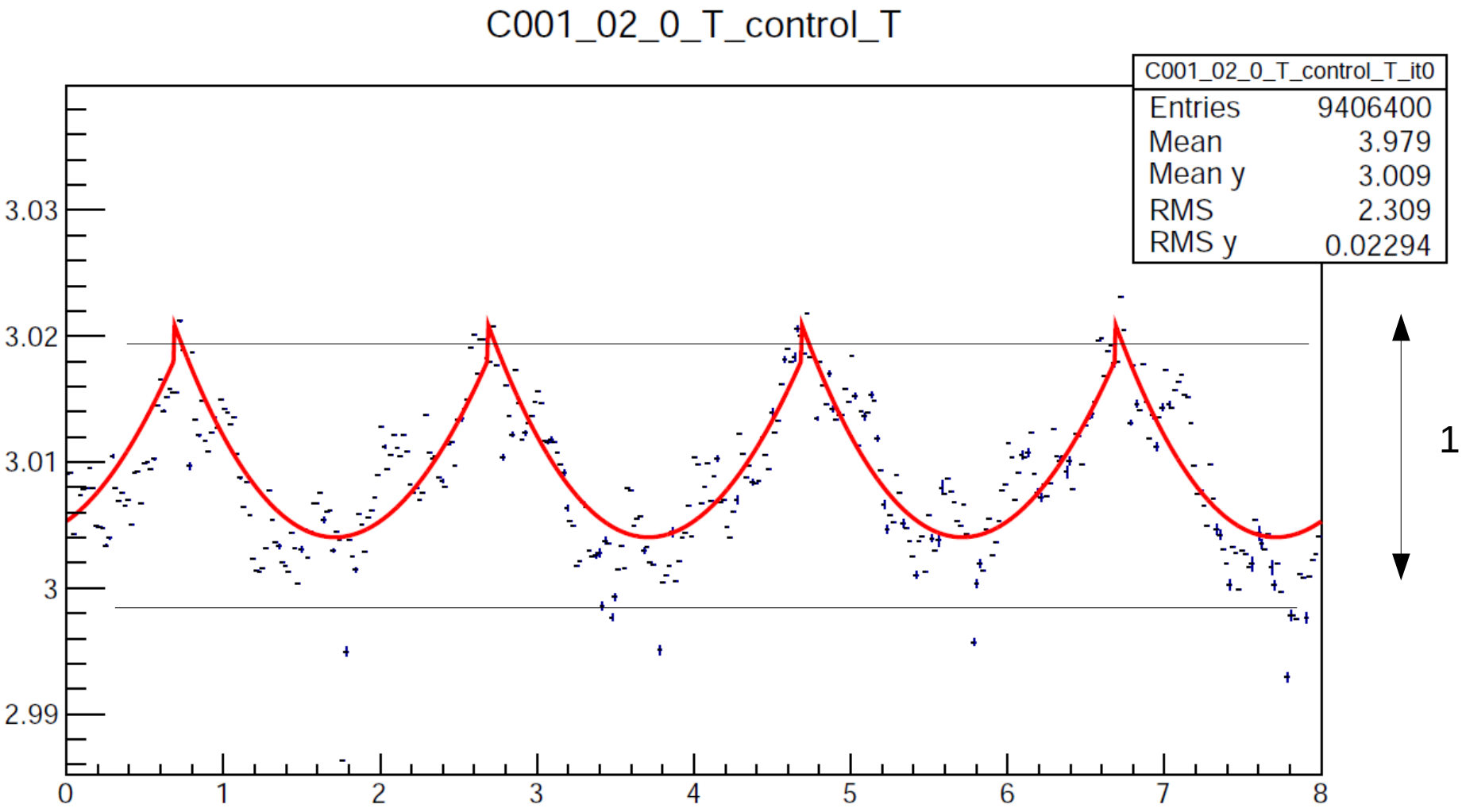


- In SC circuits important to check long term stability
- Potential problems from charge build-up due to incomplete reset.
- TDC running at 80 kHz average rate

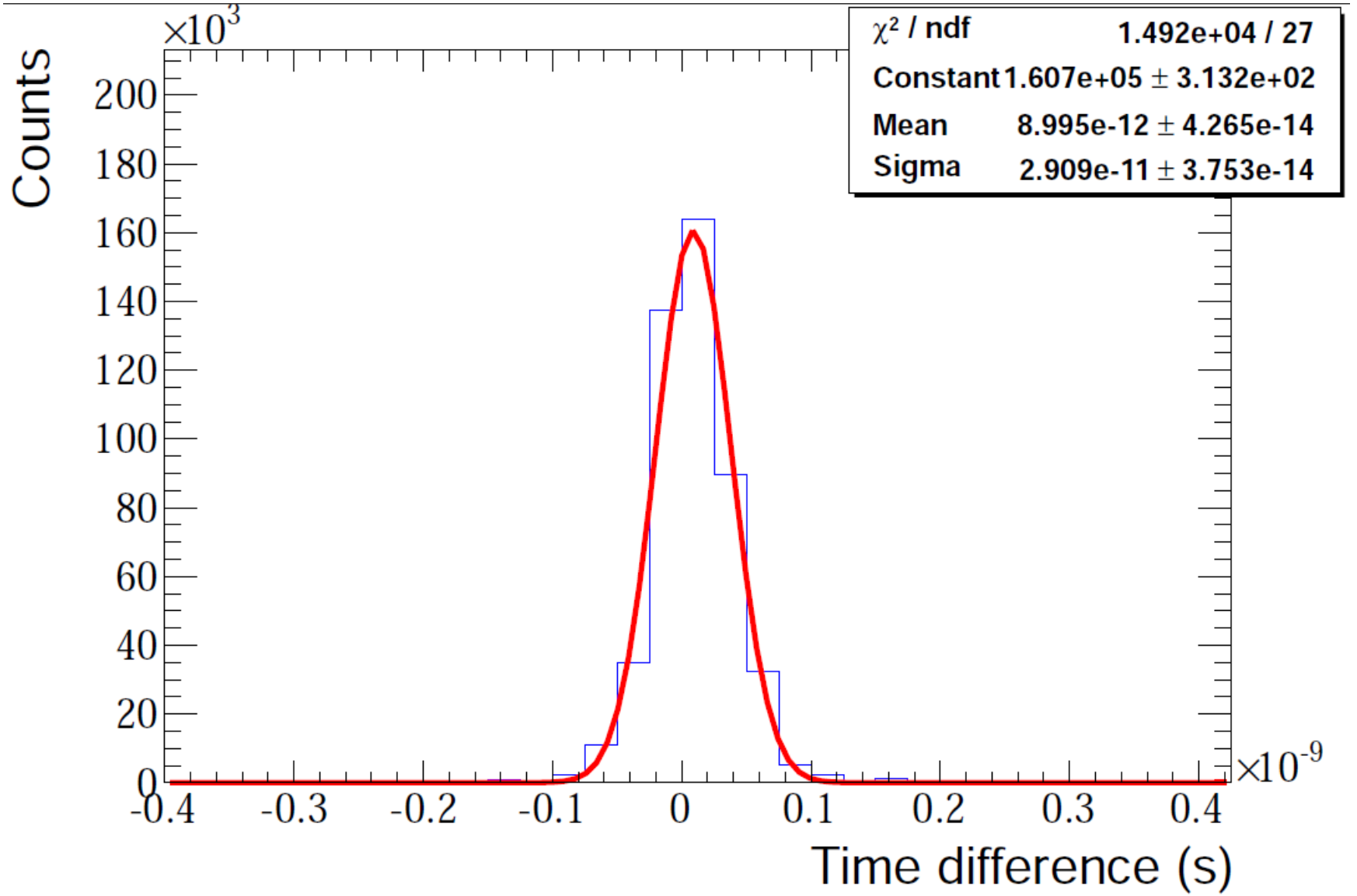
Fine time pattern...



Residual non-linearity

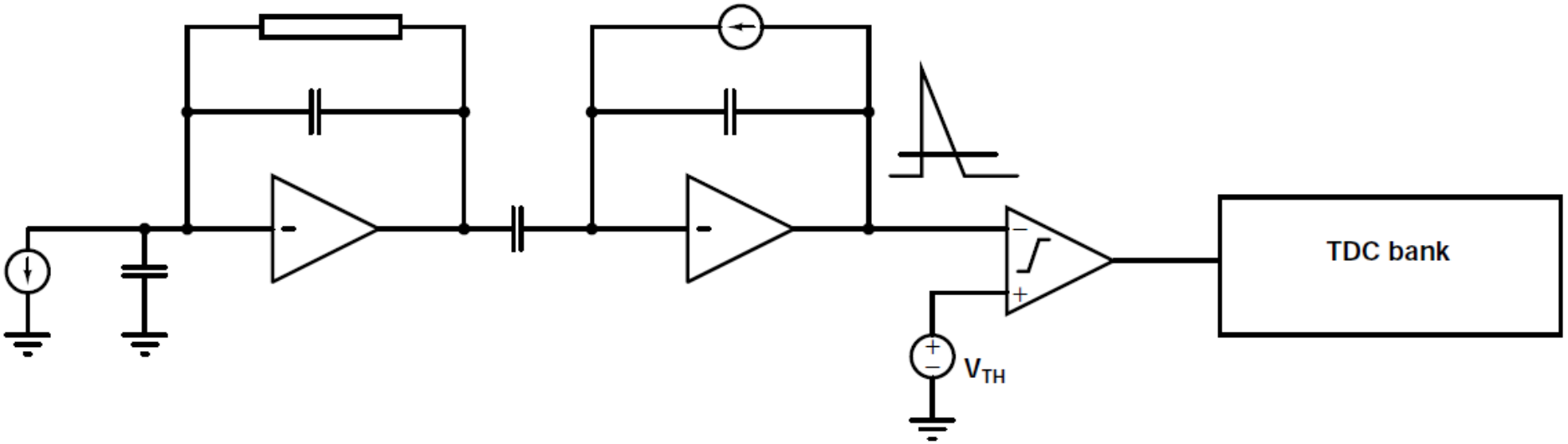


Limits on timing: jitter



Time-based readout of strip sensors

- On going project for the PANDA MVD.
- Triggerless detectors with 10E7 $p\bar{p}$ interactions per second.
- Rate O(40 kHz)/strip
- Time resolution O (ns)....



- FAST ToT + TDC
- ToT stage can saturate still providing a linear charge measurement
- Sampling the charge using only timing circuitry.
- Slower clock + interpolation provides smaller power

Summary and outlook

- A lot of progress recently made in TDC design.
- TDC can be implemented on a per-channel basis in front-en ASIC for radiation detectors.
- Time base readout=accurate timing plus charge information with basically only digital circuitry.
- Electronics is ready for high granularity and high resolution timing system.
- Hitting sub-100 ps time resolution is mostly on the shoulder of sensor designers....

References

SPAD TDC

1. R. M. Field et al, *A 100-fps, Time-Correlated Single-Photon- Counting-Based Fluorescence-Lifetime Imager in 130-nm* **to be published in IEEE J. Solid-State Circ., April 2014.**

2. I. Nissinen et al., *A time-gated 4x128 SPAD array with a 512 channel flash 80 ps-TDC for pulsed Raman spectroscopy*, **2013 IEEE ECCTD Conf. Records.**

3. B. Markovic et al., *A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation*, **IEEE Trans. Circ. Syst. I, vol. 60, March 2013.**

4. C. Veerappan et al., *A 160x128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter*, **ISSCC, Feb. 2011.**