TWEPP 2013

A multichannel Time-To-Digital Converter ASIC with better than 3ps RMS Time Resolution

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24 September 2013

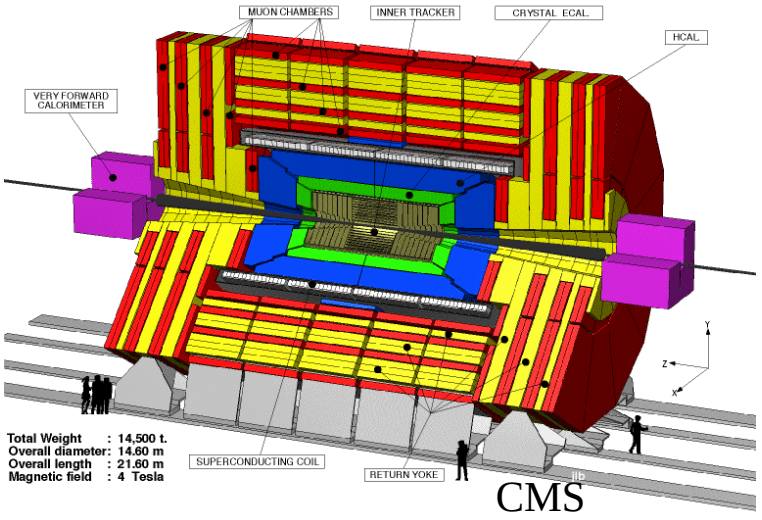
Outline

- **Time measurements in HEP**
- **Time-to-Digital Converter Concepts**
- **Challenges in Fine-Time Resolution TDC Design**
- **Demonstrator architecture and implementation**
- **Measurement Results**
- **Conclusion**

TDC applications

HEP:

- Large systems
  - ~100k channels
  - Time resolution and stability across whole system
    Common time reference for all the channels
- Single shot measurements
- Hit rates: KHz - MHz
- Detector time resolution sets requirements for TDC

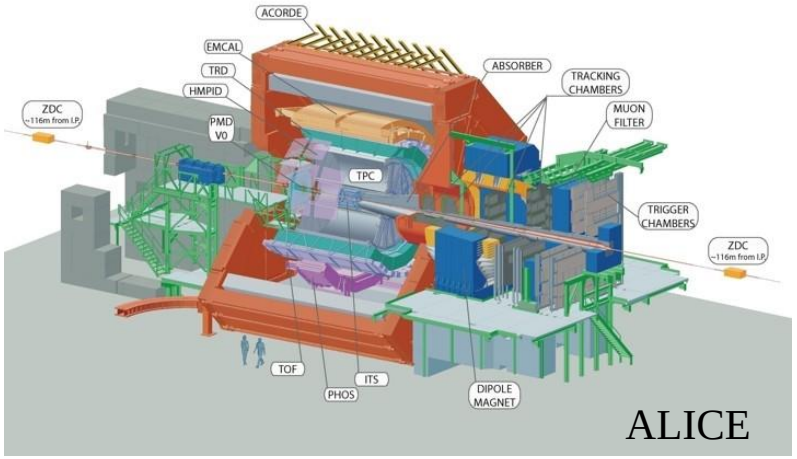


Drift time in gas based tracking detectors

- Low resolution: ~1ns
- Examples: CMS and ATLAS muon detectors

Time of flight detectors

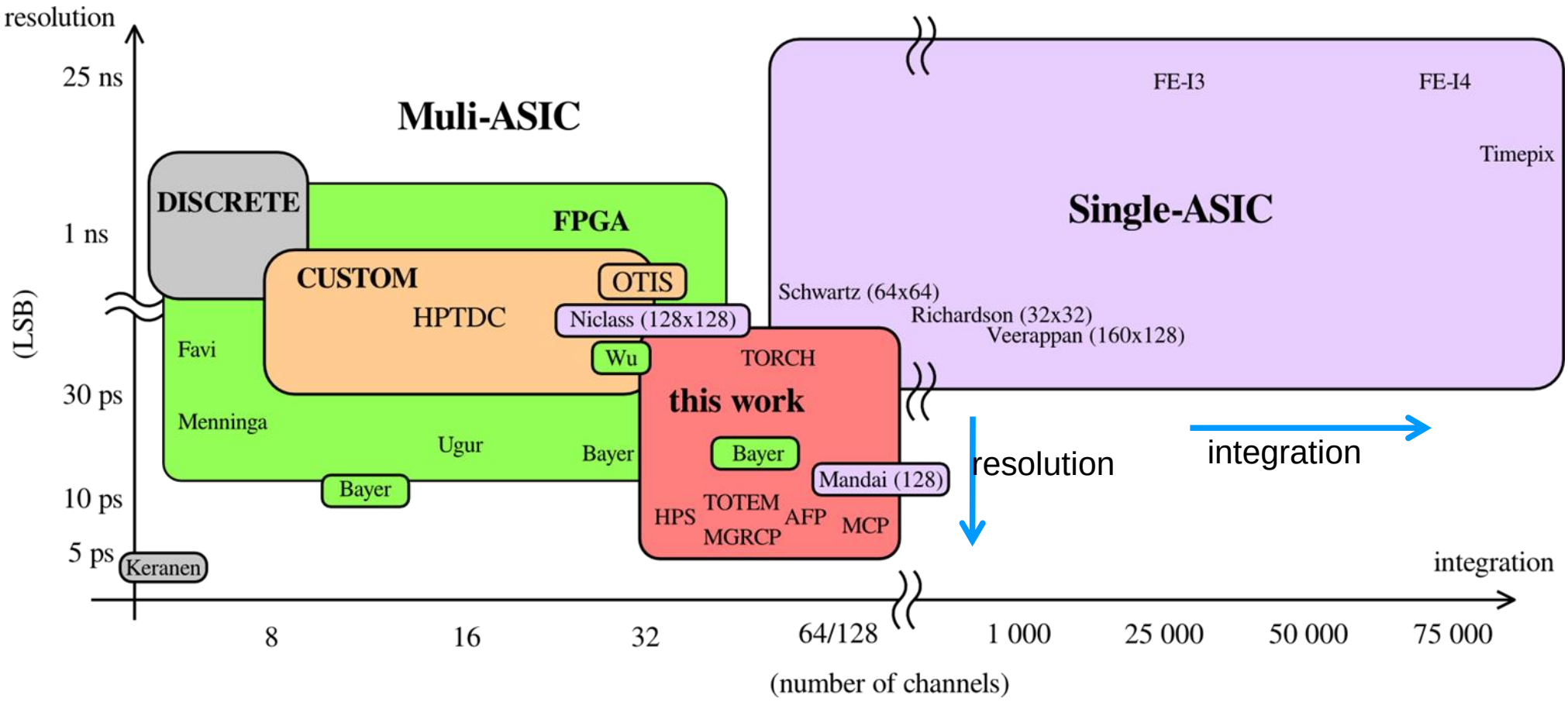
- **High resolution: 10ps – 100ps**
- Example: ALICE TOF
- New detectors: CMS HPS, ATLAS FP420, LHCb Torch, Totem, Fast forward detectors, etc.



Non HEP:

Laser ranging, Radar, On chip instrumentation, Imaging systems (PET, 3D imaging), etc.

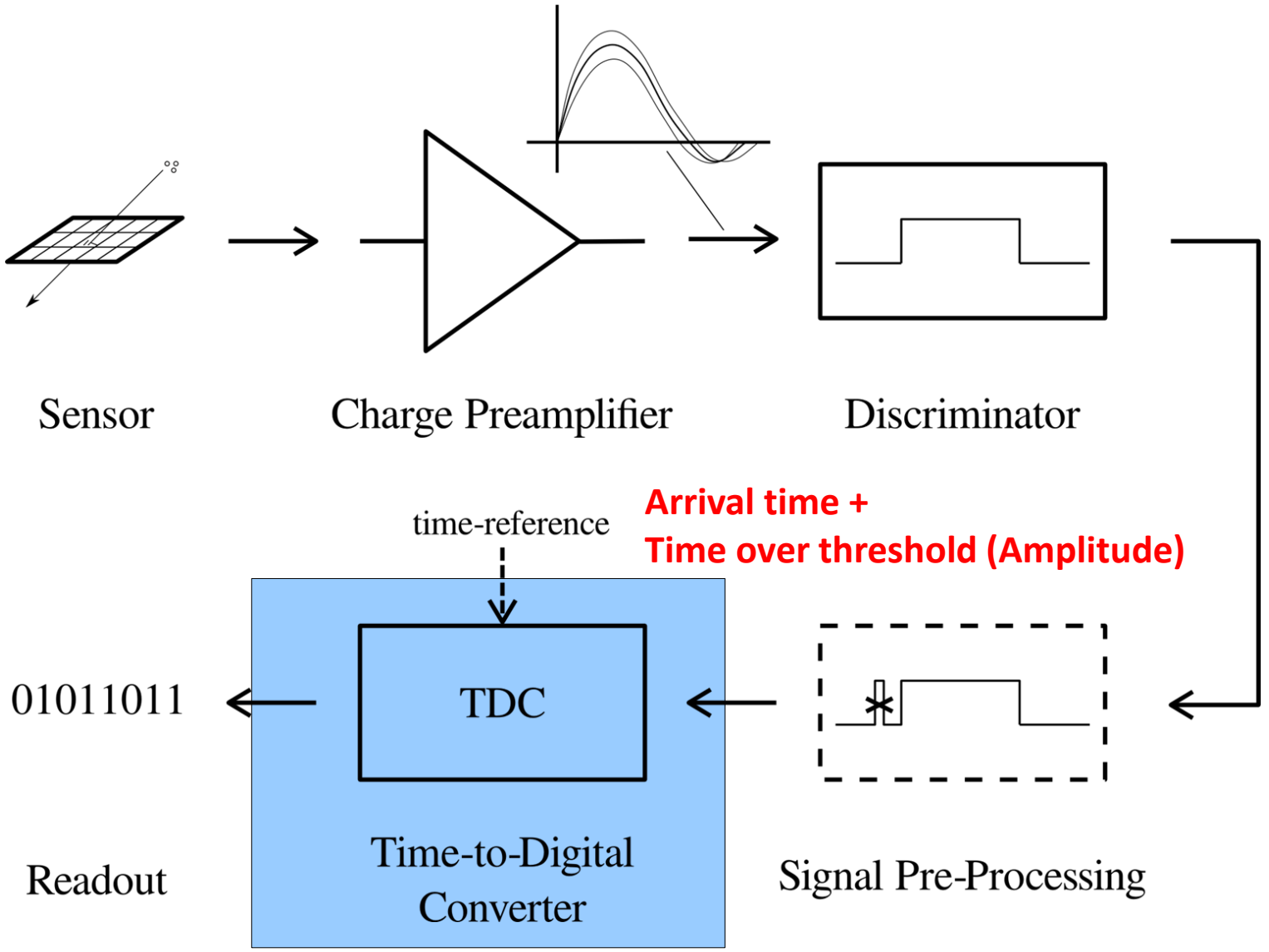
TDC Trend in HEP



New detectors and sensors require new TDC

- **~5 ps resolution**
- **High integration**
- **Flexible**

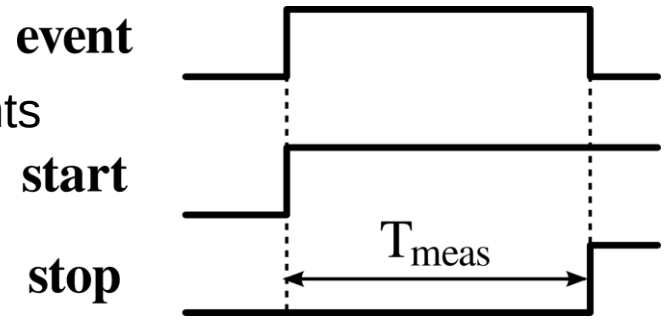
Time Measurement Chain



Time Measurements

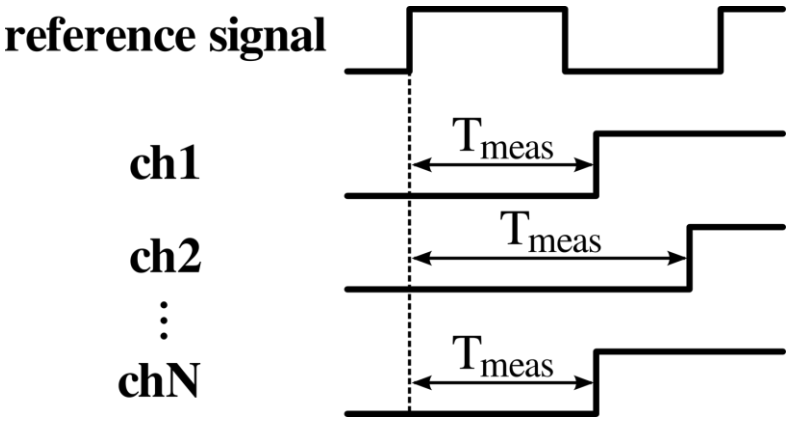
Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

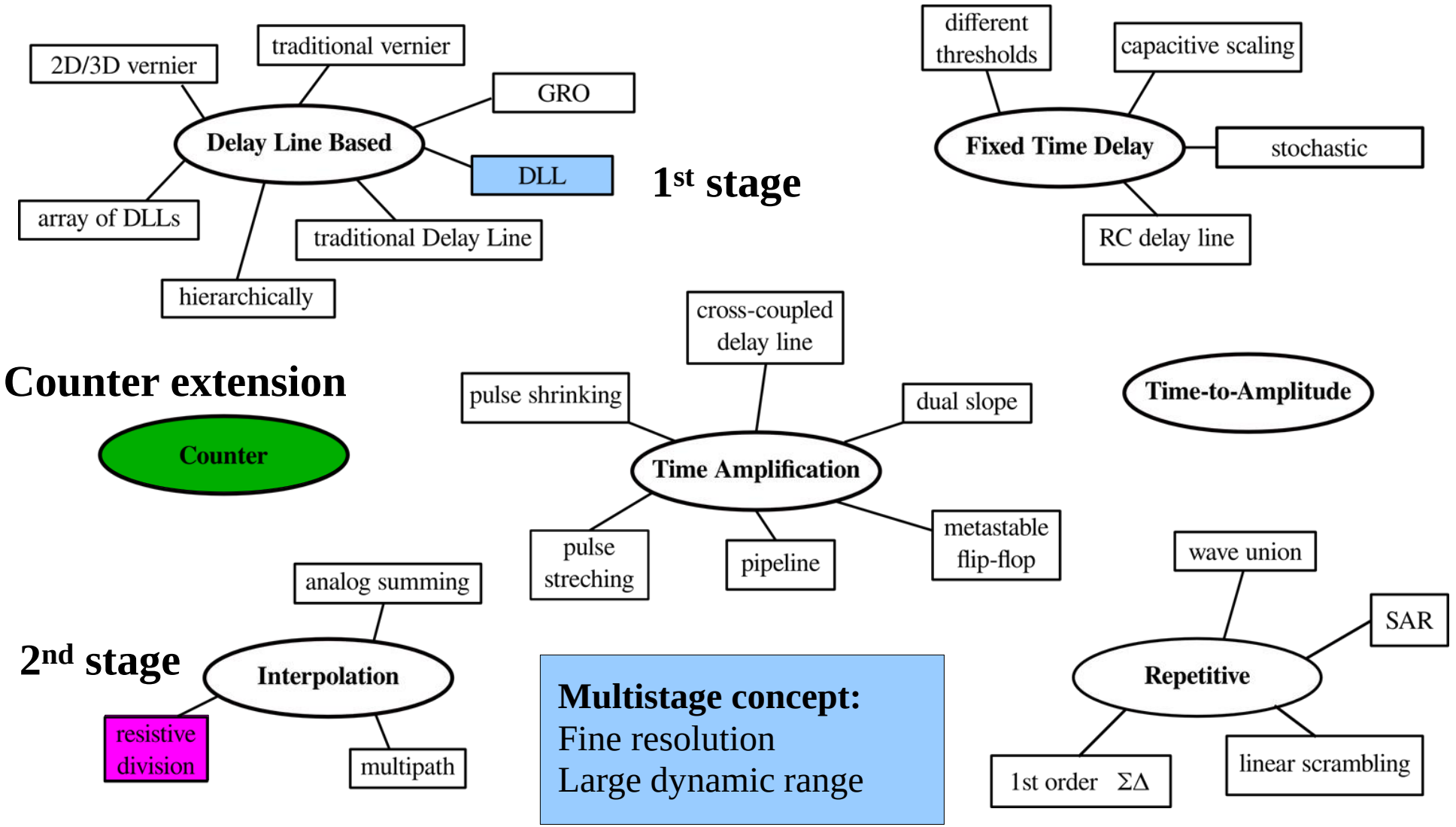


Time Tagging

- Measure “absolute” time of an event
  (Relative to a time reference: clock)
- For large scale systems with many channels
  all synchronized to the same reference



TDC Architectures

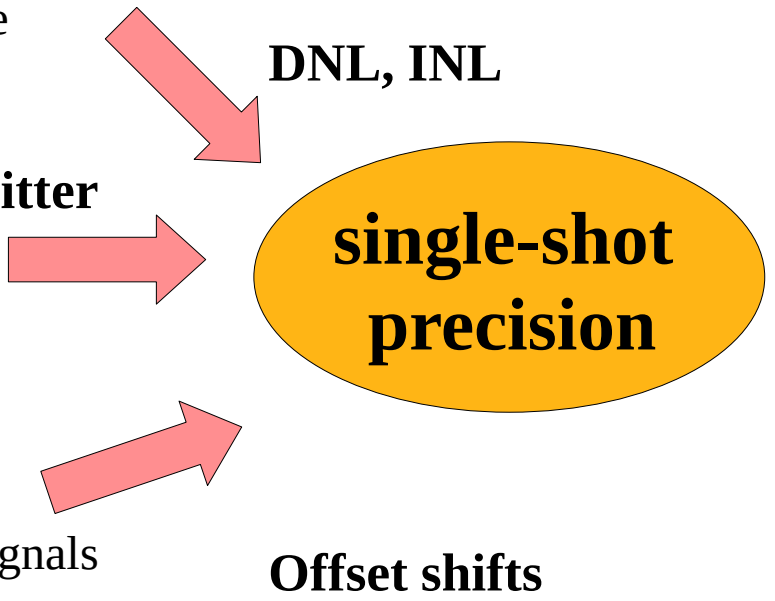


Difficulties in ps range resolution

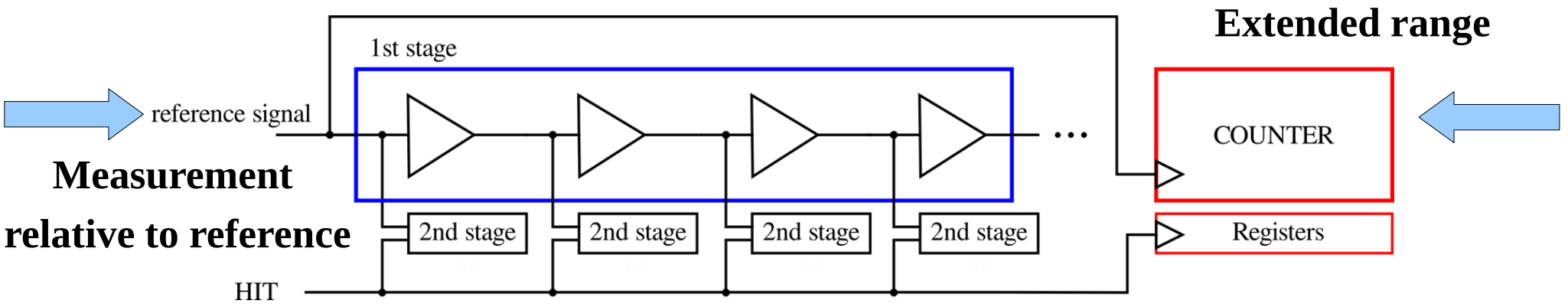
LSB/sqrt(12) ≠ rms

It is not worth making a fine binning TDC if resolution is then lost in imperfections/noise

- **Device mismatch**
  - -> Careful simulation and optimization
  - -> Major impact on design and performance
- **Noise** (power supply)
  - -> **Short delays, fast edges**
  - -> Separate **power domains**
  - -> **Substrate isolation**
  - -> Crosstalk
- **Signal distribution** critical
  - -> RC delay of wires
  - -> balanced distribution of timing critical signals
- **Process-Voltage-Temperature variations**
  - -> LSB auto calibration to compensate for slow VT variations
  - -> Global offset calibration still required



Counter Extension

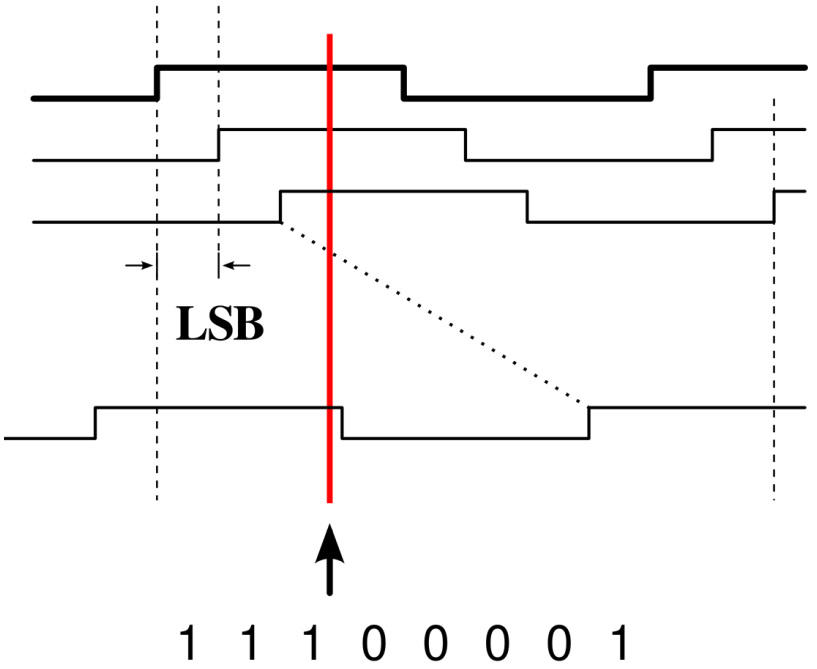


Relate measurement to reference signal

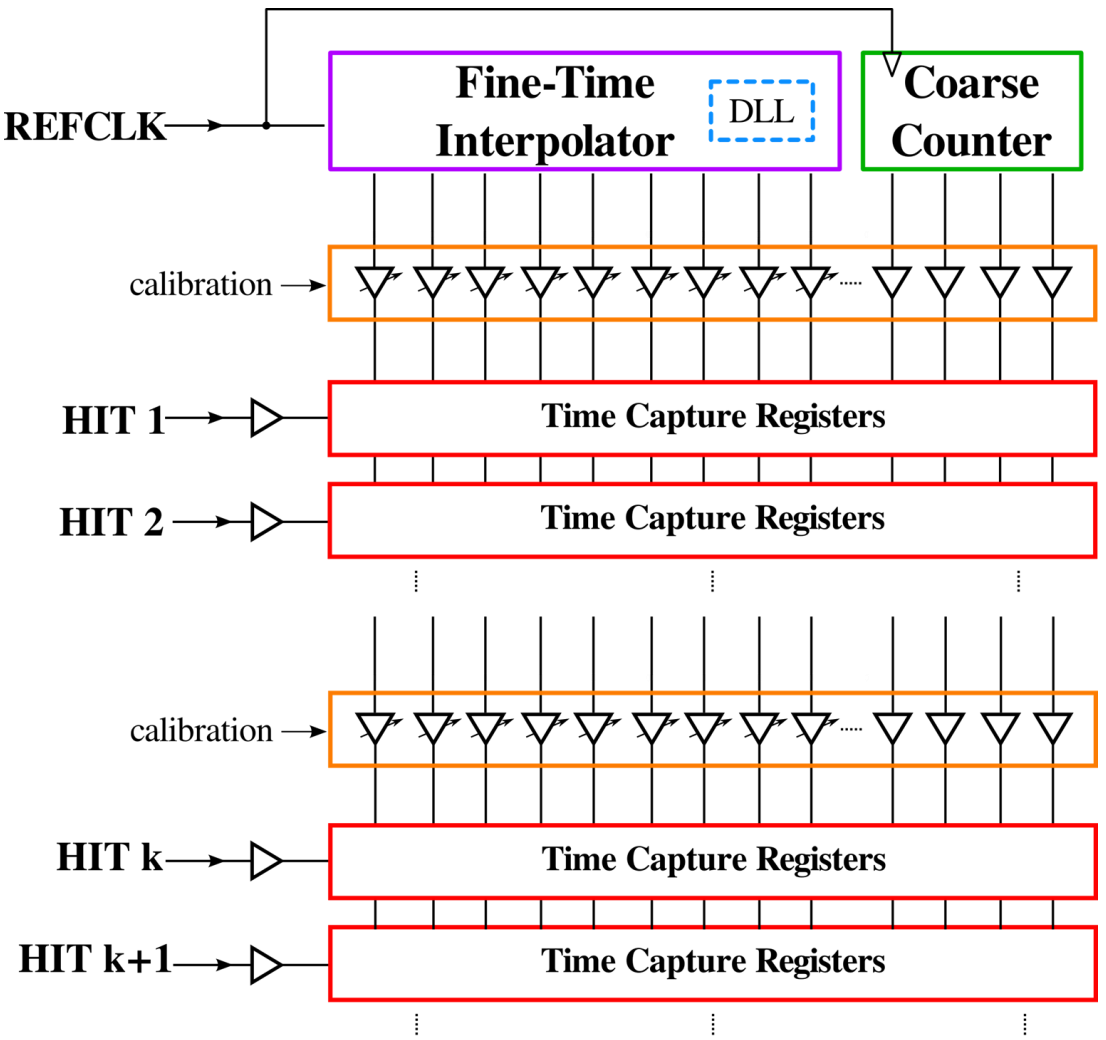
- Delay needs to fit one reference clock cycle
- Delay Locked Loop: DLL

Counter capture/metastability

- Hit is an asynchronous event
- Double counter / gray & additional bit

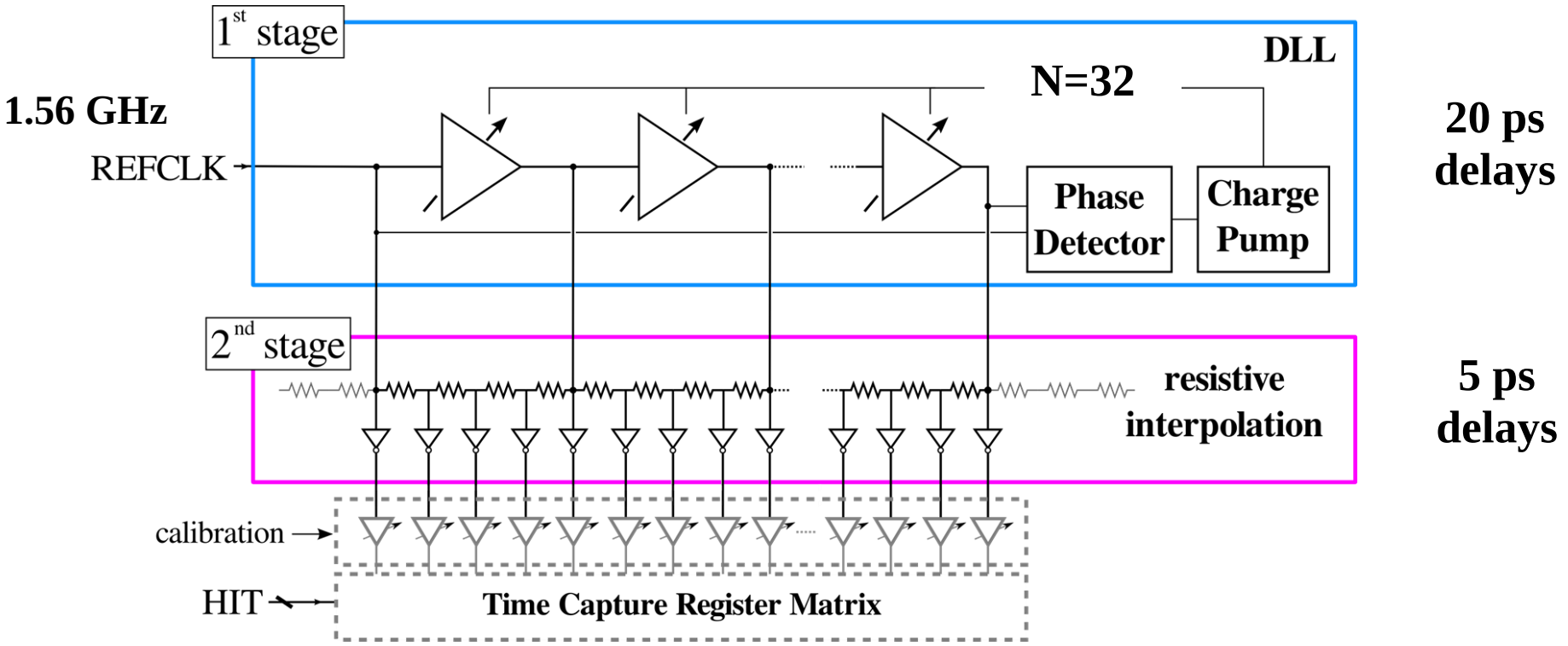


TDC Architecture



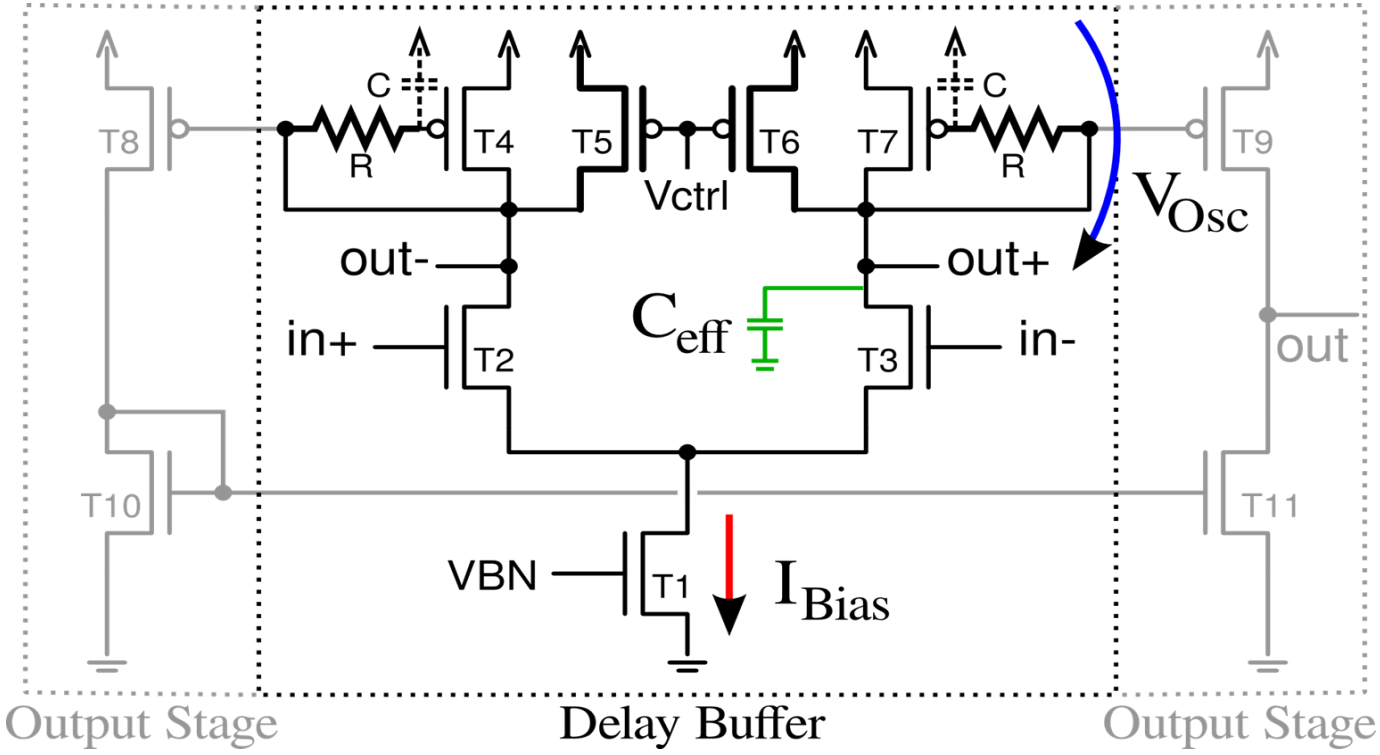
- Central interpolator with counter to extend dynamic range
- Measurements are referenced to common reference to allow to synchronize multiple TDCs
- DLL for PVT auto calibration and power consumption trade-off
- Short propagation delays and fast signal slopes of timing critical signals to reduce jitter
- Calibration applied on a group of channels to reduce circuit overhead and calibration time
- Relatively constant power consumption make it less sensitive to change in hit rate

Fine-Time Interpolator



- **DLL to control LSB size**
  - -> 32 fast delay elements in first stage - 20 ps
  - -> Total delay of DLL 640 ps at 1.56 GHz
- **Resistive Interpolation to achieve sub - gate delay resolutions**
  - -> LSB size of 2nd stage controlled by DLL
  - (Auto adjusts to DLL delay elements)

Voltage Controlled Delay Cell



- **Fully differential cell**
- **Voltage controlled**
- **Single ended output**

Additional zero in signal path

zero location $z = -\frac{1}{RC}$

~15% speed gain

Approximate propagation delay

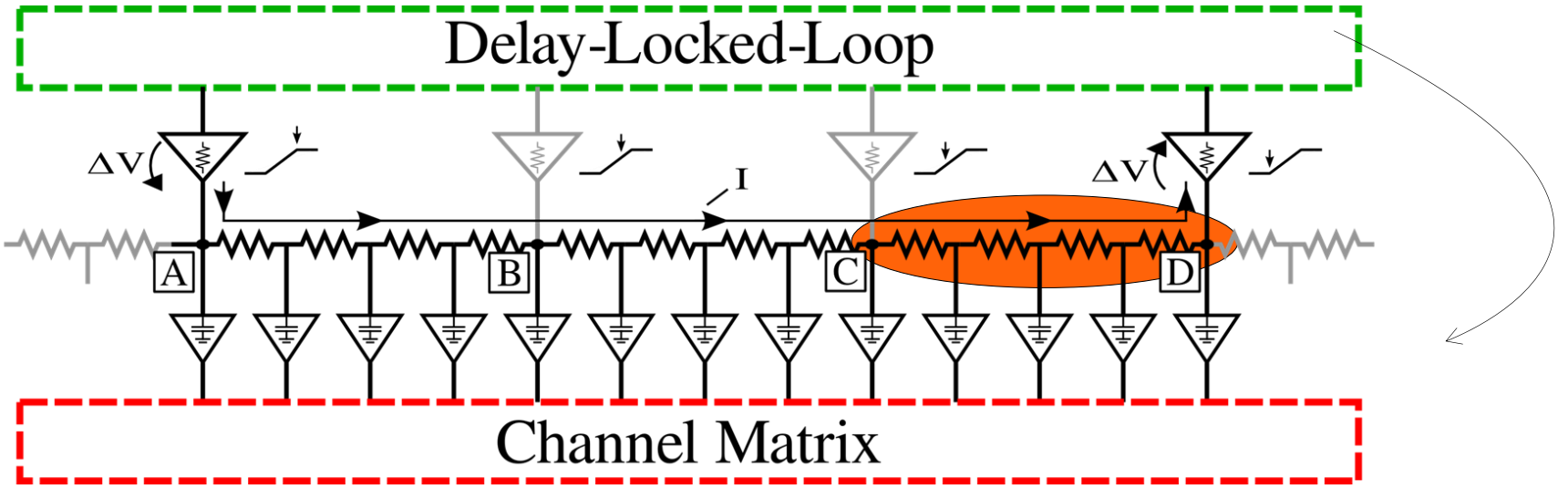
$$\delta \propto \frac{C_{eff} \cdot V_{Osc}}{I_{Bias}}$$

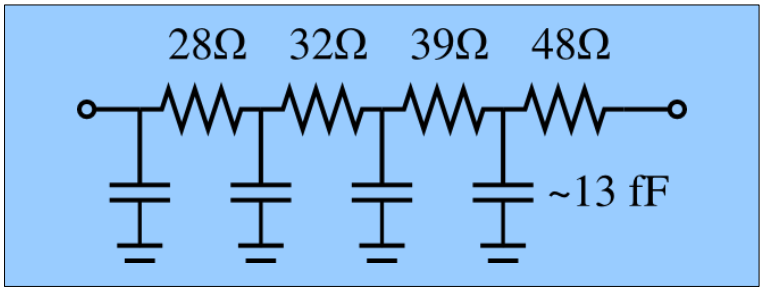
Post layout extracted simulation

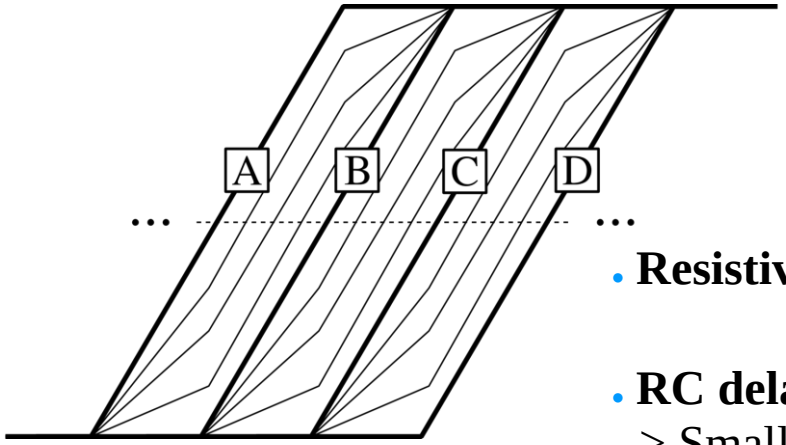
12 ps < 16 ps < 23 ps

@VDD = 1.2 V

Resistive Interpolation

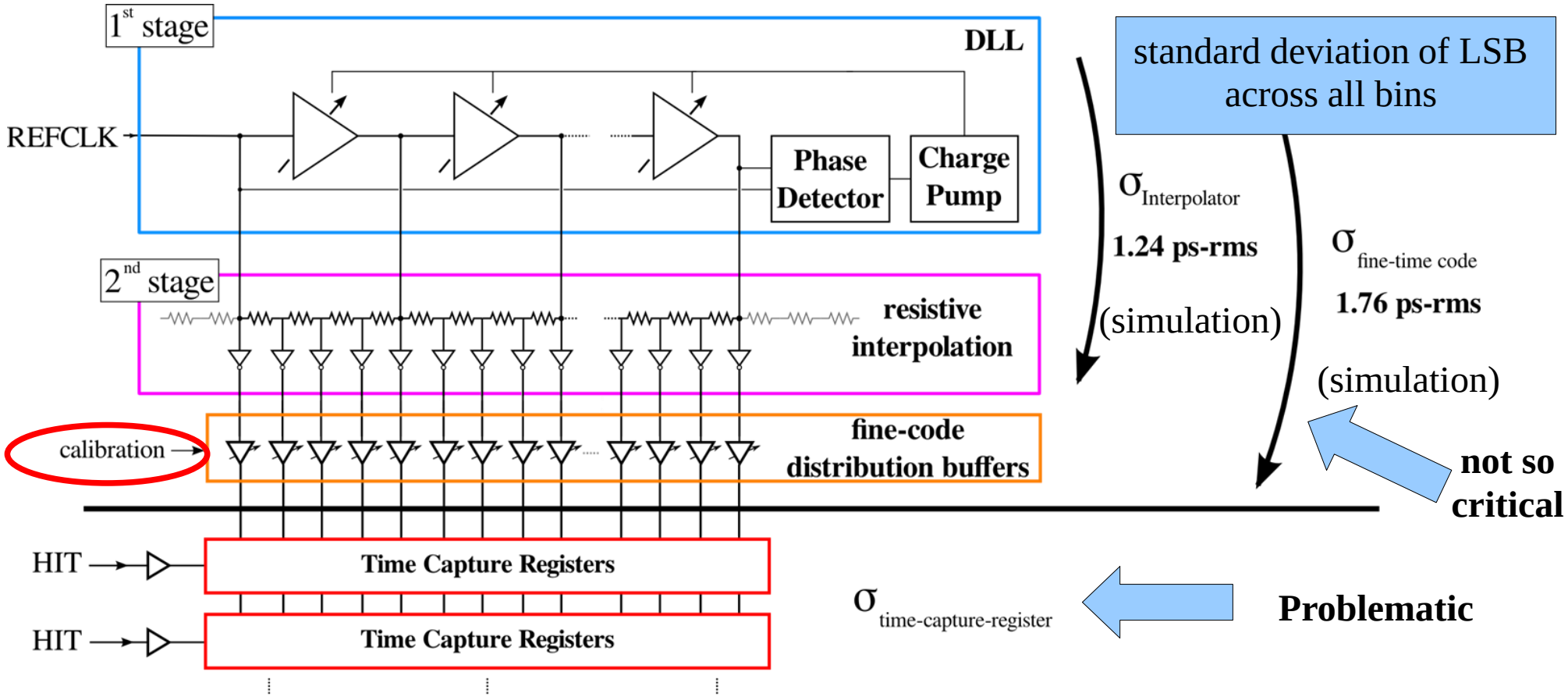






- **Resistive voltage divider**
  -> Signal slopes bigger than delay stabilized by DLL
- **RC delay** (capacitive loading)
  - > Small resistances, small loads
  - > Simulation based optimization of resistor values

Device Mismatch

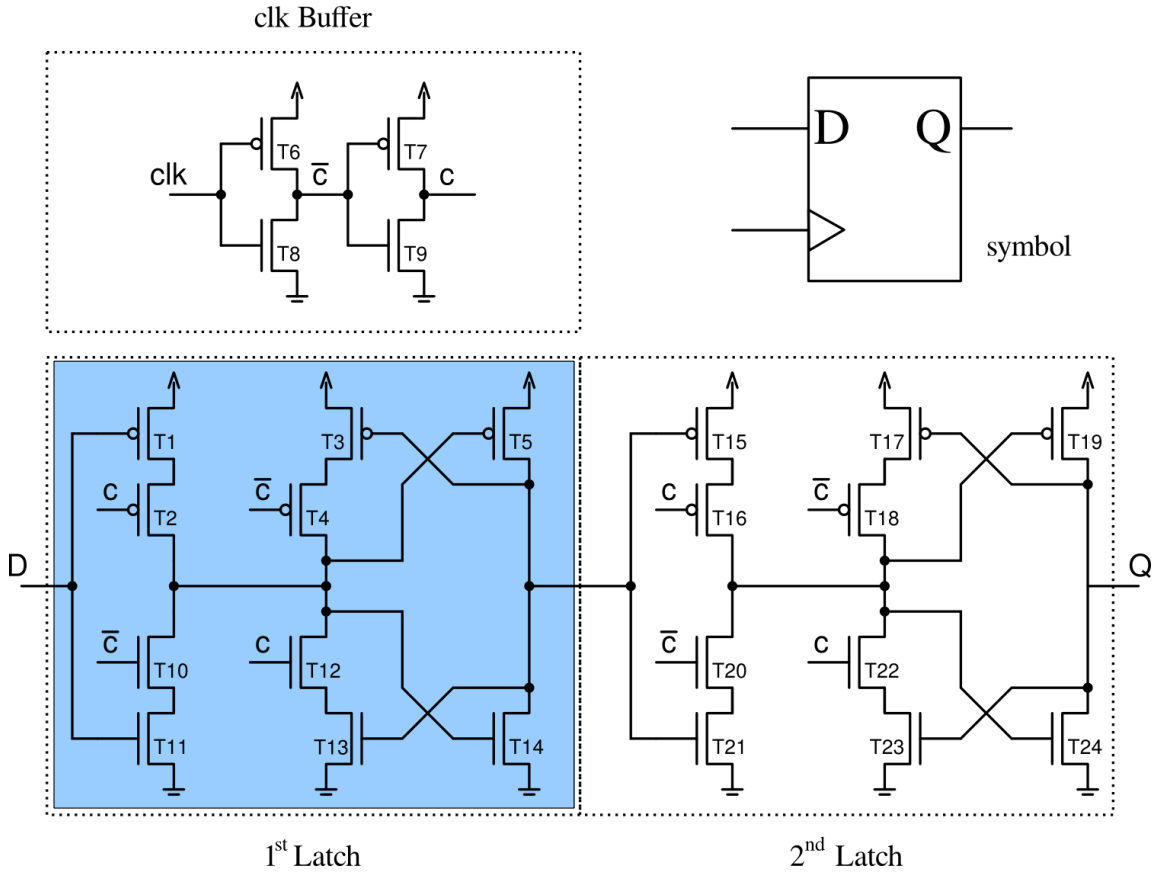


- Calibration can correct for Fine-Time Interpolator and Distribution Buffer mismatch
- Don't want to calibrate each single register
  -> Time capture registers require good matching
  Several implementations designed and implemented
- Circuits carefully optimized for best matching/power compromise with Monte-Carlo simulations

Time Capture Register

No calibration in FF:

Trade off: Power & Resolution



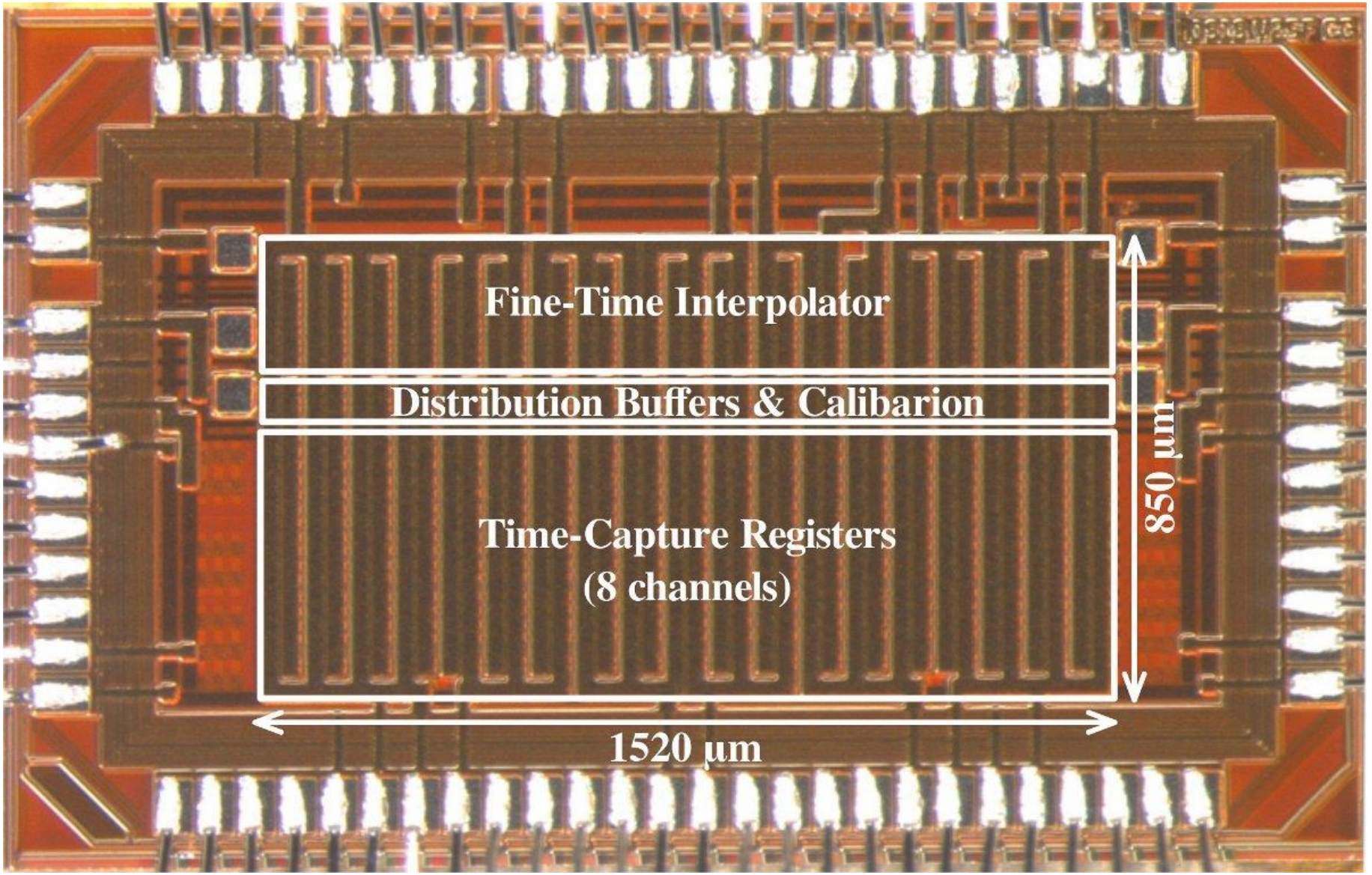
Several implementations evaluated and implemented

Example:
First latch optimized for timing (3x size of standard cell FF)

σ_{TDC} = 1.31 ps-rms

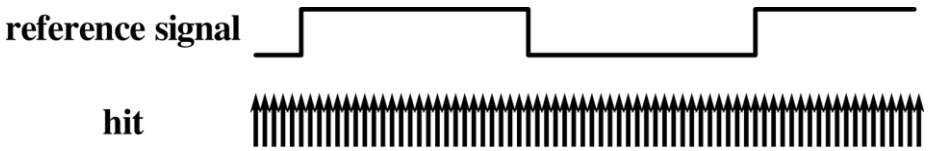
Just about good enough for 5 ps TDC

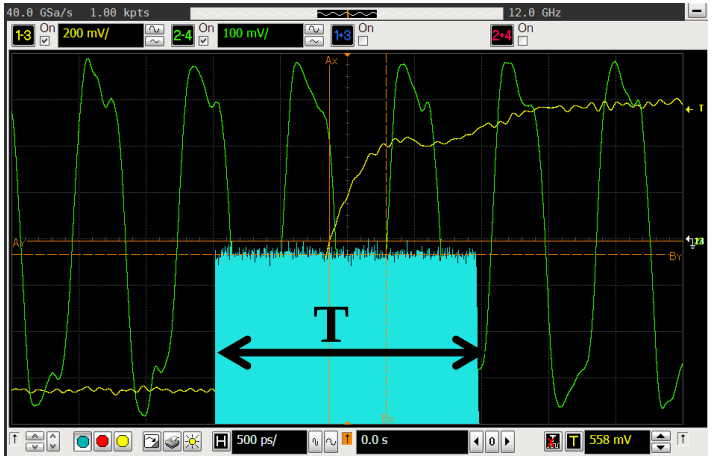
Demonstrator



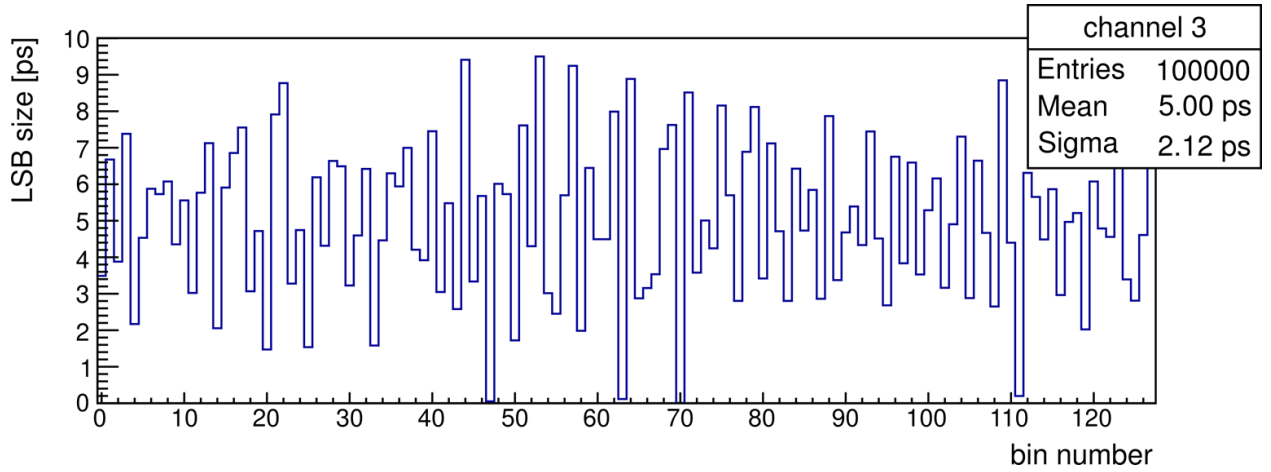
Code Density Test

- Uniformly distributed events across clock cycle
  - Asynchronous clock domains
- Number of collected hits => bin size





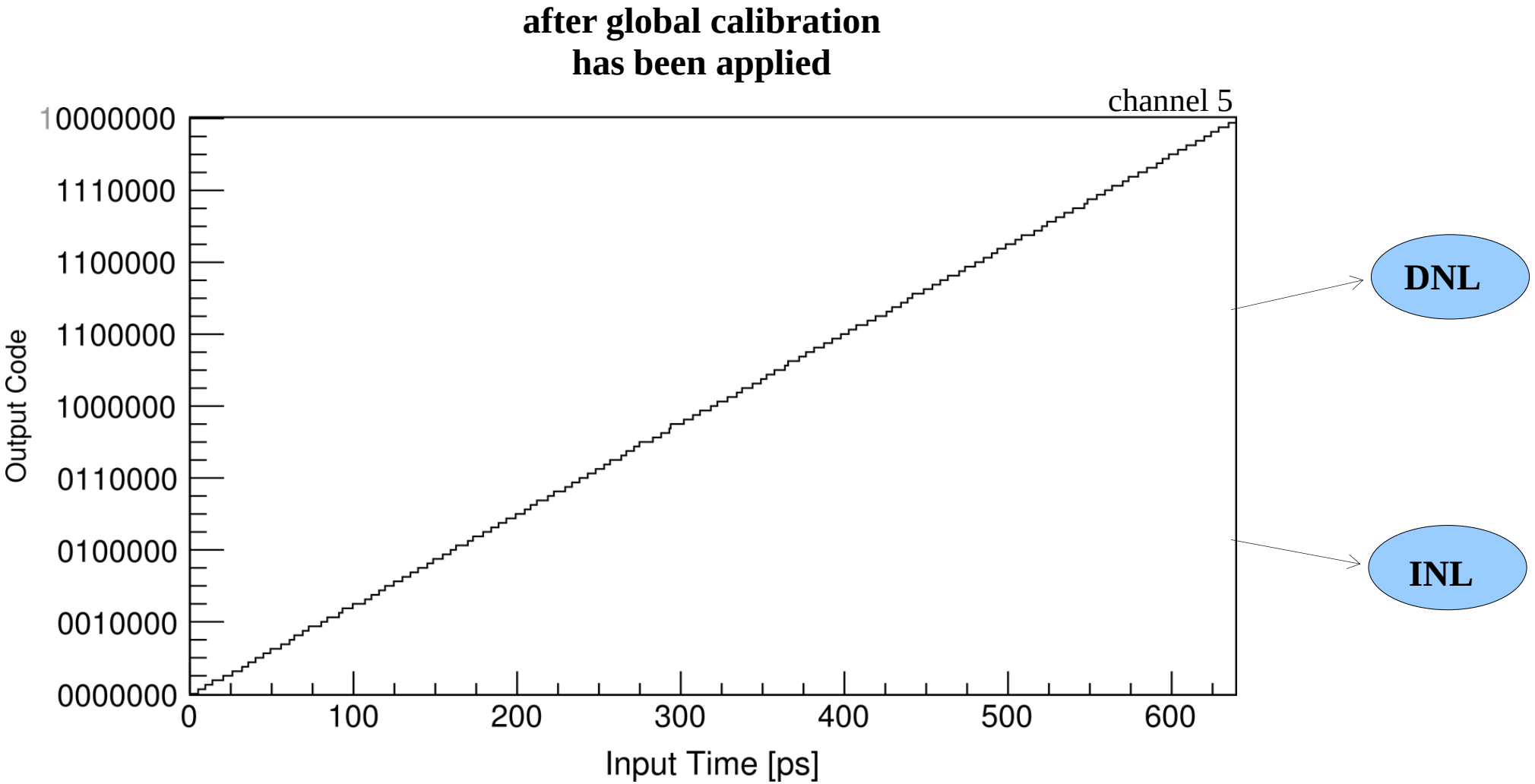
- **Before Global Calibration**



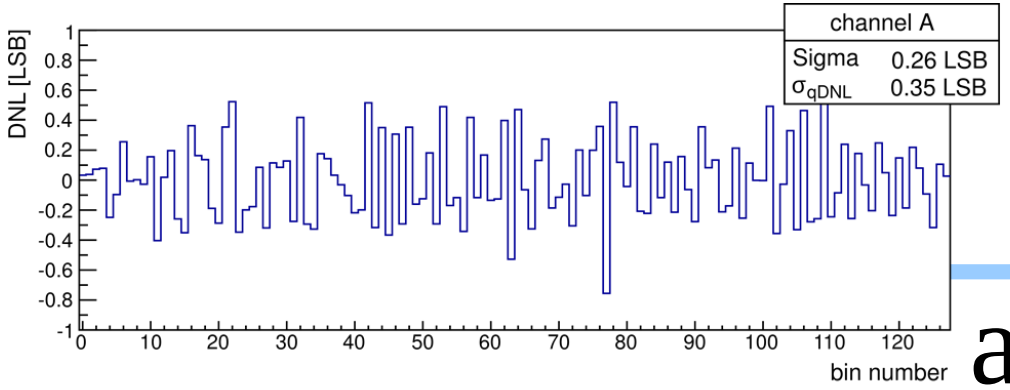
LSB = 5ps

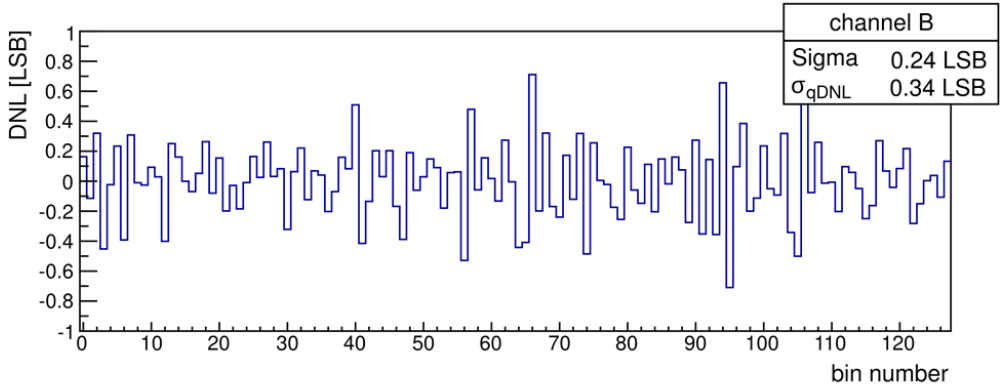
σ_{LSB} = 2.1 ps

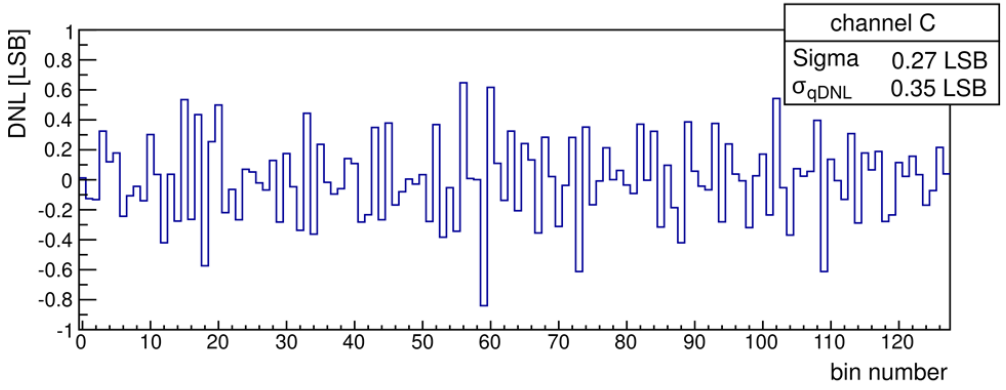
Reconstructed Transfer Function

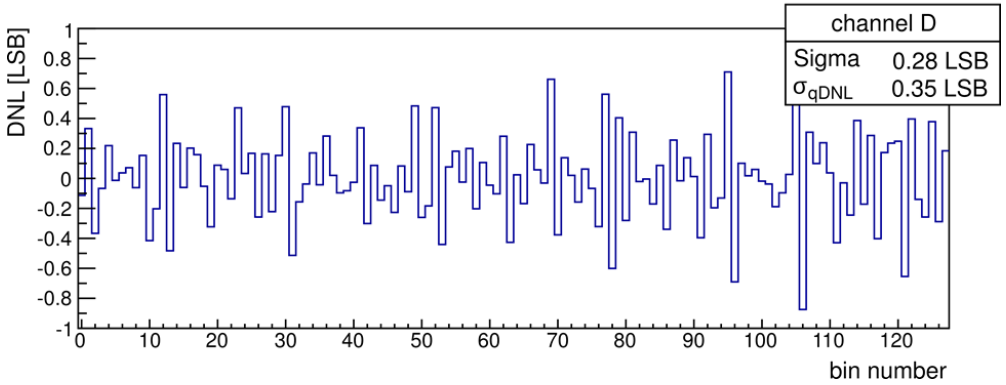


DNL
after global calibration





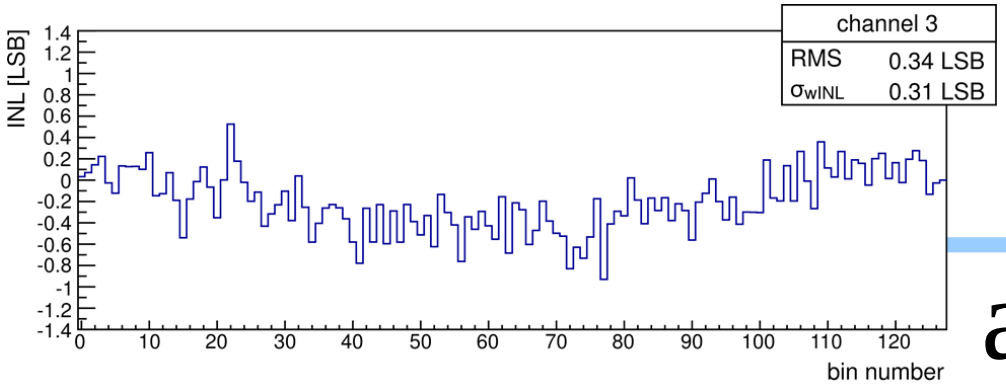


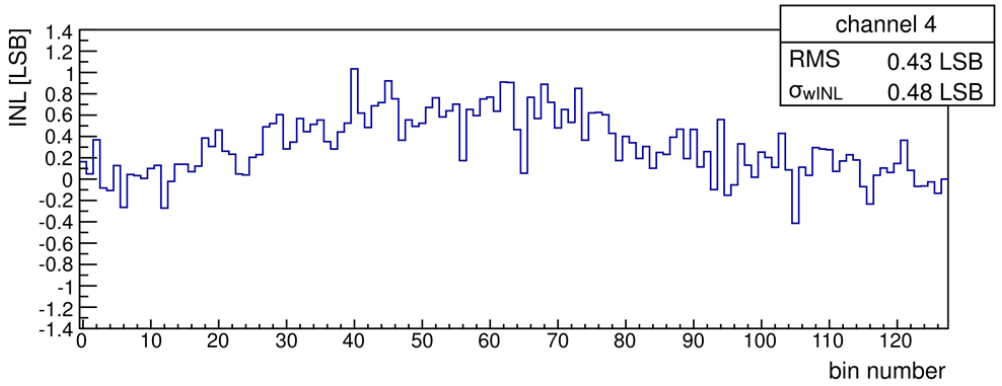


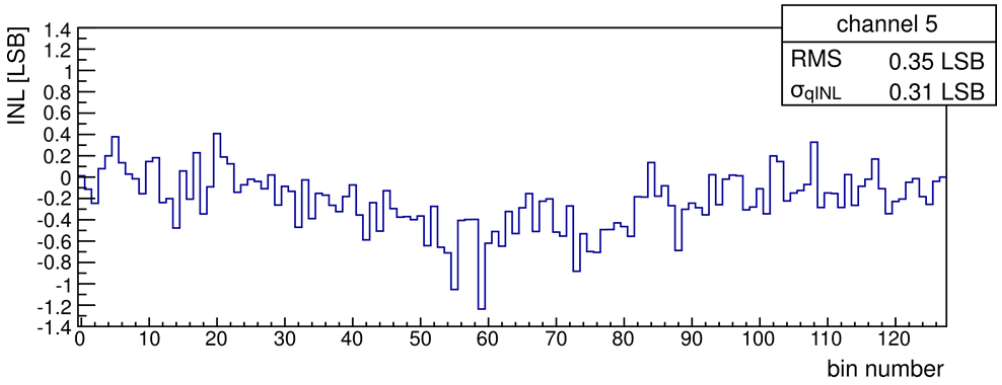
DNL = ± 0.9 LSB

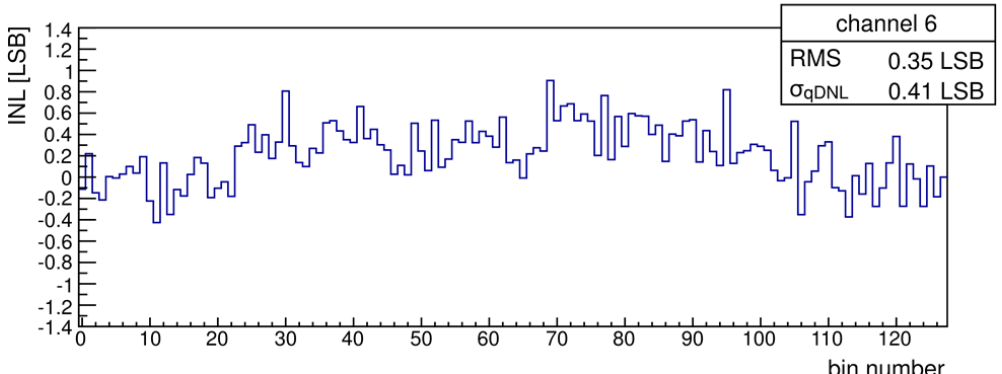
RMS < 0.28 LSB (1.4 ps)

No missing codes









INL after global calibration

INL = ± 1.3 LSB

RMS = < 0.43 LSB (2.2 ps)

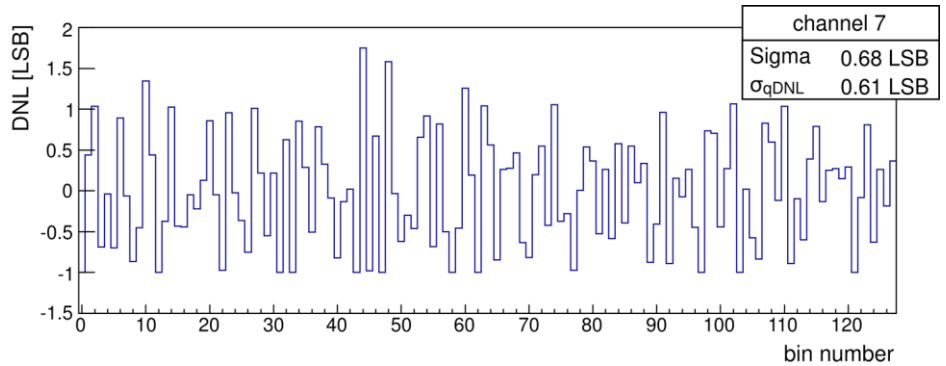
Expected RMS resolution w/ custom FF:
including quantization noise, INL & DNL

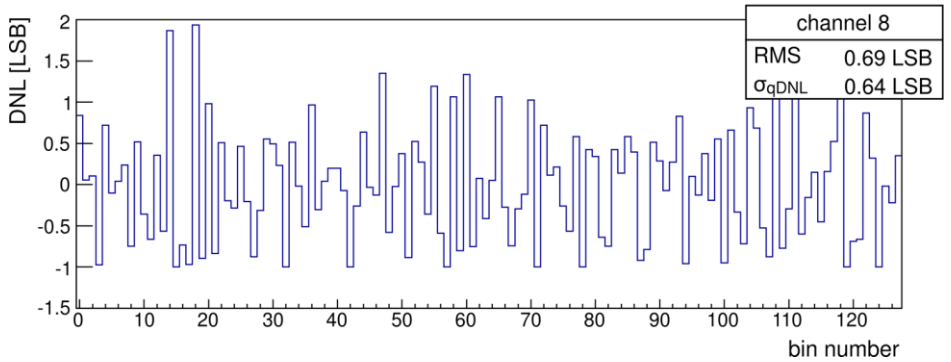
2.3 ps-RMS < $\sigma_{qDNL/wINL}$ < 2.9 ps-RMS

Ideal 5 ps LSB TDC: 1.44 ps-RMS

Standard Cell FF - Weak Matching

Differential-Non-Linearity

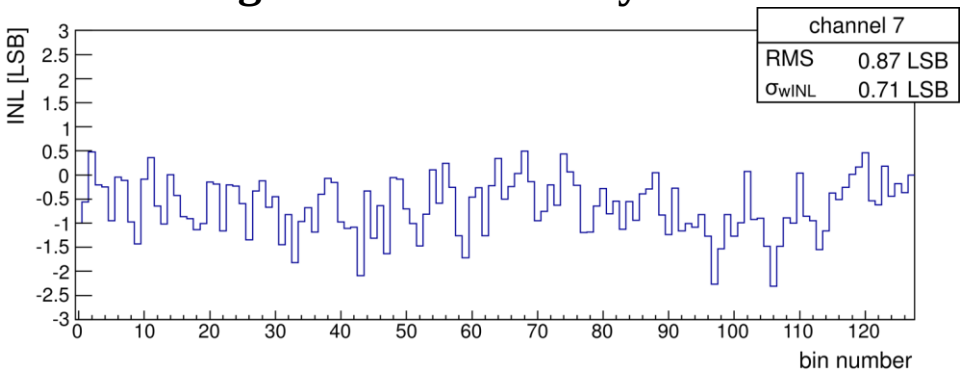


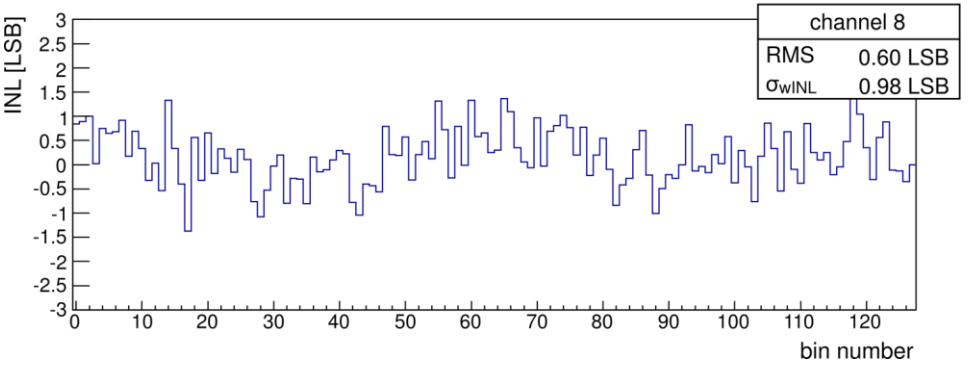


DNL = +2 LSB / -1 LSB

RMS = < 0.69 LSB (3.45 ps-rms)

Integral- Non-Linearity





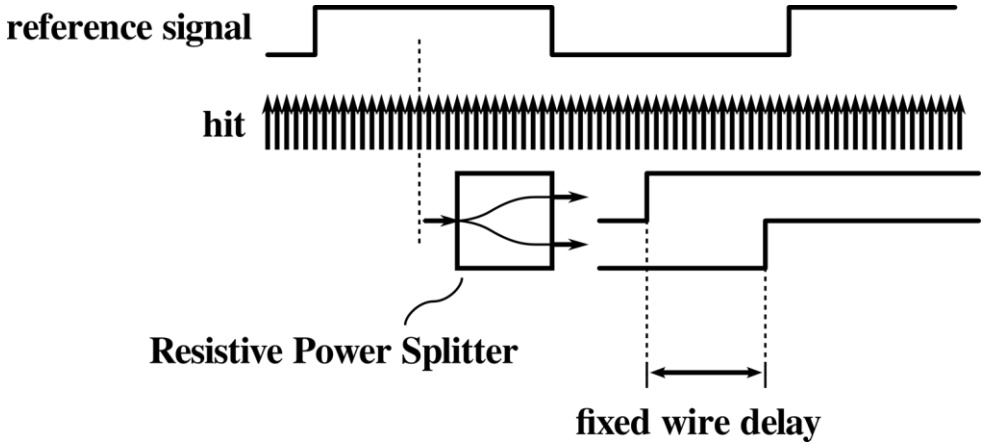
INL = ±2.5 LSB

RMS = < 0.87 LSB (4.35 ps-rms)

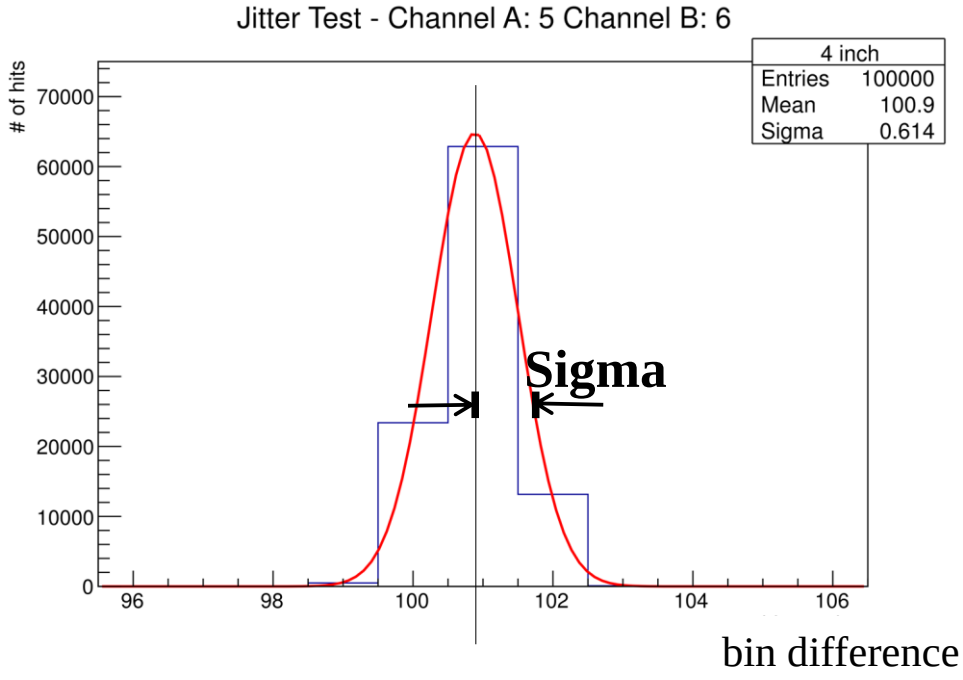
Expected time resolution: < 5.9 ps-RMS (w/ standard cell FF)

Factor ~2 worse (but lower power consumption)

Double Shot Measurement



- Uniformly distributed events across 1 clock cycle
  - asynchronous clock domains
- Send same hit to two distinct channels
- Delay fixed by wire length differences
- Jitter contribution of hit not canceled out

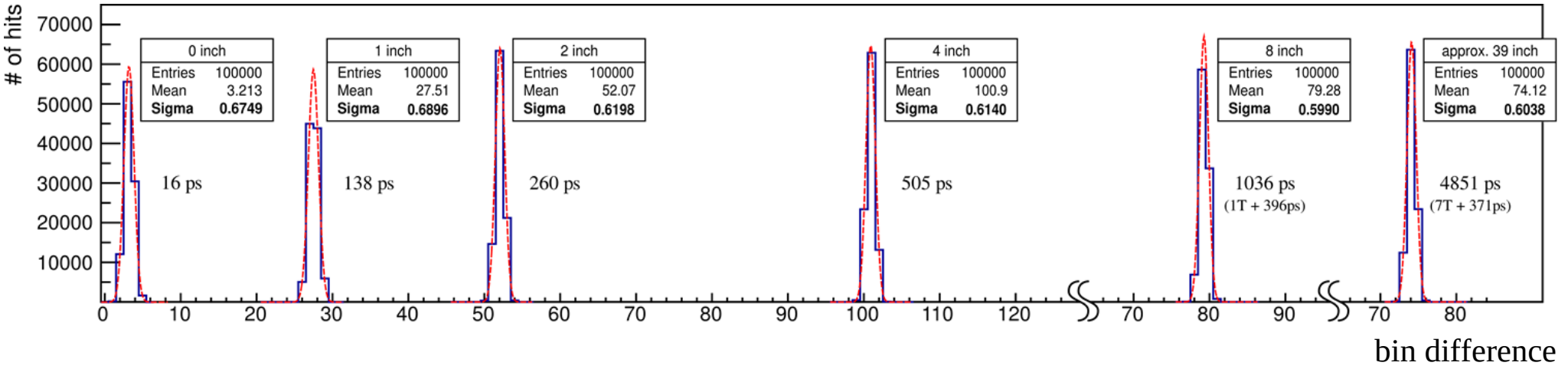


Single Shot Resolution in ps

Sigma*5ps/sqrt(2)

Measured Single Shot Precision

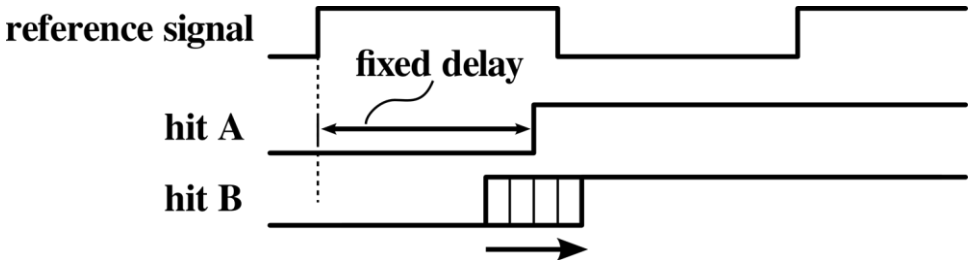
- Three measurement series
  - Both hits arrive within one reference clock cycle
  - Second hit arrives one clock cycle later
  - Second hit arrives multiple clock cycles later (~5ns)



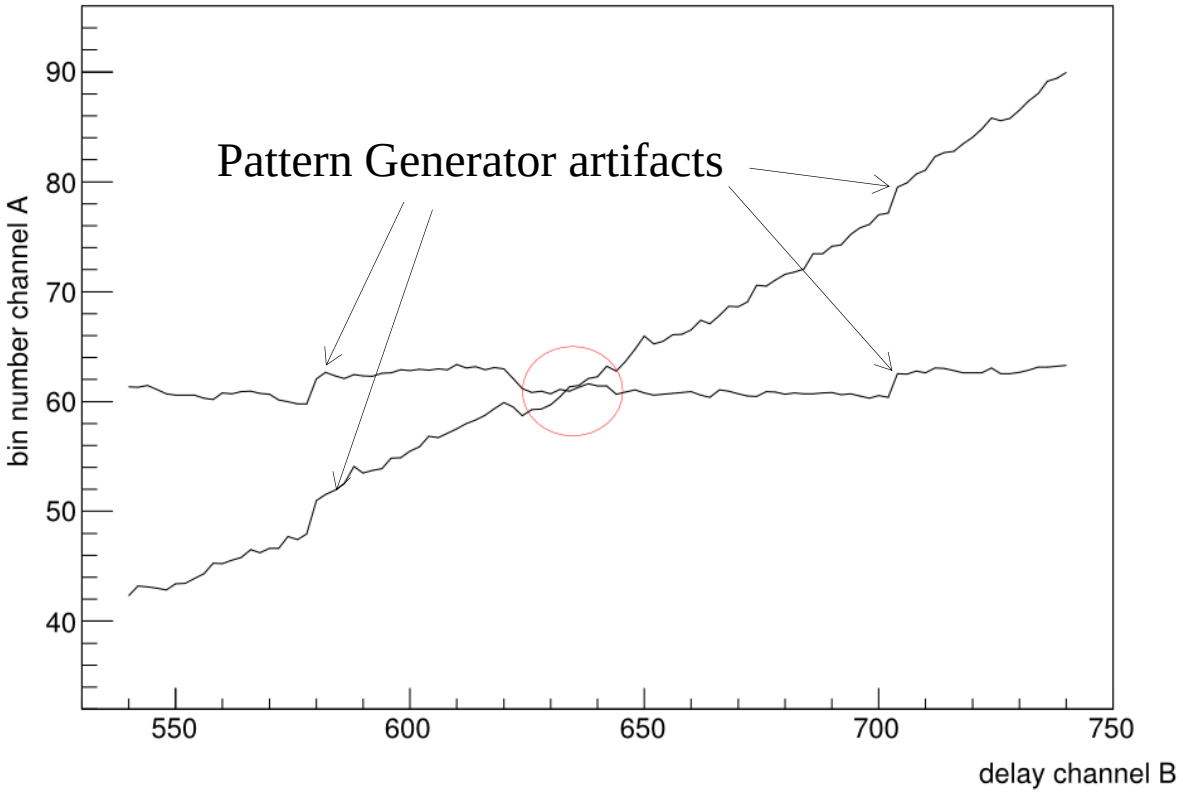
σ_{TDC} < 2.44 ps-RMS

- Limited by non-linearities of TDC
  - -> Very silent setup
  - -> Robust architecture

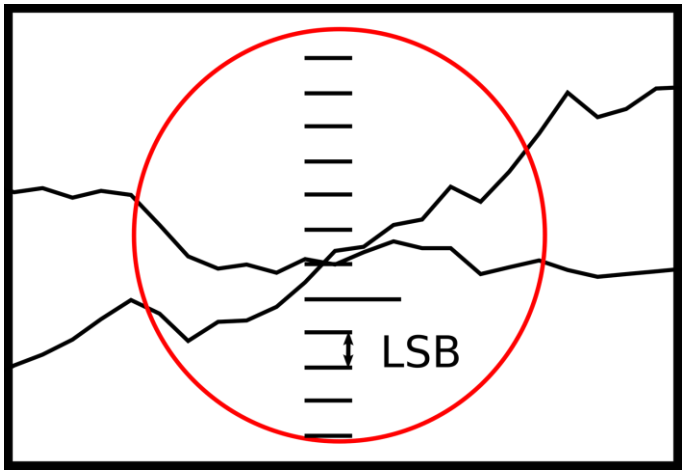
Inter Channel Crosstalk



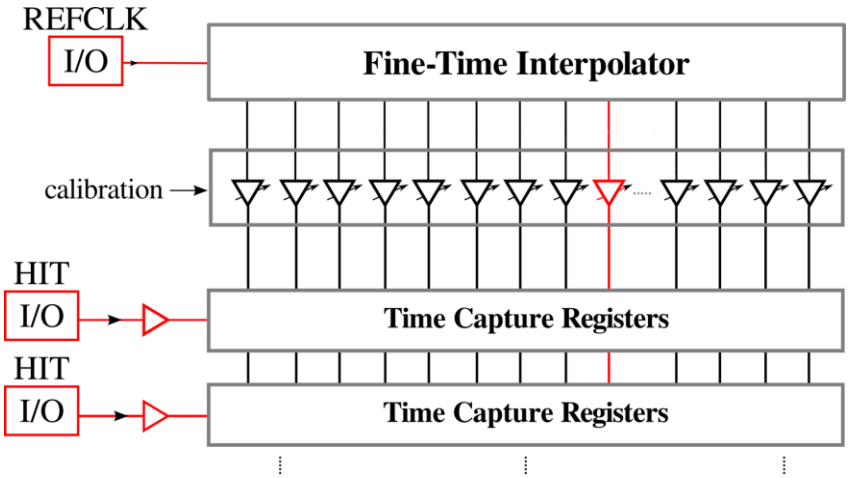
- Sweep hit B over hit A
- Monitor change in delay of hit A



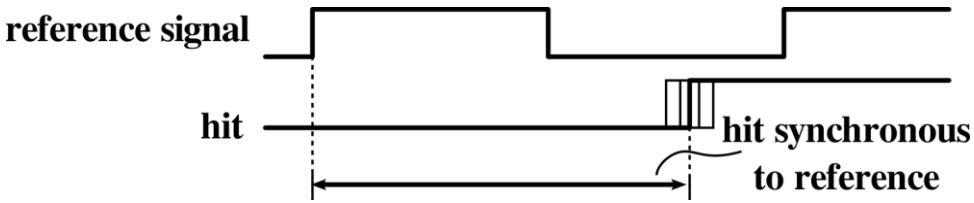
Smaller than ± 1 LSB

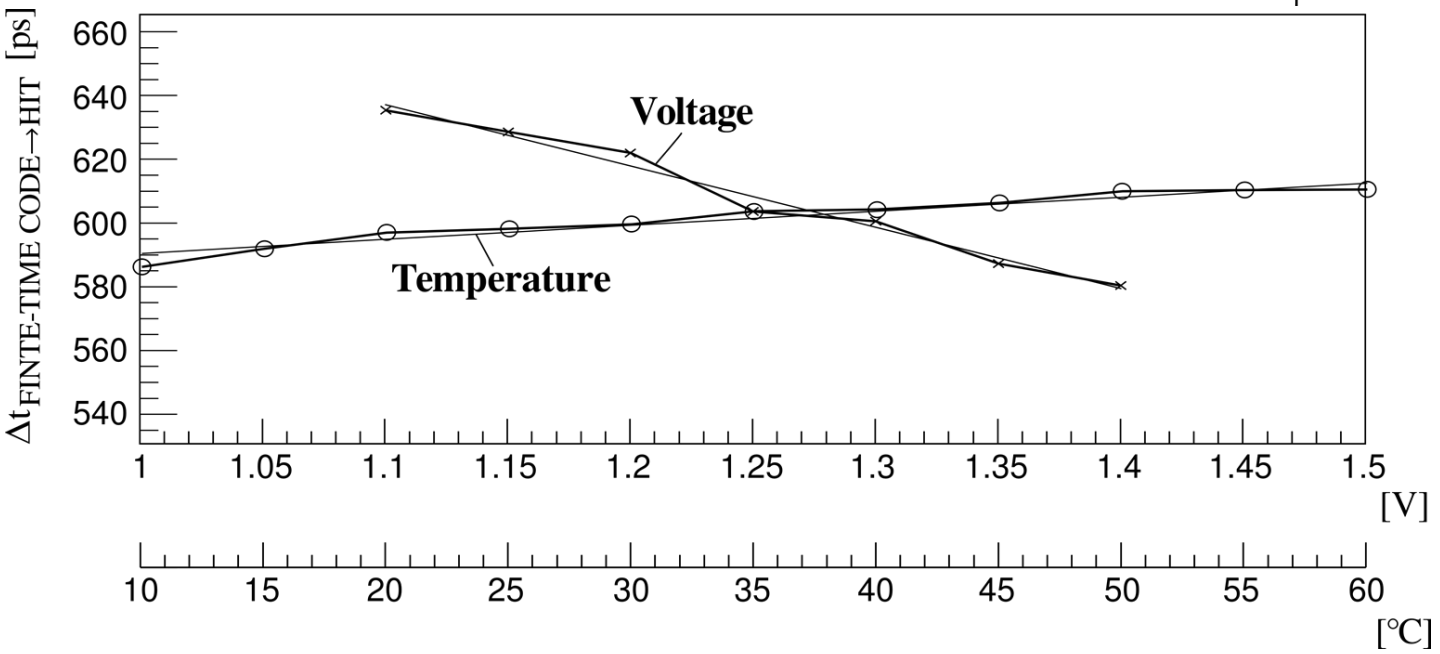


PVT variations



- External reference, DLL auto adjusts
- Delay path changes: **Offset shift**
  Input buffers, drivers, gates, etc.



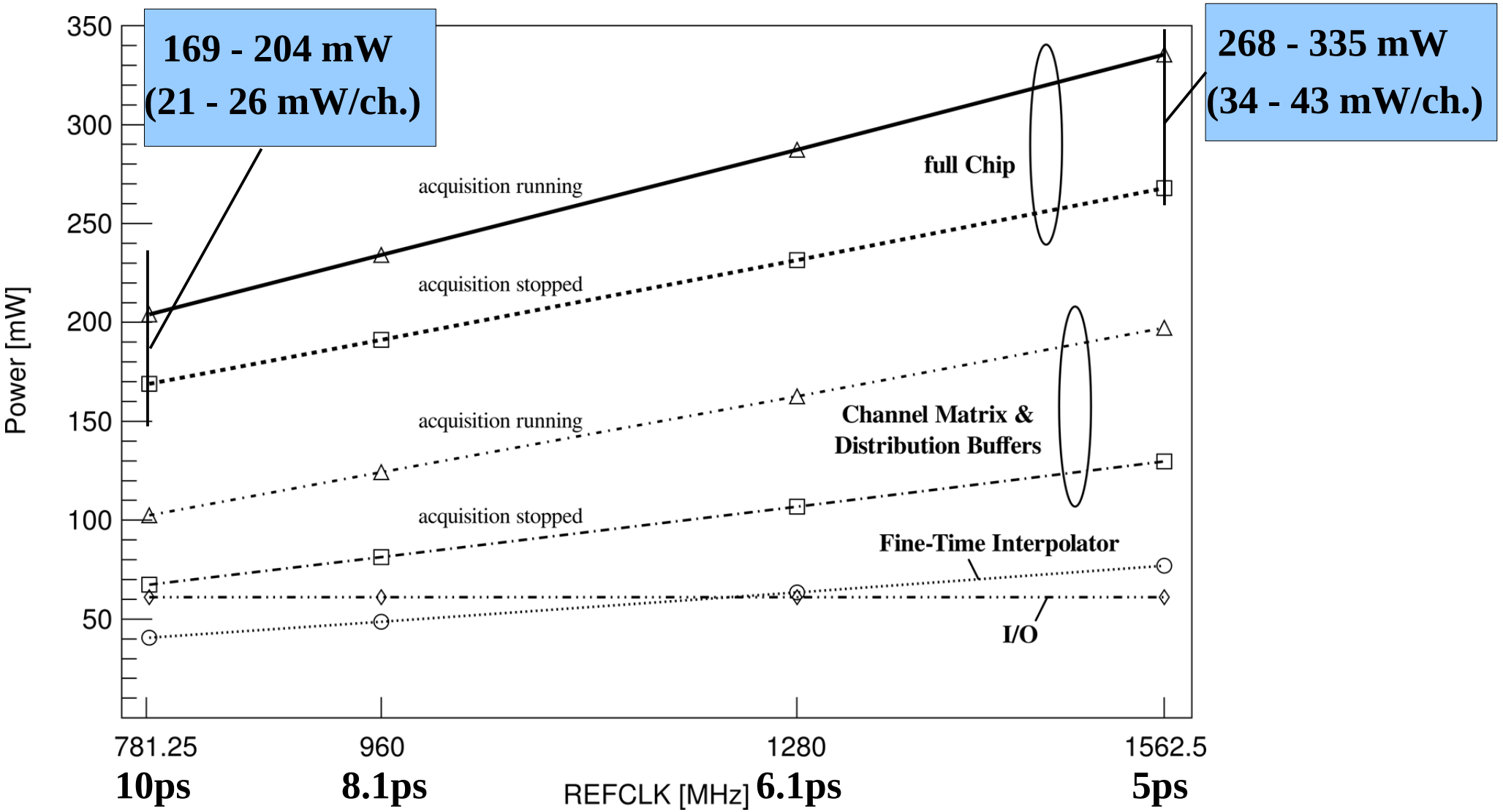


-0.2 ps / mV
0.4 ps / deg

Can if required be improved by further delay matching between reference path and hit path

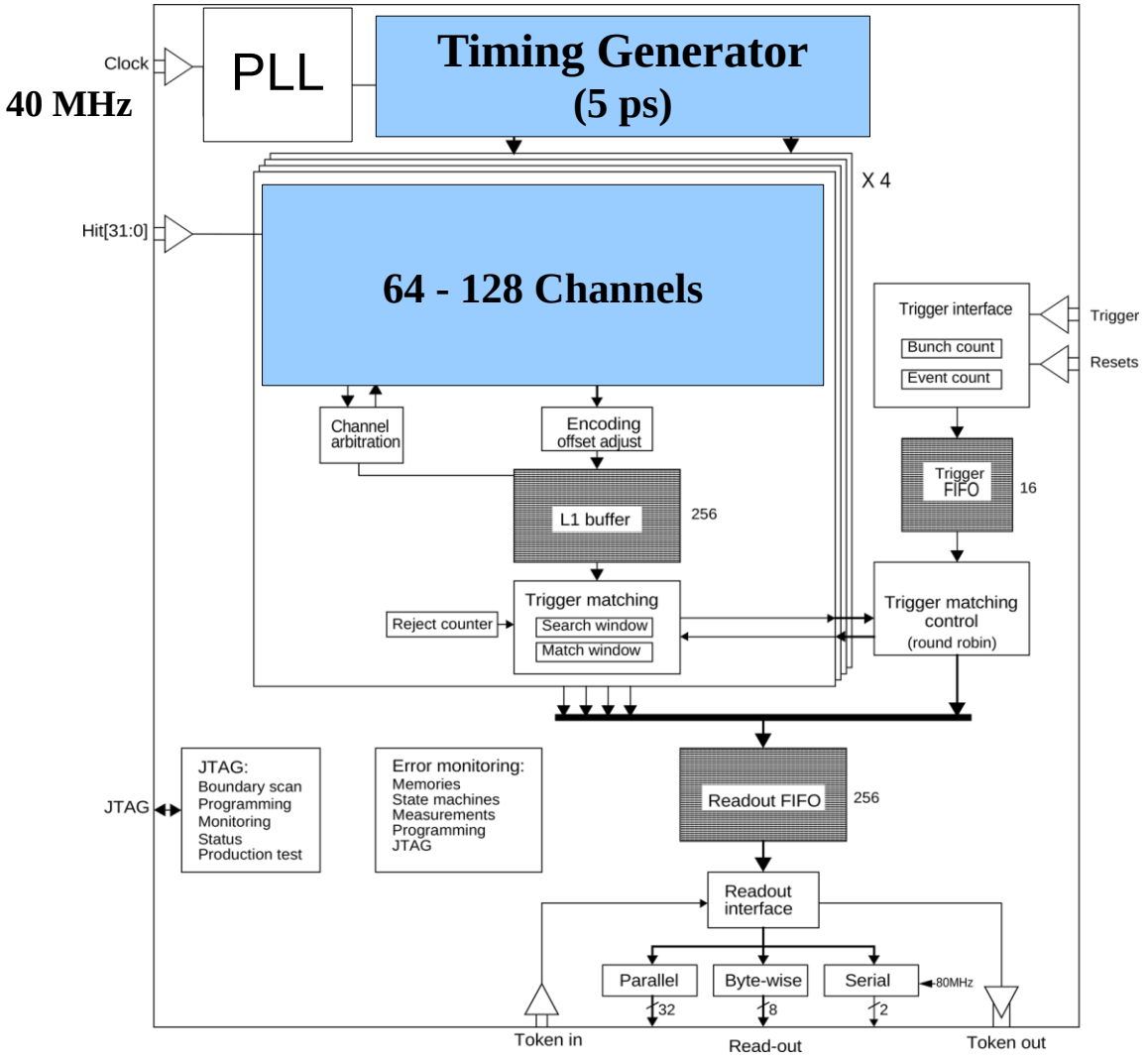
Power consumption

8 channels



Full TDC ASIC to be made

TDC Architecture:



Demonstrator ASIC

- < 3 ps-RMS resolution
- < 50 mW/channel
- Missing: PLL, Counter, Digital logic

Full TDC

- Based on HPTDC
- 64 - 128 channels per ASIC
- 40 MHz input clock
- < 5 ps-RMS timing precision (Power consumption optimization)
- Radiation tolerant
- Flexible readout architecture

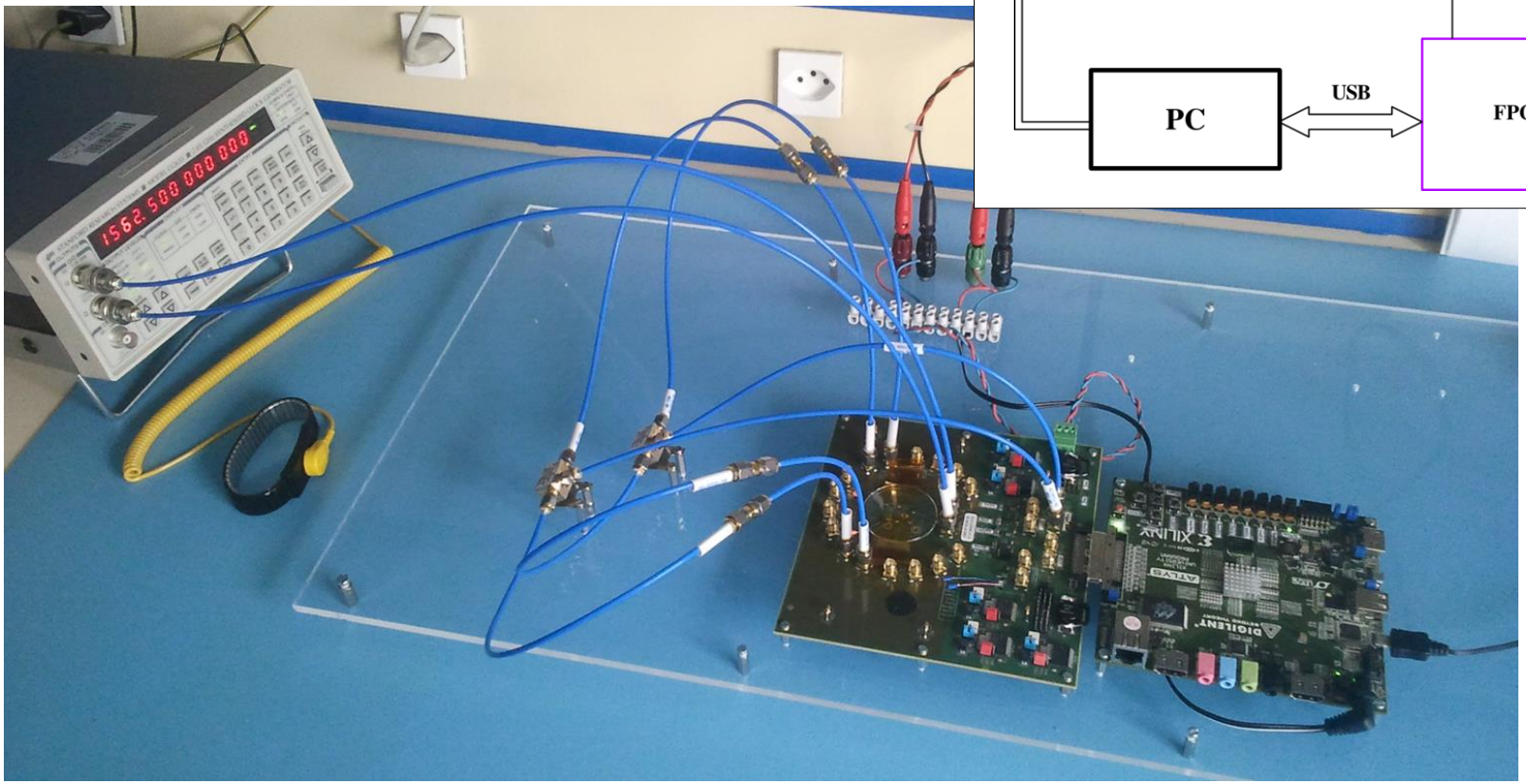
Conclusion

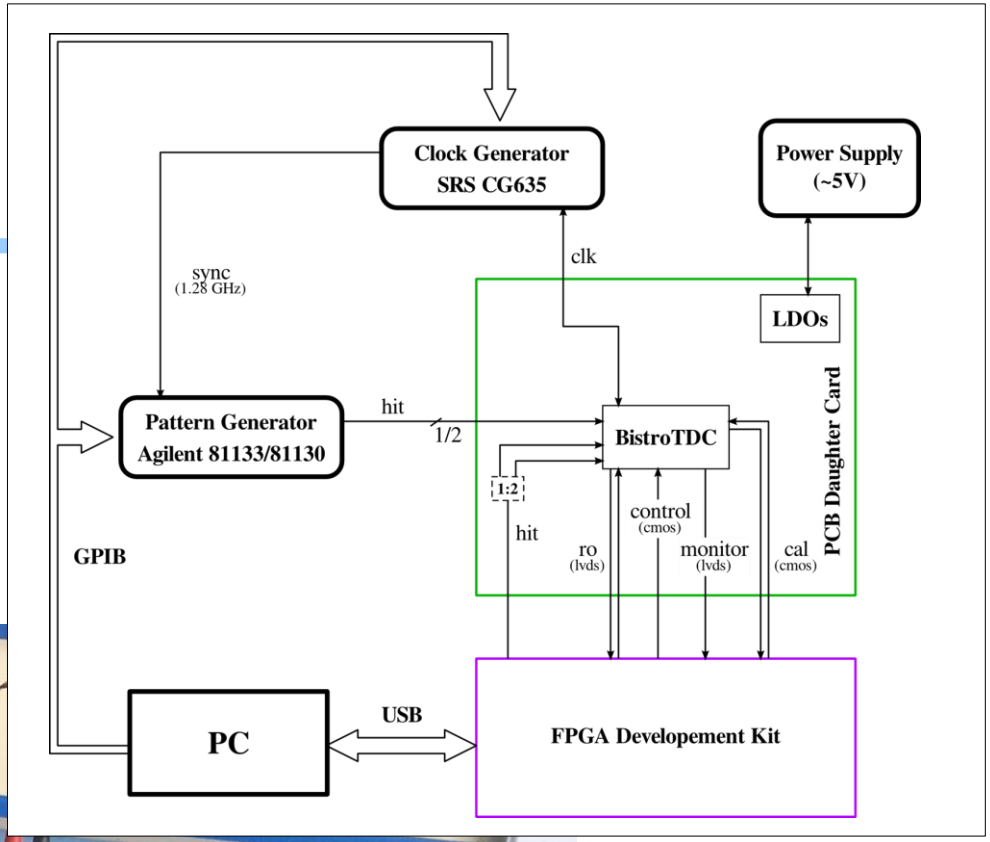
- Demonstrator TDC has been designed, prototyped and successfully tested.
- 3ps RMS time resolution has been demonstrated
- Device mismatch considerably affects performance
  -> Trade off: Power, Resolution, Calibration
- Macro suitable for high resolution general purpose TDC

BACKUP

Test Setup

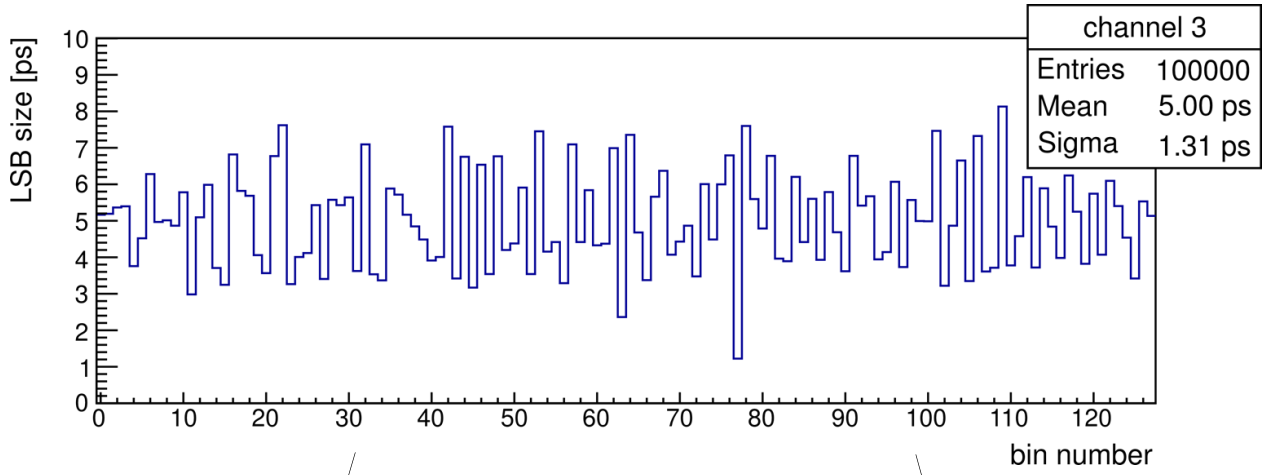
1562.5 MHz = 5 ps **@VDD = 1.3 V**





Interpolator Linearity

- **After Global Calibration**



LSB = 5ps

before calibration:

σ_{LSB} = 2.1 ps

after calibration:

σ_{LSB} = 1.3 ps

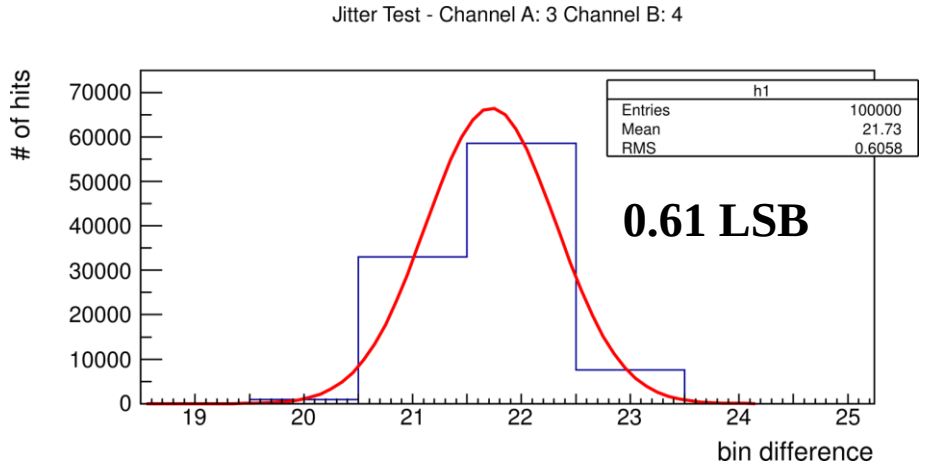
no missing codes

Differential-Non-Linearity

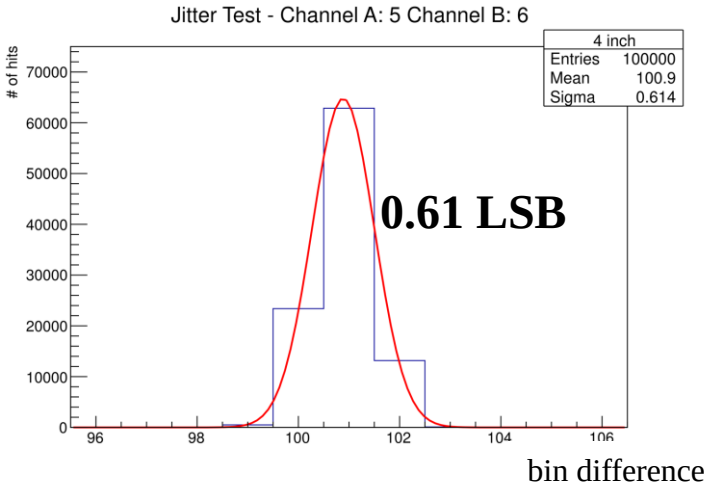
Integral- Non-Linearity

I/O Buffer Influence

- **E-Link ~ 1mA**

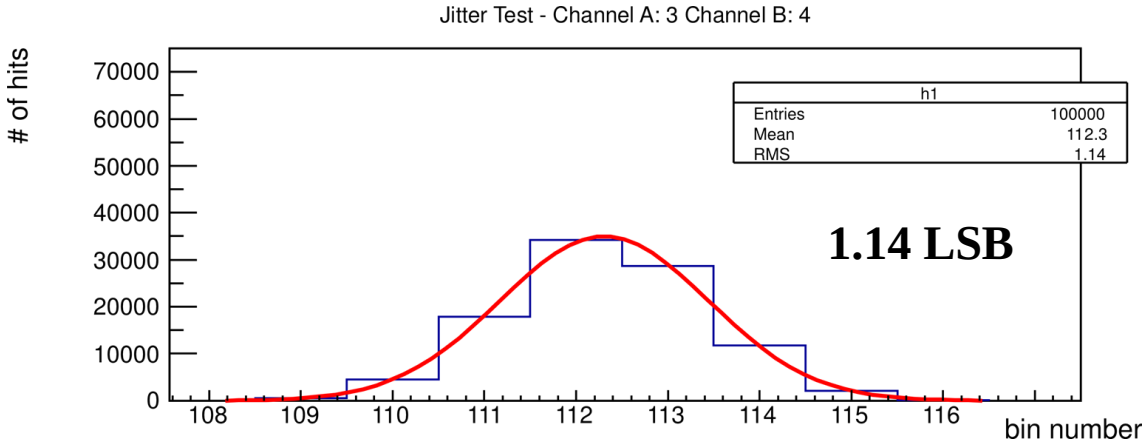


- **GBT RX ~ 10mA**

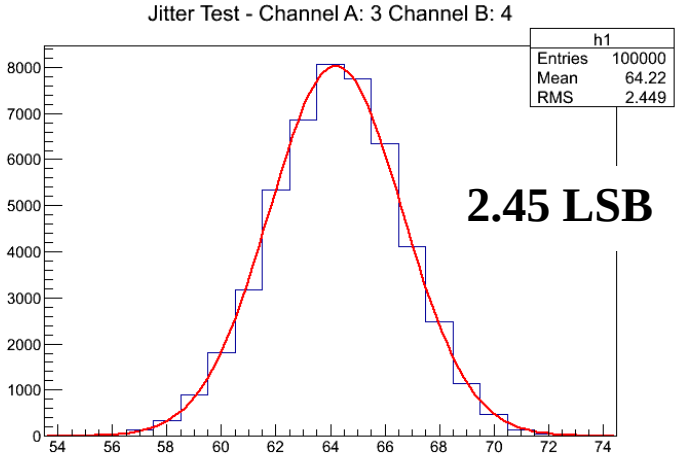


- attention on Vcm level and VDD

VDD = 1.35 V, Vcm = 1.2 V



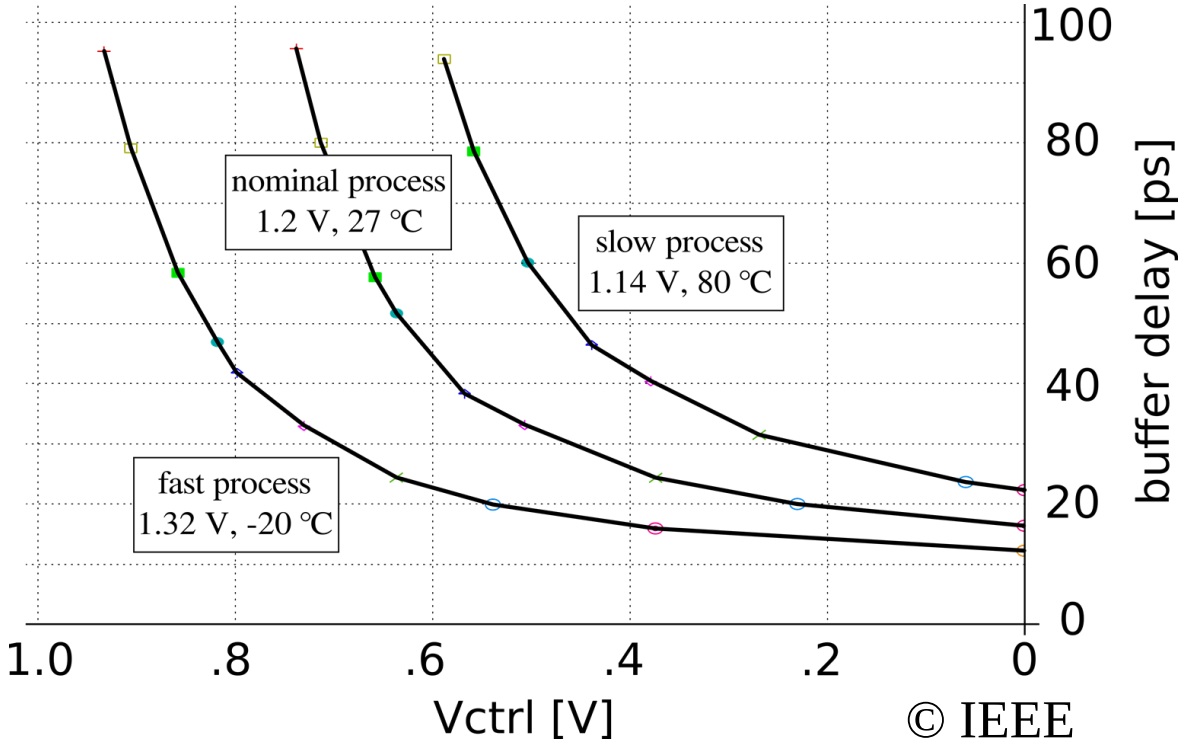
VDD = 1.2 V, Vcm = 1.2 V



Reference Clock Frequency

5 ps = 1562.5 MHz

- How fast the delay line can go depends on process variations and operating conditions



Post Layout Extracted

LSB: **12/4 ps - 23/4 ps**

REFCLK: **1.38 - 2.60 GHz**

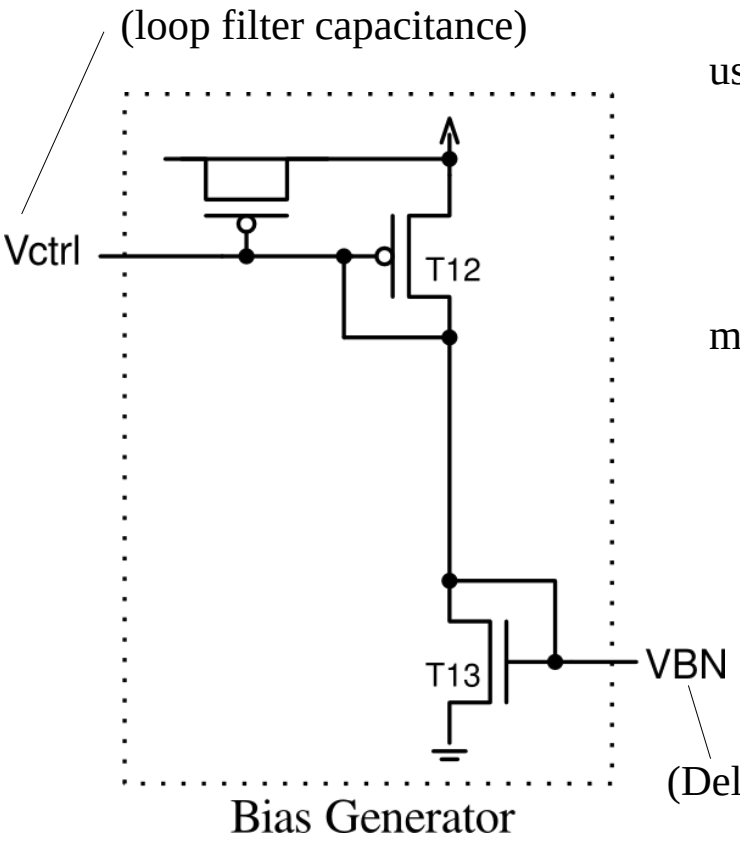
measured max. freq @ 1.2 V

REFCLK: **1.48 GHz**
-> 21/4 ps

little bit on the slow side

VDD = 1.3 V

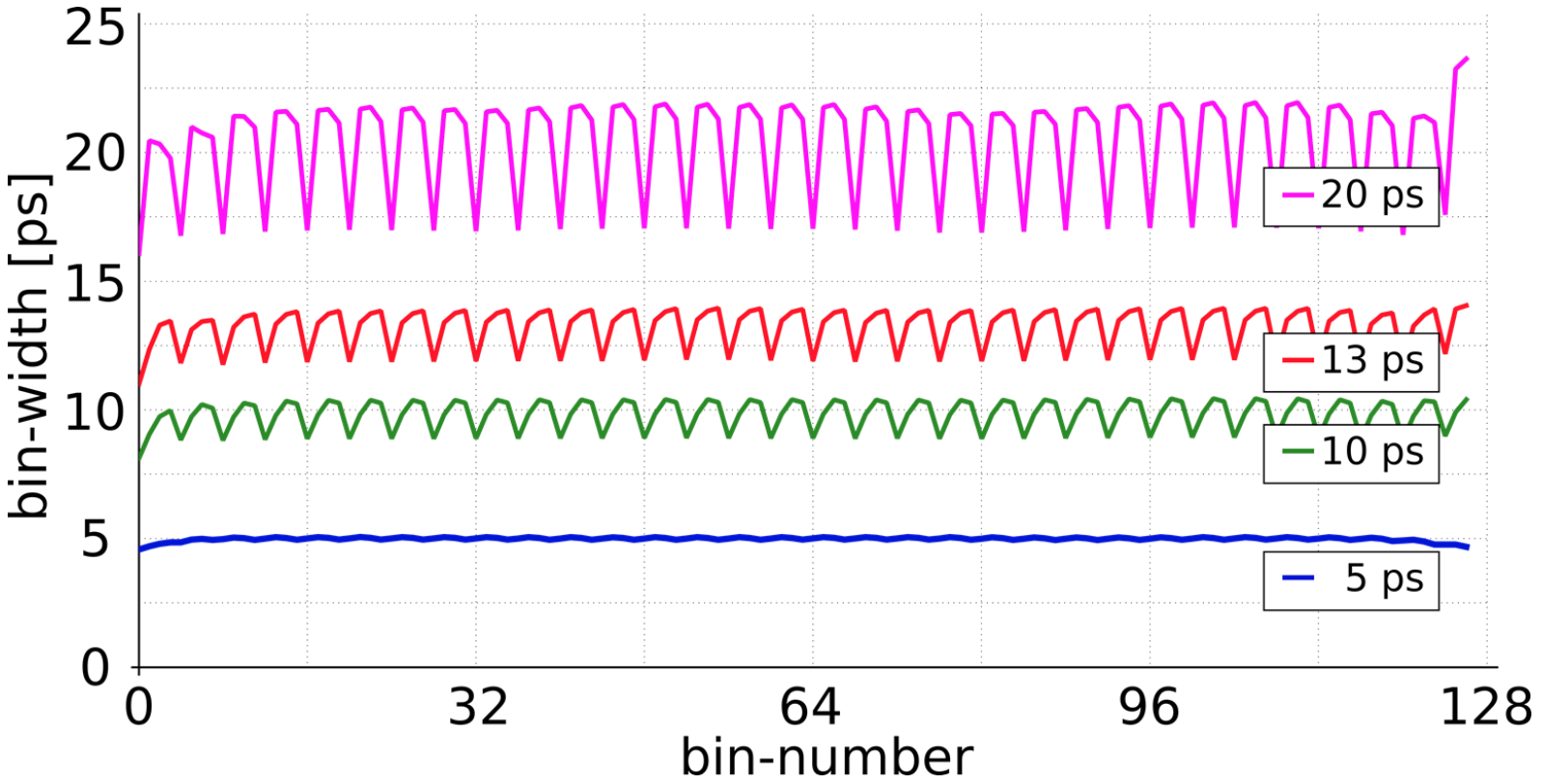
Delay Buffer Biasing



use simple bias to make use of big loop filter capacitance
-> most stable voltage in chip

main control on PMOS:
-> no strong arguments to control PMOS
instead of NMOS but ...
-> big intrinsic capacitive nodes on both controls
-> smaller gain at slower operation

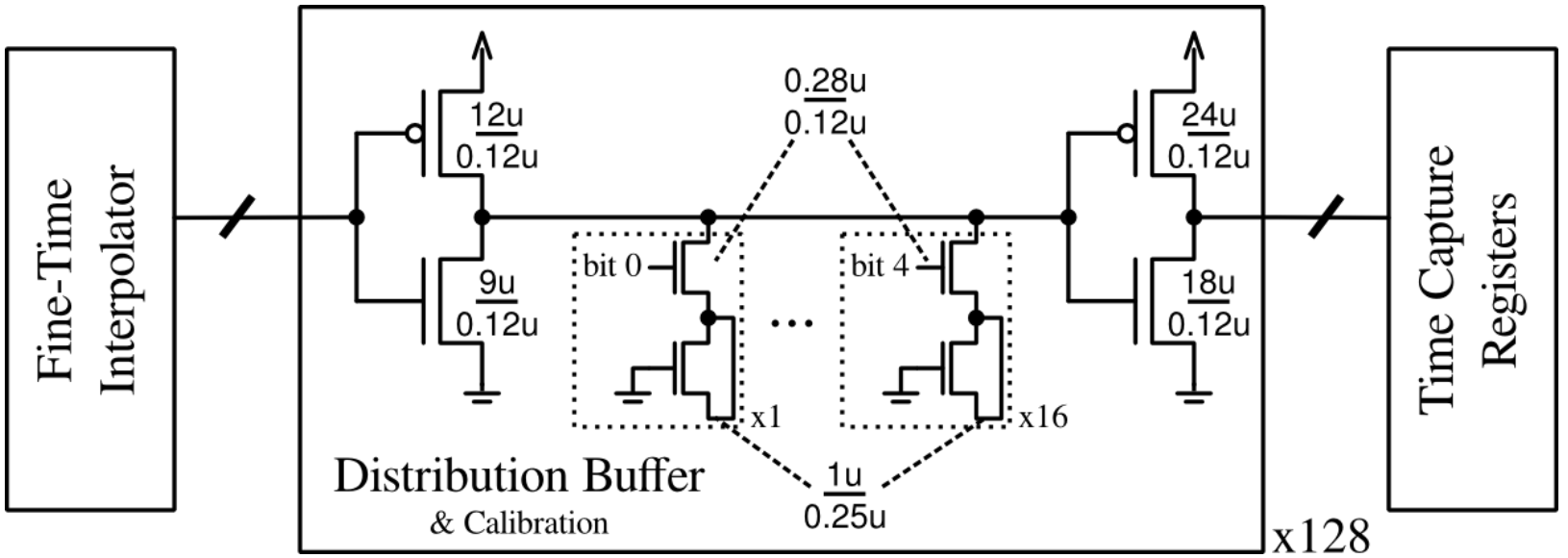
Simulated Bin-Widths



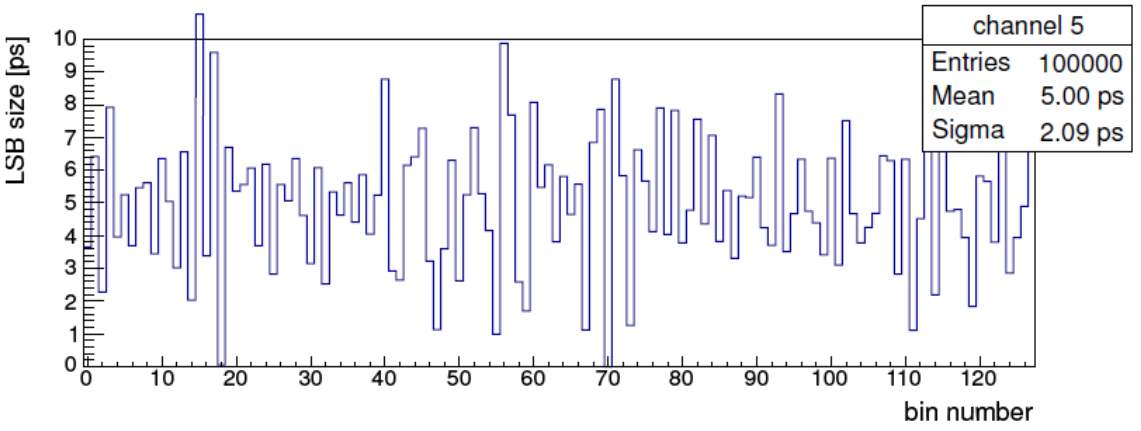
rms = 2.2 ps

rms = 0.1 ps

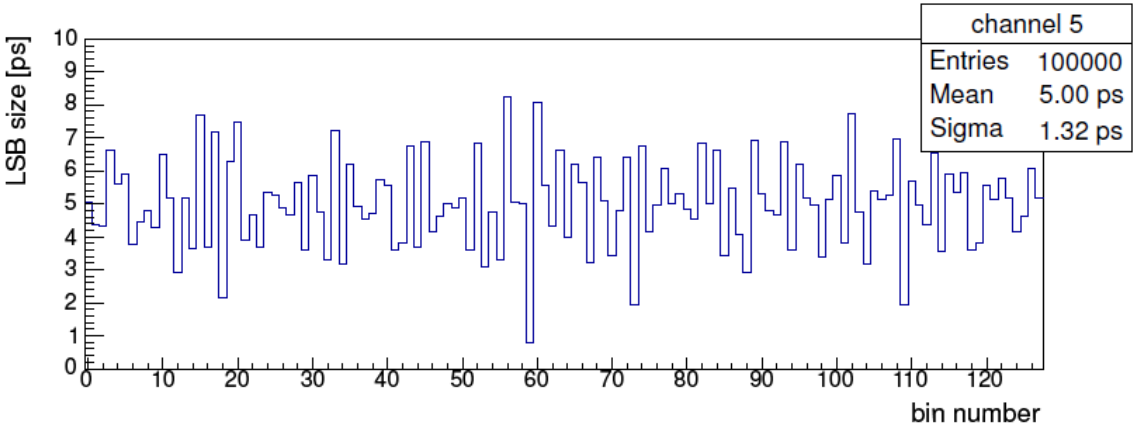
Distribution Buffer w/ Calibration



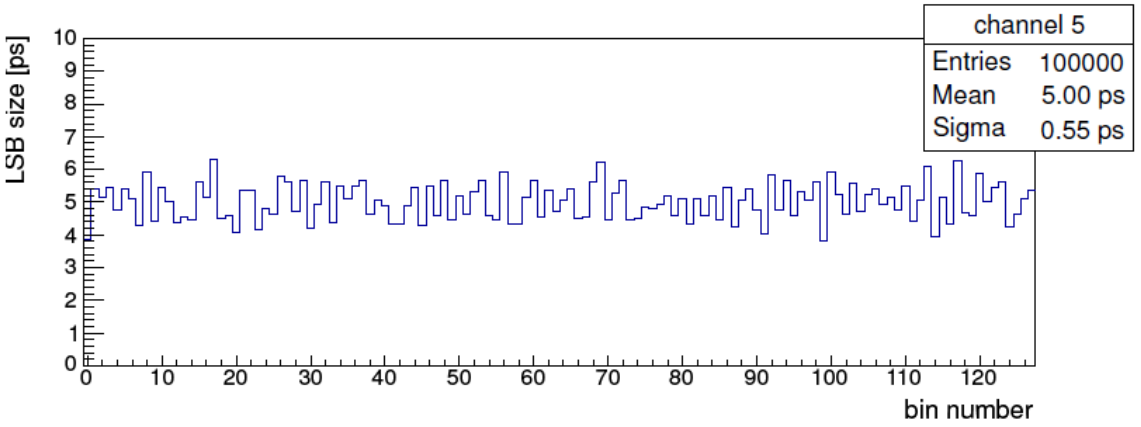
- binary weighted calibration (5 bits)
- delay can be varied from -16 ps to +15 ps in 1 ps steps
  (2fF per step)
- can correct INL errors up to 6.4 LSB



(a) No (uniform) calibration



(b) Global calibration



(c) Single channel calibration

Figure 6.19: Measured LSB size of channel 5 for different calibration settings.

Calibration Efficiency

No calibration

Device mismatches coming from

- Fine-time interpolator
- Time Capture registers

Global calibration

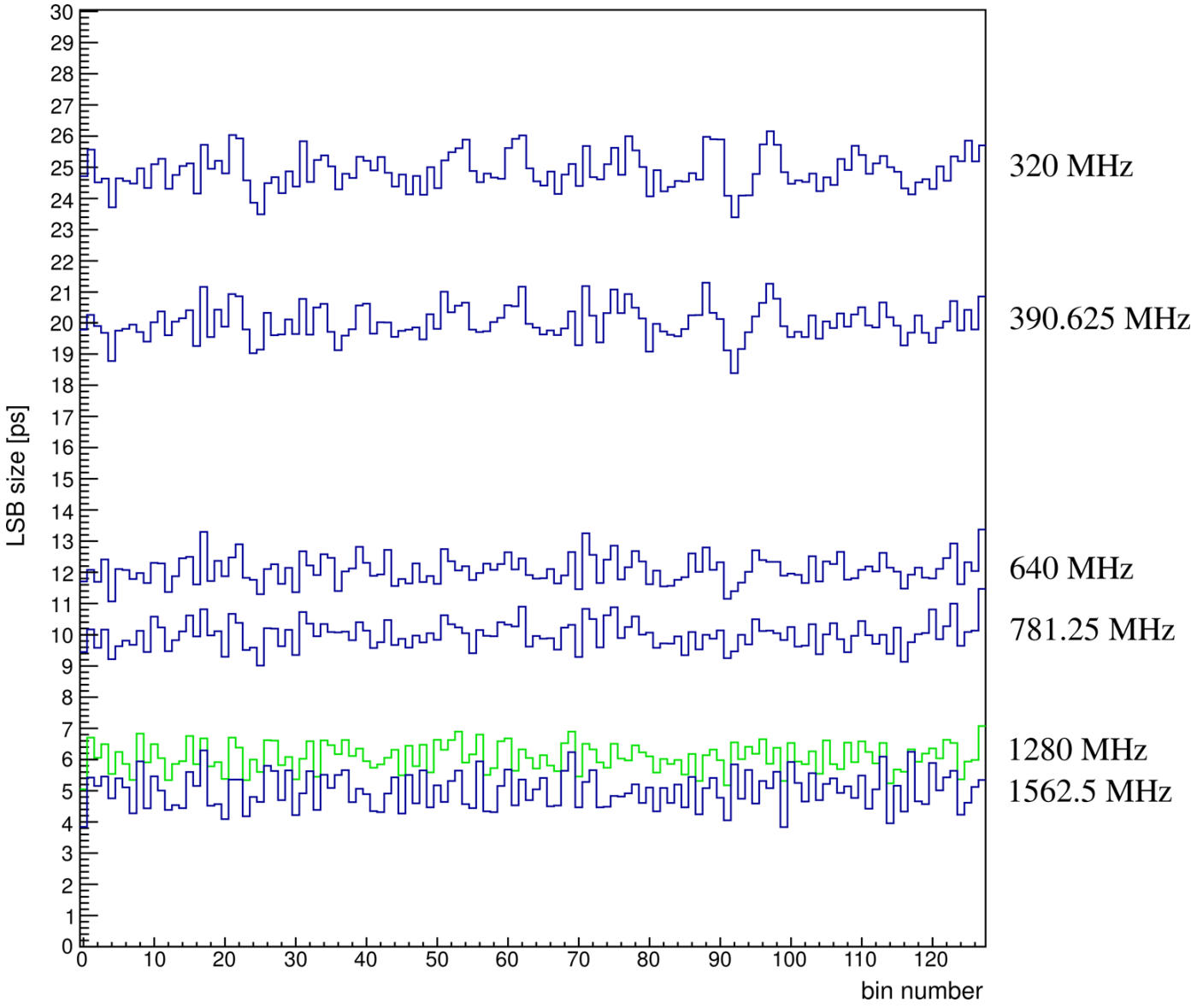
Device mismatches coming from

- Time Capture registers only

Single channel calibration

Ideally cancels all device mismatches

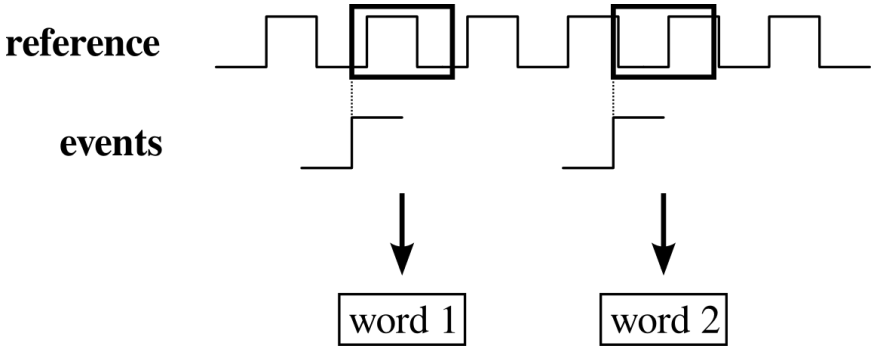
Variable LSB Size (CH5)



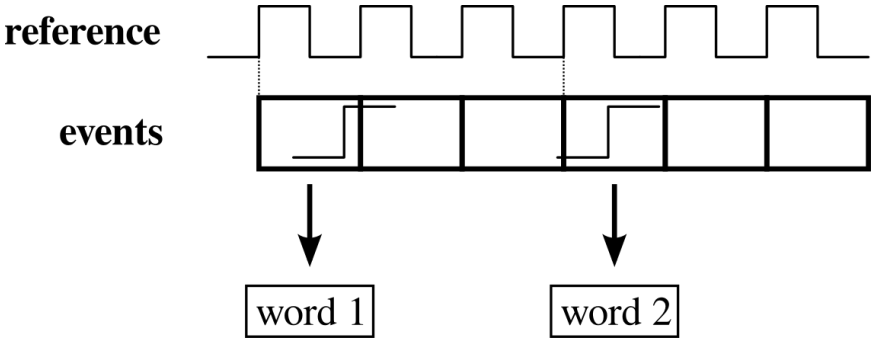
after single channel calibration

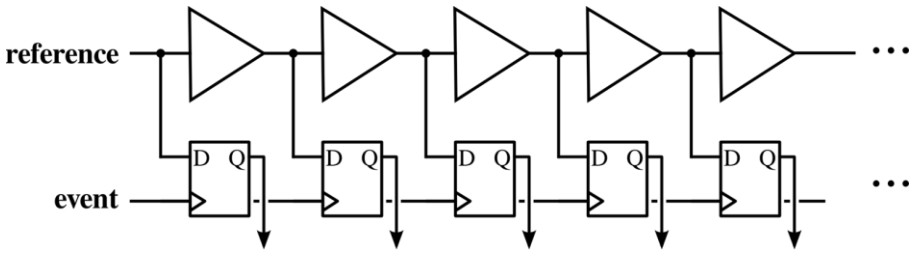
Clock vs. Event Capture

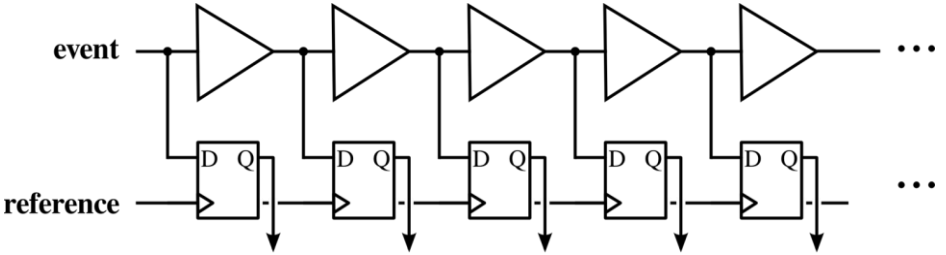
capture state of the reference signal



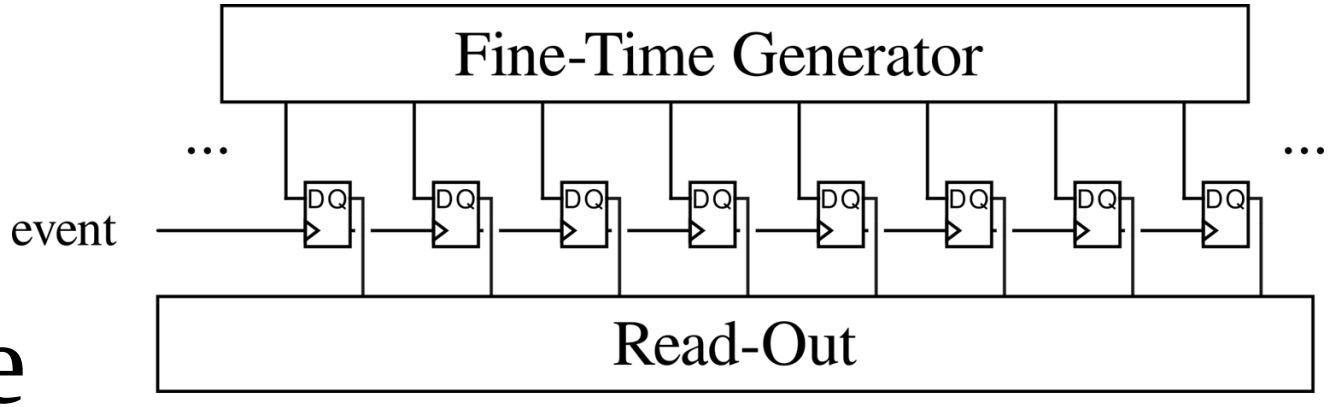
capture state of the event signal

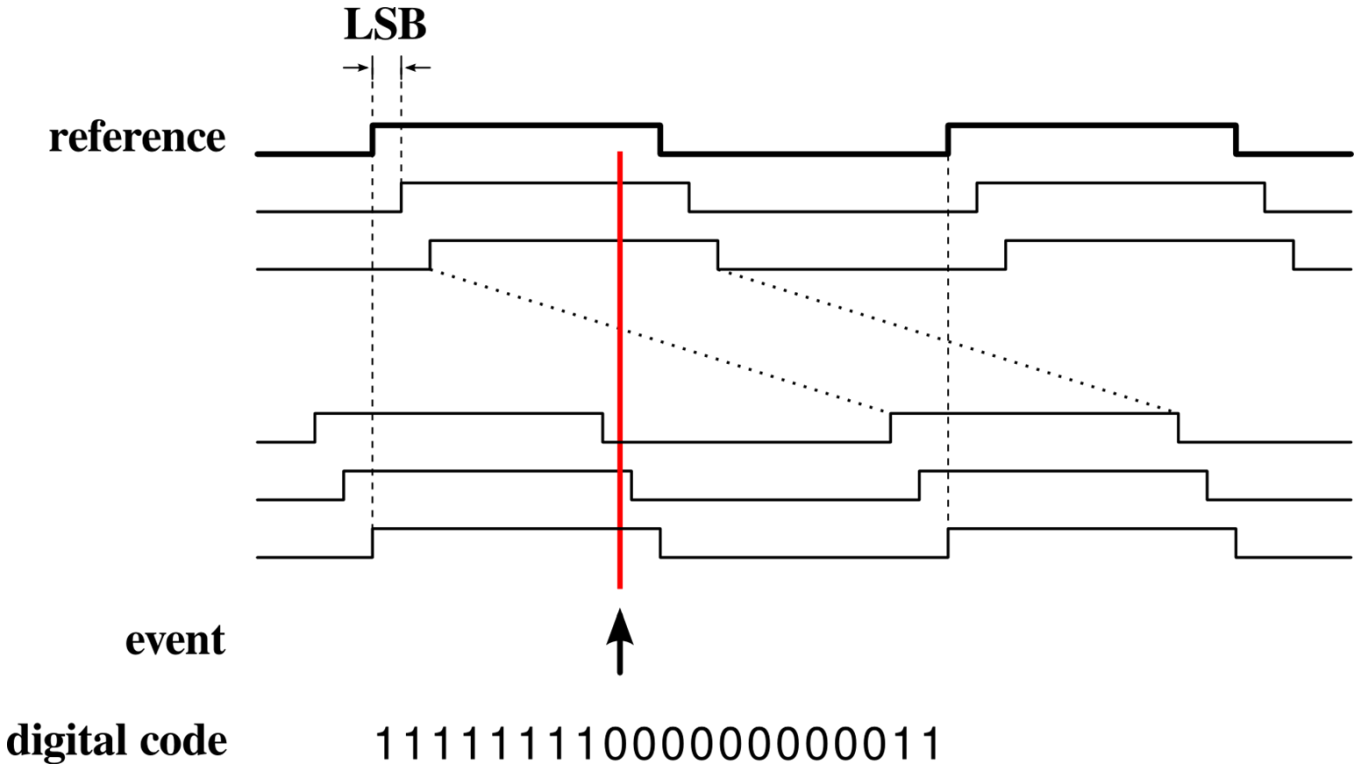






Clock Capture Architecture

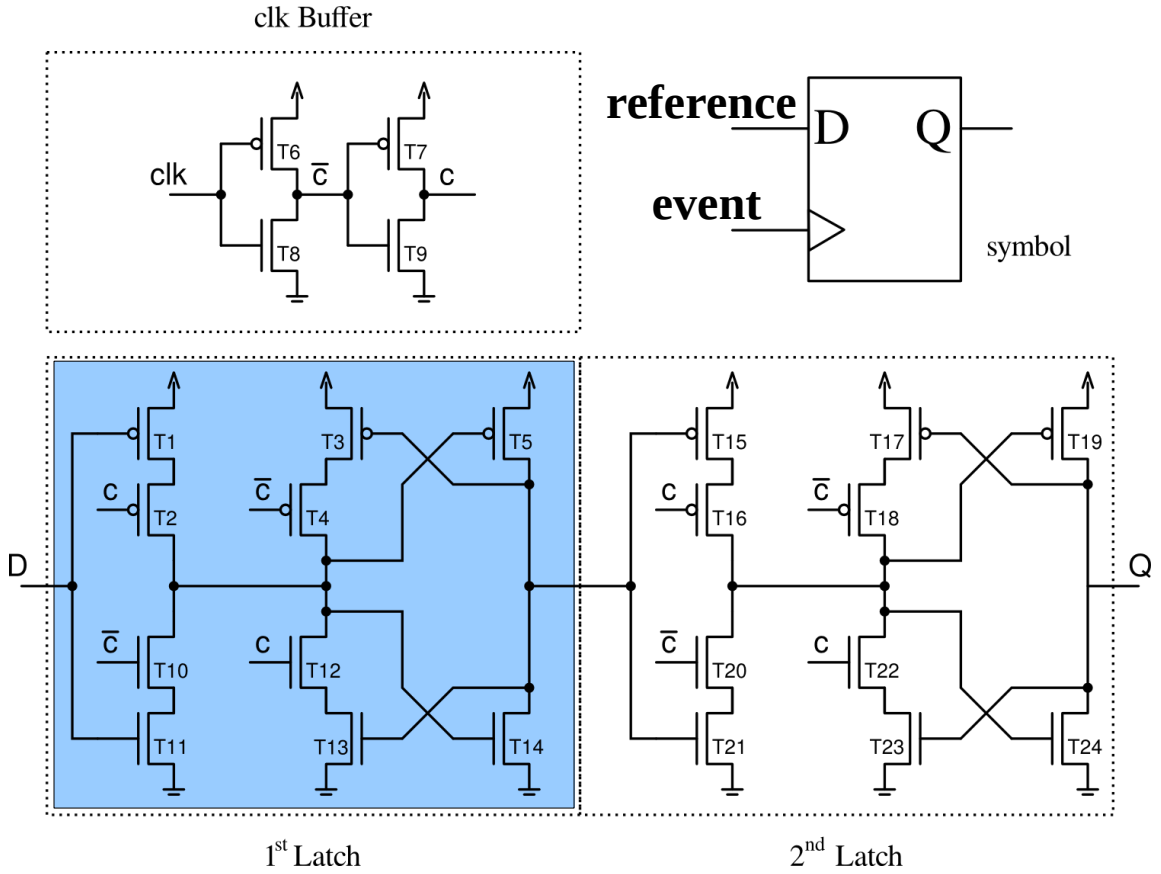




Clock Capture Register

no calibration in FF:

Trade off: power & resolution

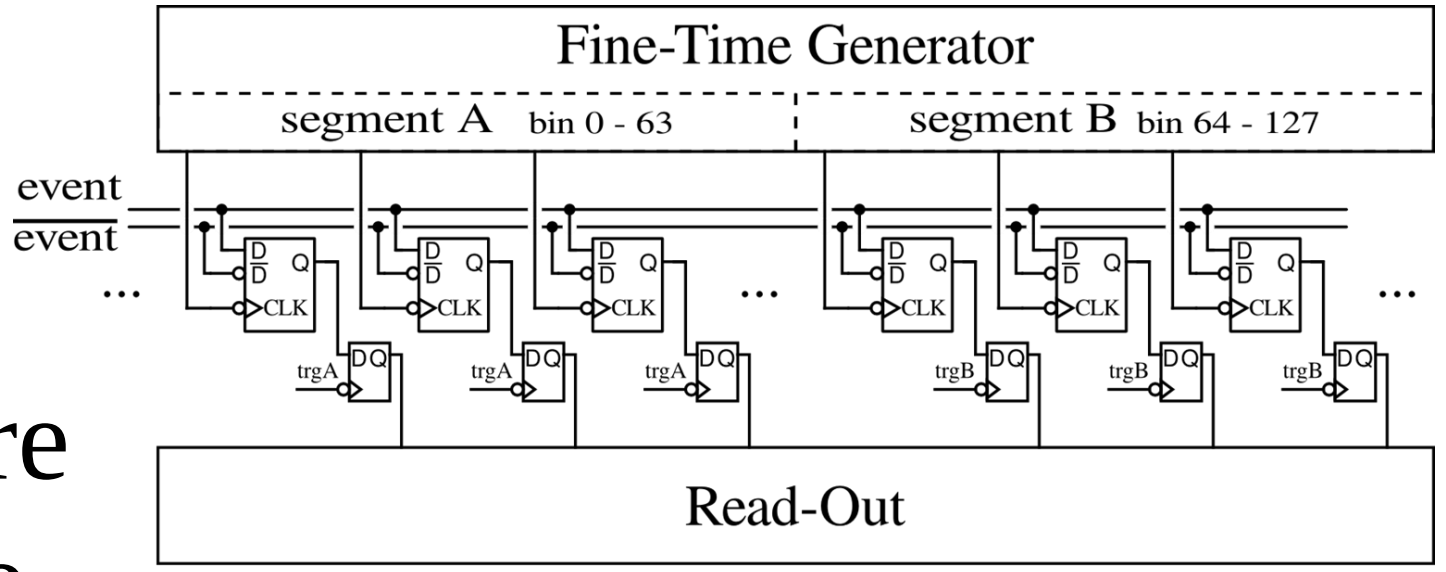


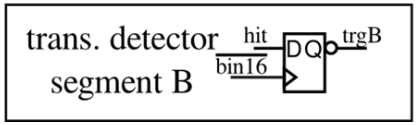
1-Latch optimized for timing (3x size of standard cell FF)

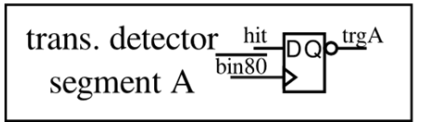
σ_{TDC} = 1.3 ps-rms

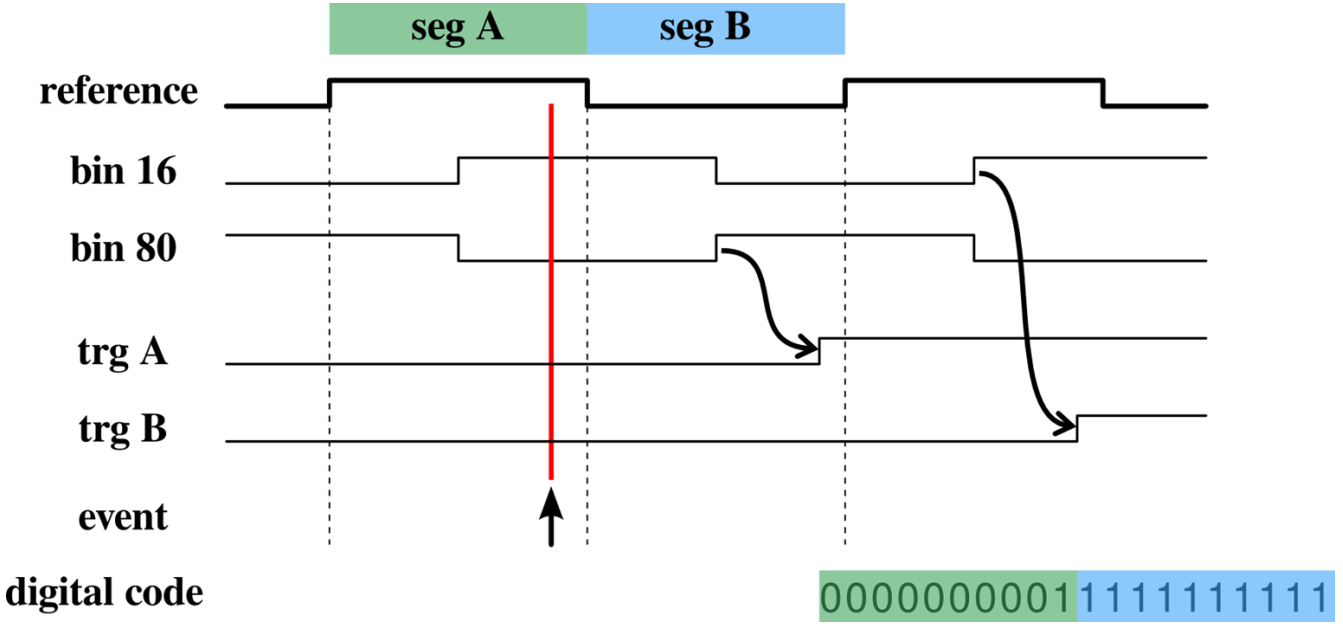
Just about good enough for 5 ps TDC

Event Capture Architecture





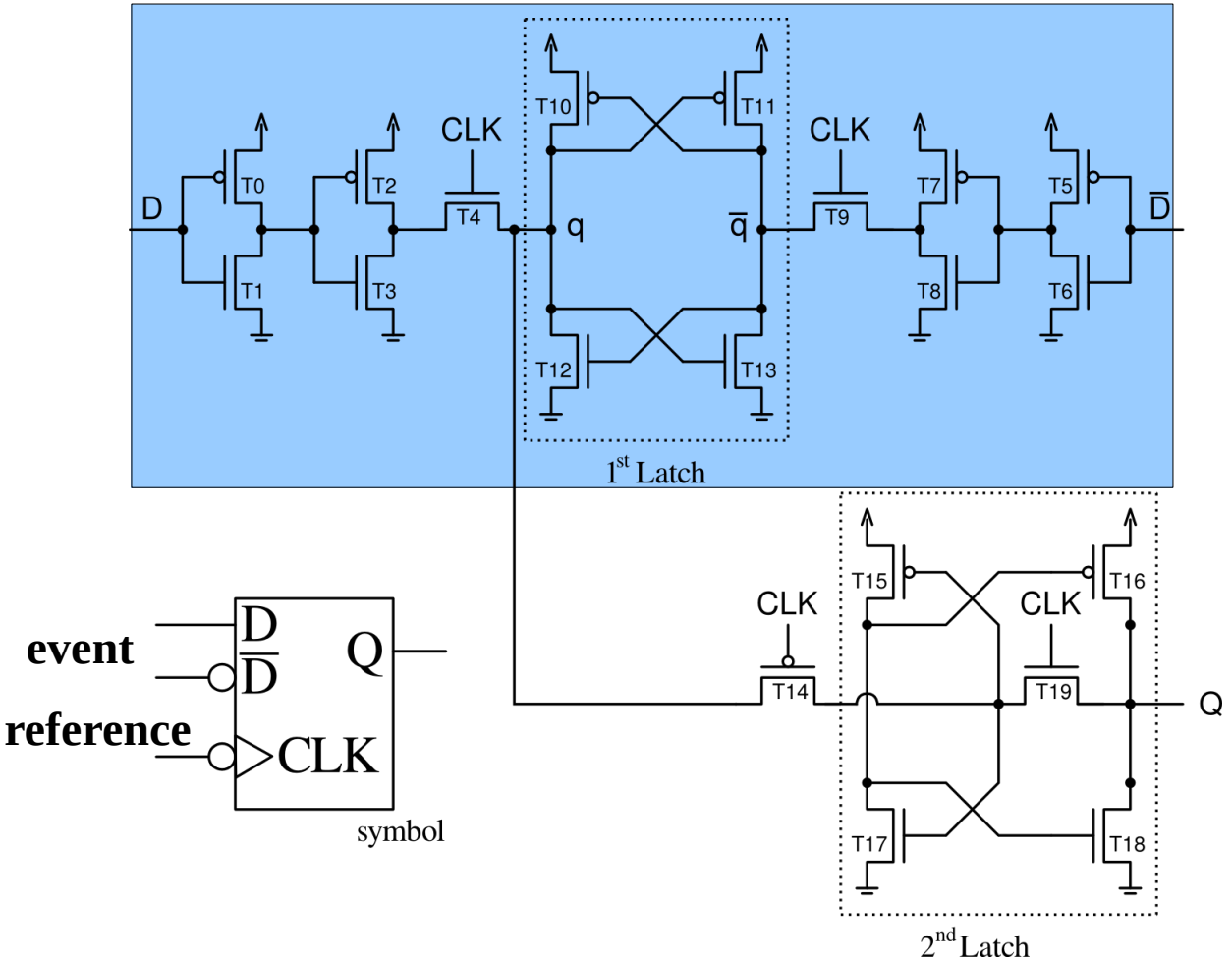




Event Capture Register

no calibration in FF:

Trade off: power & resolution

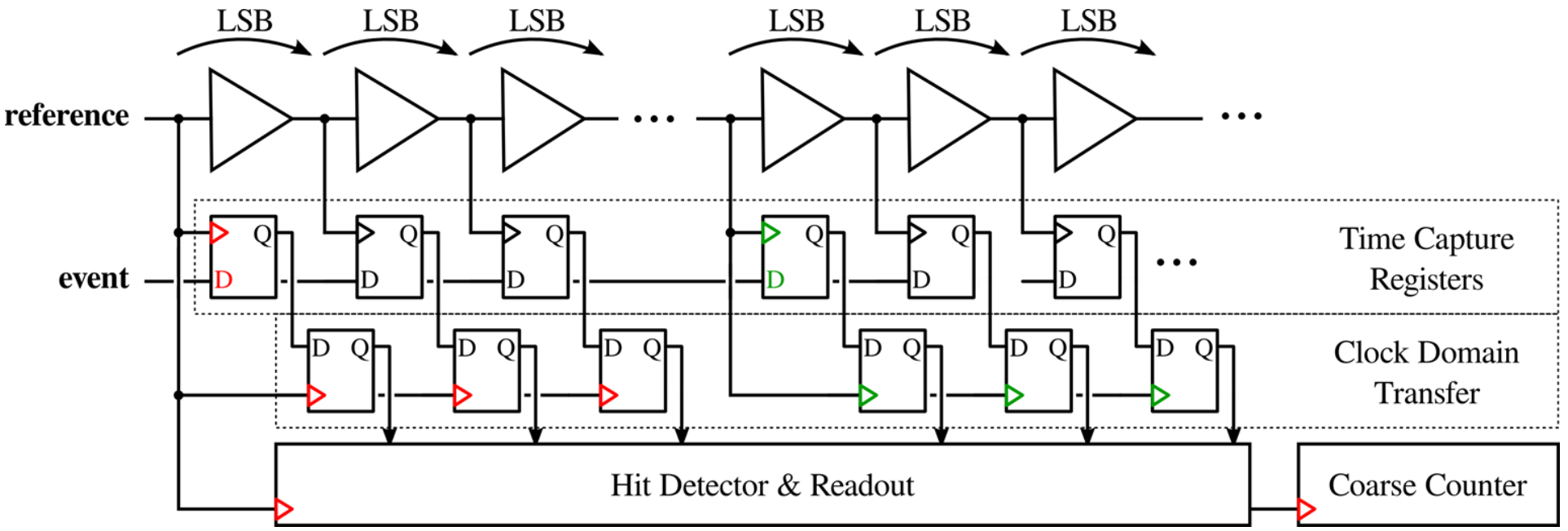


1-Latch optimized for timing (3x size of standard cell FF)

σ_{TDC} = 1.3 ps-rms

Just about good enough for 5 ps TDC

Event Sampling



- no delay on event signal (global interpolation approach)
- need to identify an event within one clock cycle
- additional registers clocked with the reference signal

Detailed Power Consumption I

Table 5.14: Power consumption estimates of the respective blocks of the demonstrator.

Block	acquisition on	acquisition off
Interpolator	71 mW	
Delay Line	40 mW	
Resistive Interpolation	28 mW	
Loop Components	3 mW	
Channel Matrix	163 mW	109 mW
Distribution Buffers	109 mW	
CH 1-2	-	
CH 3-6	11.1 mW	0 mW
CH 7-8	4.8 mW	0 mW

Detailed Power Consumption II

Table 6.4: Measured power consumption of respective blocks of the demonstrator supplied with 1.3 V.

Frequency [MHz]	Global Interpolator	Channel Matrix		I/O
		acquisition on	acquisition off	
1562.5	85 mW	185 mW	117 mW	72 mW
1280	70 mW	152 mW	97 mW	72 mW
781.25	43 mW	95 mW	60 mW	72 mW
640	36 mW	80 mW	50 mW	72 mW
390.625	24 mW	50 mW	33 mW	72 mW
320	20 mW	42 mW	28 mW	72 mW

Channel Performance Comparison

Table 6.3: Measured rms-time resolution of different channels and LSB size settings.

Channel	LSB	Δ Bin	Double-Shot	Single-Shot	Expected
1 & 2	5 ps	-20 LSB	5.25 ps-rms	3.71 ps-rms	3.03 ps-rms
3 & 4	5 ps	21.7 LSB	3.05 ps-rms	2.16 ps-rms	2.10 ps-rms
5 & 6	5 ps	3.2 LSB	3.37 ps-rms	2.39 ps-rms	2.10 ps-rms
7 & 8	10 ps	-3.7 LSB	7.02 ps-rms	4.96 ps-rms	4.03 ps-rms
5 & 6[a]	6.1 ps	8.8 LSB	4.09 ps-rms	2.89 ps-rms	2.11 ps-rms
5 & 6[a]	10 ps	5.4 LSB	5.50 ps-rms	3.89 ps-rms	3.70 ps-rms
5 & 6[a]	12.2 ps	4.5 LSB	6.34 ps-rms	4.49 ps-rms	3.89 ps-rms
5 & 6[a]	20 ps	2.7 LSB	9.79 ps-rms	6.92 ps-rms	8.20 ps-rms
5 & 6[a]	24.4 ps	2.2 LSB	11.26 ps-rms	7.96 ps-rms	9.50 ps-rms

[a]Erroneously applied single channel calibration for channel 5.